Power optimization in current mode circuits

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Abstract

We propose a method to minimize power dissipation in current-mode CMOS analog and multiple-valued logic (MVL) circuits employing a stack of current comparators. First, we present an approximation model for current in a current comparator circuit. Power reduction is achieved through turning off the redundant comparator circuits using a switch-architecture. Simulations are carried-out for current-mode flash ADC designs and literal generating circuits for MVL. We show that the simple switch architecture with minimum area overhead can be used to trade-off power dissipation with delay in these designs.

1. Introduction

Wide spread interest in wireless communication and portable computing has created a critical need for low-power low-voltage analog and digital integrated circuits. The three components of power dissipation in CMOS logic are switching, static (or leakage) and short-circuit. Of the three components, the dominant component in analog and multiple-valued logic circuits being static power dissipation. Therefore, static power reduction is an important optimization constraint in analog and MVL circuit design.

Current-mode circuit techniques, which process the active signals in the current domain, offer a number of advantages [1]. Current comparator is a fundamental component of current-mode analog integrated circuits. A critical design aspect for comparator is good trade-off between sensitivity, speed and power dissipation. Speed, in fact, can usually be increased at the expense of higher power consumption, while sensitivity requires high gain and hence low bias current, which leads to a slower time response. In the last decade, several comparator architectures have focused to address some of these issues [2]-[5]. When circuits employ a set of comparators for purposes such as those in flash ADC and literal based multiple-valued logic modules, the comparator set generates a thermometer code that reflects the input signal amplitude. As the input signal amplitude increases, more and more comparators are turned on thereby establishing a large static current from power supply to ground. Since we are interested in the outputs of only those comparators whose output changes from zero to one for the given input, we can, in principle, turn-off many of the comparators whose outputs are already high and that they do not contribute any information to the final digital value. This can be accomplished by introducing switches at appropriate places to turn off the current drawn by such comparators without affecting the final output value. The approach is analogous to selective signal gating in digital circuits.

2. Power dissipation in current comparators

It is a well-understood fact that the power dissipated in a digital circuit can be expressed as

$$P = C.V_{DD}^2.f.\alpha + t_{sc}.I_{peak}.V_{DD}.f.\alpha + I_{leakage}.V_{DD} \quad (1)$$

where C, f, α and t_{sc} are the total switching capacitance, clock frequency, switching activity factor and the time during which a short circuit exists between supply and ground respectively. The three terms on the right hand side of (1) correspond to dynamic power, short-circuit power and leakage power respectively

In the case of analog circuits, the dynamic power component and the associated short circuit power components are far too small compared to the static component. The static power dissipation is again due to two terms, one resulting from the finite resistance

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path from supply to ground due to triode and saturation region operation of the transistors, and the other being junction leakage component similar to the one in digital circuits. In our discussion, as a first approximation we shall neglect the leakage power and the switching (dynamic and short circuit) power in comparison to the power dissipation due to finite resistance path from supply to ground.

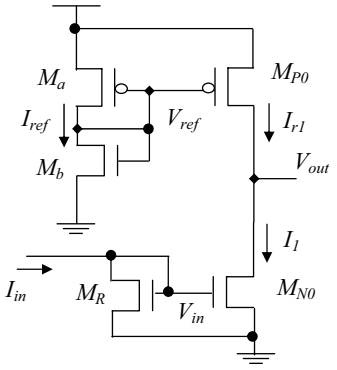

Fig. 1 Simple current comparator with a reference current generator

Figure 1 shows the current comparator circuit proposed in [2]. It compares a current signal, I_{in}, with a predetermined reference, I_{r1}, and generates a two-level voltage signal V_{out}. Let us assume that M_{N0} is identical to M_R, M_{P0} is identical to M_a, and that there are no errors due to lithographic effects in forming the transistors. There are three modes of operation.

Case 1. $I_{in} = I_1 = I_{r1}$. Both M_{N0} and M_{P0} are in saturation mode and $V_{out} \approx V_{DD}/2$.

Case 2. $I_{in} > I_{r1}$. M_{N0} is in the triode mode, M_{P0} is in saturation mode, and V_{out} is set at its low level.

Case 3. $I_{in} < I_{r1}$. M_{N0} is in the saturation mode, M_{P0} is in triode mode, and V_{out} is set at its high level.

The circuit path from supply to ground in the comparator branch (through M_{N0} and M_{P0}) will carry a current equal to I_{ref} in case 1 and almost equal to I_{ref} in case 2 and equal to I_{in} in case 3.

In case 1, the current in the comparator branch is given by,

$$I_{r1} = \frac{\mu C_{ox}}{2}\frac{W}{L}\left(V_{GS} - V_T\right)^2 \qquad (2)$$

where μ, C_{ox}, W, L, V_{GS} *and* V_T are the mobility, gate capacitance, channel width, channel length, gate to source voltage and threshold voltage respectively for the PMOS and NMOS transistors.

In case 2, the actual current flowing in the comparator will not be exactly equal to I_{ref}. This is because the voltage drop across the PMOS transistor will be much larger than that across the NMOS transistor. This means, the drain to source voltage, V_{DSP}, of M_{P0} will be larger than the drain to source voltage, V_{DSA}, of M_a, and hence the current I_{r1} in M_{P0} will be larger than I_{ref} due to channel length modulation. In this case, I_{r1} is given by [6],

$$I_{r1} = I_{ref}(1+\varepsilon) \qquad (3)$$

The error, ε, is given by,

$$\varepsilon = \frac{V_{DSP} - V_{DSA}}{V_A} \qquad (4)$$

where V_A is the Early voltage. The error could be as large as 30% or more and stems from finite output resistance of the MOS transistor. In case 3, a similar situation exists when the input current, I_{in}, is much smaller than the reference current. In this case, the current in M_{N0} will be larger by $(1+\varepsilon)$ times I_{in}. Thus in extreme cases where $I_{in} << I_{ref}$ or $I_{in} >> I_{ref}$, exact current mirroring does not take place with this comparator configuration. Such errors can be minimized by considering long channel transistors or by using other current mirror configurations such as cascade configuration. As a second approximation, we neglect this error and assume a relation between I_1 and I_{in} as depicted in fig. 2 for the simple current comparator configuration depicted in fig. 1.

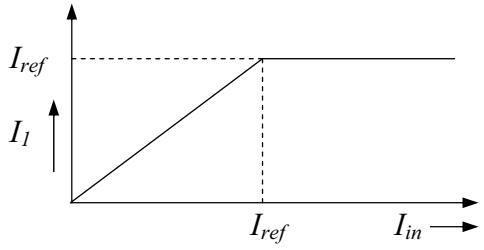

Fig. 2 Relation between I_{in} and I_1

Section 3 gives a description of the switch architecture used for power optimization.

3. Switch Architecture

Our power optimization scheme assumes a circuit topology wherein a number of current comparators are used to compare the input current signal to generate a thermometer code. Figure 3 shows the schematic of power optimization scheme using the switch and 4 shows the circuit diagram of the switch. In fig. 3, each comparator (CMP) is equal to the M_{P0} and M_{N0} connection of fig. 1 with the gates of PMOS and

NMOS transistors connected to V_{ref} and V_{in} respectively. For a given input signal, let us assume that the comparator outputs from 1 to J are high, and above J are low (thermometer code). In this case, J^{th} output is of significance and, we can turn off the PMOS devices of lower comparators by switching their gates to V_{dd}. This, however, will not alter the comparator outputs, but stop the current drawn from the supply and thereby reducing the power dissipation.

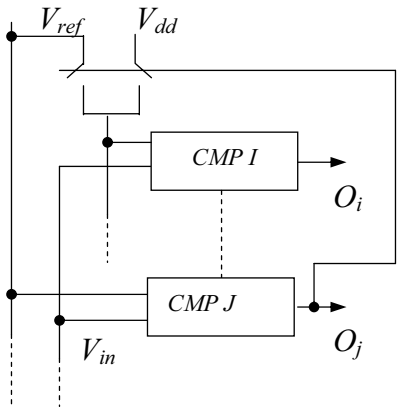

Fig. 3 Power optimization scheme

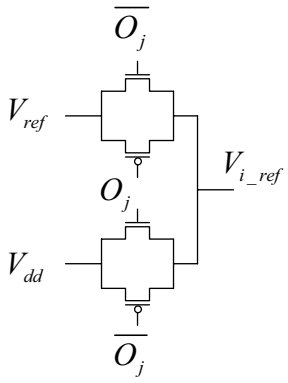

Fig. 4 Circuit diagram of the switch

In the following section, we apply this technique for power optimization in current-mode flash ADC circuit and window-literal circuit for self-restoring logic architecture used in the realization of multiple-valued logic functions

4. Current-mode Circuit Examples

4.1 Flash ADC

We designed a 7-bit current-mode flash ADC using current comparators. The ADC was designed for a dynamic range of 32μA. The block schematic of the design is shown in figure 5 and the circuit schematic of the reference block, input block and the current comparator block (blocks A, B & C respectively) is shown in figure 6.

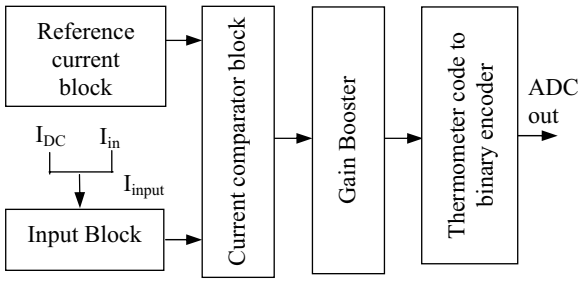

Fig.5 Schematic of flash ADC

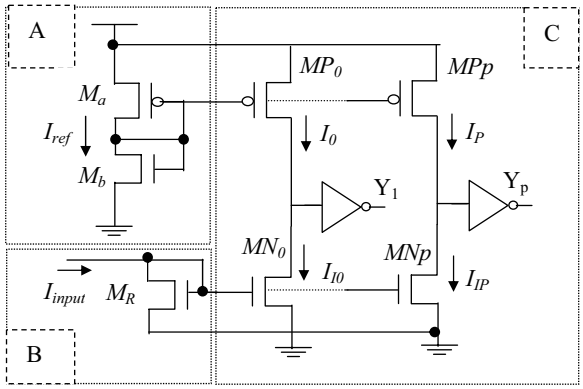

Fig. 6 Circuit schematic of basic ADC block

The *reference current block* generates a reference current I_{ref} and the *input block* receives the input current I_{input}. The input current is the sum of I_{in} and I_{DC}, where I_{in} corresponds to the input signal fed in for conversion and I_{DC} is used to provide adequate DC bias to maintain the required input signal bandwidth. The effect of I_{DC} is corrected to avoid offset in the ADC by appropriately increasing the reference currents. The current comparator block consists of 128 current comparators comprising 128 PMOS and NMOS current mirrors. The reference current, I_{ref}, is replicated by the PMOS current mirrors such that the current flowing in these mirrors progressively increase from I_0 (first mirror) to I_{127} (last mirror). The reference currents flowing in successive current mirrors differ by,

$$\Delta I = (I_{127} - I_0) / 128 \qquad (5)$$

The difference in successive transistor widths required to achieve this current difference is given by,

$$\Delta W = (W_0 / I_0)\,\Delta I \qquad (6)$$

where W_0 is the width of M_{P0}. The input current, I_{input}, is also replicated by NMOS current mirrors to generate 128 identical copies. These are then compared with the reference currents to generate the thermometer code. The voltage gain of the comparators is boosted by the gain booster circuit, which consists of cascaded sections of inverters.

The ADC is designed using 0.7-μm MIETEC CMOS technology. We could achieve a maximum sampling speed of 80Ms/sec at a power consumption of 78mW.

To optimize power, we modified the ADC architecture by employing power saving switch as shown in fig. 7. The circuit differs from the one depicted in figure 6 in that it includes switches to turn-off the redundant currents being drawn from V_{dd}. 128 comparators of the ADC are grouped in such a way that each group consists of, say, k comparators. (We have taken k as a power of 2. Number of groups when k=16 is 8, CCMP0-CCMP7). Switches can be introduced in all groups except the last group. For a given value of input current, full reference current gets established in those comparators whose outputs have gone high whereas, only a portion of the reference currents flow in the remaining (higher order) comparators, and hence their output is at logic low. Thus, if the outputs of i^{th} group of comparators are high, then all the lower group outputs also will be high. In this scenario, we can turn-off reference PMOS transistors of lower group of comparators by connecting their gates to V_{dd}, there by forcing the reference currents in these transistors to go zero and at the same time, maintaining their outputs intact (at logic high). For low values of input current, most of the switches are on and there is hardly any power saving. As the input signal magnitude increases, we see more and more reference currents being turned-off, there by saving significant amount of power. It is observed that the input signal amplitude for which maximum power is dissipated shifts from $I_{in}(max)$ to 0.5* $I_{in}(max)$ as the number of comparator groups are increased from one to 16.

Power saving in ADC comes at the cost of increased delay. It is found that the number of comparators per group have a bearing on both power saving and delay. Figure 8 shows power delay trade-off as a function of number of comparator groups

Simulation results show that the average power can be reduced by 23% with a delay penalty of around 9%, which corresponds to 5 comparator groups (each group consisting of around 26 comparators).

Simulation results showing total current drawn by the set of comparators when the input signal is swept from zero to 32μA is depicted in figure 9. The numbers on the right side of the graph indicate the number of comparators in each group. From the graph, we see that when the input signal amplitude is small (i.e., less than 20% of $I_{in}(max)$), grouping doesn't have any significant effect on power dissipation. This means that we can have asymmetric grouping with more number of comparators in lower groups and less number of comparators in higher groups. Such a grouping would further improve power reduction as well as delay.

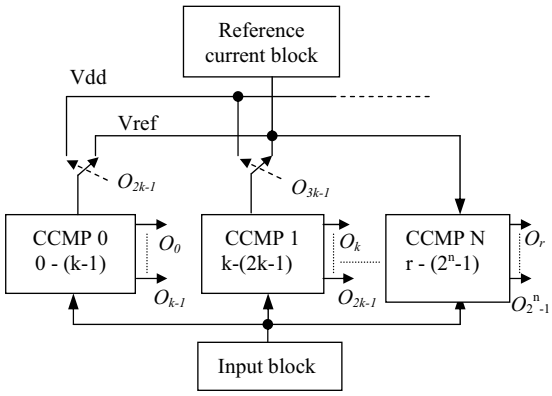

Fig. 7 Power optimized ADC

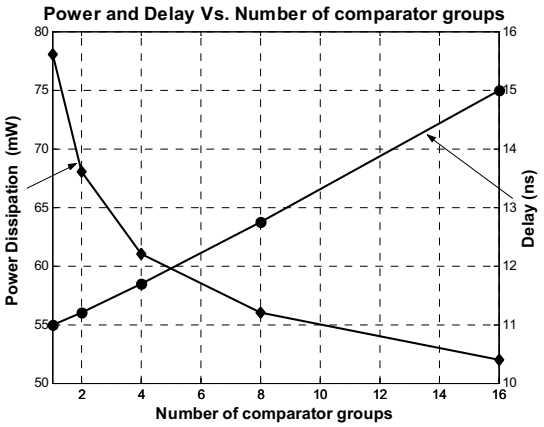

Fig. 8 Power-Delay tade-off

4.2 Literal generating circuit for Multiple-Valued Logic

Multiple-Valued Logic (MVL) designs have been receiving considerable attention over a couple of decades. The signal processing on the basis of the

multiple-valued logic is carried out using multiples of logic levels and thresholds, in contrast to binary logic with its two states. Most of the designs are current-mode circuits because of their advantages over voltage-mode circuits [7]-[8].

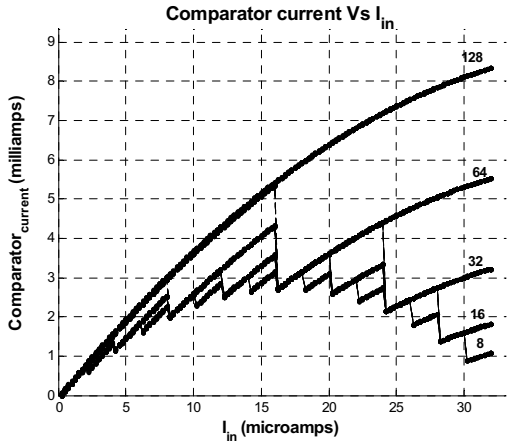

Fig. 9 Comparator current with grouping

When literals are used to realize MVL functions as in the case of *self-restoring logic architecture* [9], it is necessary to generate different logic values for each variable. Current signals are used to represent the logic levels with assignments such as Logic 0 = 0 (no current), Logic 1 = I_0, Logic 2 = $2I_0$, and so on with I_0 equal to, say, 10μA. An obvious choice to determine the current level is a current comparator circuit.

The literal generating circuit of an *m*-valued logic is very similar to that shown in fig. 6 except for a few additional binary logic gates. However, the total number of current comparators would be far too less than that used in an ADC and we can introduce switches to turn off every comparator except the last one, for power optimization. For an *m*-valued, *n*-variable logic function, the total number of comparators would at most be equal to *(m-1)n*.

Power dissipated in the comparator block depends on the literal values present in the function. For functions with each variable assuming equi-probable literal values, the average current drawn per variable is given by,

$$I_{AVG} = \frac{m+1}{2} I_{in} + \frac{1}{2}\left(\frac{(m+1)(m+2)}{6}+1\right) I_0 \quad (7)$$

For a function with *n*-variables,

$$I_{TOT} = n.I_{AVG} \quad (8)$$

and the average power dissipated by the comparator block is,

$$P_{CMP} = I_{TOT} V_{DD} \quad (9)$$

When switches are introduced for each variable to turn off the redundant comparators, the average current drawn by the comparator block per variable is given by,

$$\overline{I_{AVG}} = \frac{m+1}{2} I_{in} + \frac{m+1}{2} I_0 \quad (10)$$

Comparing (7) and (10), it is seen that the static current can be reduced significantly in functions with radix 4 and above. When the variable takes values *0, 1, 2, ... m-1* with probabilities $p_0, p_1, p_2, ... p_{m-1}$ respectively, then the average static current in the literal generating block without the power optimization switch is given by,

$$I_{P\_AVG} = \sum_{k=0}^{m-1} p_k \left[(m-k) I_{in} + I_0 + \frac{k(k+1) I_0}{2} \right] \quad (11)$$

With the power optimization switch in place, the average current in this case is given by,

$$\overline{I_{P\_AVG}} = \sum_{k=0}^{m-1} p_k \left[(m-k) I_{in} + k I_0 \right] \quad (12)$$

The actual reduction in power depends on the probability of the value that each variable takes in a given function.

We performed simulation experiments on a number of randomly generated 2-variable, 4- and 5-valued functions implemented on 0.13μm CMOS process in *self-restoring logic* style. All circuits were excited with the same input signals with equal literal probabilities. Some example functions are listed in table 1. Theoretically, a saving of around 20% can be achieved for these functions.

Simulation results show that a power reduction in the range of 5% - 19% is possible in these examples. A low value of power reduction in some cases is attributed to functions with variables not taking all logic values. Additional power saving can be achieved by introducing similar switches in the output block of the *self-restoring logic*, instead of using a *max-gate*. The delay introduced in these cases was almost same and did not exceed 6%.

Current comparator circuits are also employed in many other analog and fuzzy logic function realizations and there is scope for power reduction using the method suggested in this work. However, some problems may arise in precision analog and digital circuits due to charge injection with the insertion of the switches. In fact, this was a problem in current-mode flash ADC design. In such cases, additional circuitry has to be used to overcome this effect.

Table 1. Some 2-variable 4-valued functions used in the experiment

Function	Power Dissipation (μW)		
	Unoptimized	*Optimized*	*% Saving*
$f_1 = {}^{2}x_1^{3}\,{}^{0}x_2^{1} + 2\,{}^{0}x_1^{1}\,{}^{0}x_2^{0} + 3({}^{1}x_1^{1}\,{}^{1}x_2^{1} + {}^{2}x_1^{3}\,{}^{3}x_2^{3})$	*210*	*181*	*13.8*
$f_2 = {}^{2}x_1^{2}\,{}^{0}x_2^{0} + {}^{3}x_1^{3}\,{}^{1}x_2^{1} + {}^{0}x_1^{1}\,{}^{2}x_2^{2} + 2\,({}^{0}x_1^{0}\,{}^{0}x_2^{0} + {}^{1}x_1^{1}\,{}^{1}x_2^{1}) + 3\,({}^{3}x_1^{3}\,{}^{0}x_2^{0} + {}^{2}x_1^{2}\,{}^{1}x_2^{1} + {}^{1}x_1^{1}\,{}^{3}x_2^{3} + {}^{3}x_1^{3}\,{}^{3}x_2^{3})$	*214.9*	*192.3*	*10.5*
$f = {}^{1}x_1^{1}\,{}^{1}x_2^{2} + {}^{1}x_1^{3}\,{}^{2}x_2^{2} + 3({}^{2}x_1^{3}\,{}^{0}x_2^{0} + {}^{3}x_1^{3}\,{}^{0}x_2^{1}) + 2\left({}^{0}x_1^{1}\,{}^{0}x_2^{0} + {}^{0}x_1^{0}\,{}^{0}x_2^{1} + {}^{1}x_1^{3}\,{}^{3}x_2^{3}\right)$	*212*	*178.5*	*15.8*
$g = {}^{0}x_1^{0}\,{}^{0}x_2^{2} + {}^{1}x_2^{1} + {}^{1}x_1^{1}\,{}^{3}x_2^{3} + 3\,{}^{2}x_1^{2}\,{}^{3}x_2^{3} + 2\left({}^{1}x_1^{1}\,{}^{0}x_2^{0} + {}^{3}x_1^{3}\,{}^{0}x_2^{0} + {}^{1}x_1^{1}\,{}^{2}x_2^{2} + {}^{3}x_1^{3}\,{}^{2}x_2^{2}\right)$	*208.6*	*171.2*	*17.93*

5. Conclusions

Power optimization scheme, using switch architecture, in analog and multiple-valued logic circuits employing a series of current comparators is presented. A 7-Bit Current-mode Flash ADC and a number of 2-variable 4-valued functions were designed and simulated with and without power optimization scheme. Simulation results show that static power dissipation by the comparators can be significantly reduced with a nominal delay penalty. In the case of ADC, power delay trade-off can be achieved to give best results by varying the total number of comparator groups and by varying the number of comparators in each group. A power saving of 23% was achieved with an additional delay of 9% in flash ADC, while 5% -19% power saving was reported with an additional delay of 6% in the case of multiple-valued functions.

6. References

[1] C. Toumazou, F. J. Lidgey, and D. G. Haigh, *ed*., *Analogue IC design: the current-mode approach,* IEE circuits and systems series 2, 1990.

[2] Freitas, D. A. and Current, K. W., "CMOS current comparator circuit", *Electronic letters* 19(17), pp. 695-697, 1983

[3] Taff, H., "Novel approach to high speed CMOS current comparators", *Electronic letters* 28(3), pp. 310-312, 1992

[4] Tang, A. T. K. and Toumazou, C., "High performance CMOS current comparator", *Electronic letters* 30(1), pp. 5-6, 1994

[5] Chen, L., Shi, B., and Lu, C., "Circuit design of a high speed and low power CMOS continuous-time current comparator", *Analog Integrated Circuits and Signal Processing, Kluwer Academic Publishers*, 2001, pp. 293-297.

[6] Gray, P. R., Hurst, P. J., Lewis S. H. and Meyer, R. G., "Analysis and Design of Analog Integrated circuits", 4th Ed., John Wiley and Sons Inc., 2001.

[7] K.W. Current, "Current-mode CMOS multiple-valued logic circuits", *IEEE J. Solid State Circuits*, vol. 29, no. 2, pp. 95-107, Feb.1994

[8] A.K.Jain, R. J. Bolton and M. H. Abd-El-Bar, "CMOS Multiple-valued logic design – Part I: Circuit implementation", *IEEE Trans. On Circuits and Systems – I: Fundamental theory and applications*, vol. 40, no. 8, pp. 503-514, Aug. 1993.

[9] Teng, D. H. Y., and Bolton, R. J., "A self-restored Current-mode CMOS Multiple-Valued Logic design Architecture", *Proceedings of the 7th IEEE Pacific Rim Conference on Communications, Computers and Signal processing*, (Victoria, Canada), pp. 436-439, Aug. 22-24, 1999.