Impact of Channel Engineering on Unity Gain Frequency and Noise-Figure in 90nm NMOS Transistor for RF Applications

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Abstract

In this paper, we have studied and compared the RF performance metrics, unity gain frequency (f_t) and Noise Figure (NF), of the devices with channel engineering consisting of halo and super steep retrograde channel (SSRC) implants, and the devices with uniform channel doping concentration, using process, device, and mixed mode simulations. The simulation results show that at 90nm gate lengths, for a given off-state leakage constraint (I_{OFF}), devices with uniform channel doping concentration deliver higher f_t and lower NF than the devices which used halo and SSRC, due to better sub-threshold slope and transconductance. However, at 0.25μm technology the same is not true. Therefore, in the 90nm devices uniform channel doping profile is recommended to get better RF performance.

1. Introduction

Radio frequency (RF) integrated circuits in CMOS are developing a strong presence in the commercial world. For applications such as wireless LAN and Bluetooth, they are dominant, and in areas such as GSM cellular transceivers and GPS receivers, they are making inroads [1]. As the devices were scaled down, around the quarter micron (0.25μm) regime novel device structures such as halo (pocket) implantation, super steep retrograde channel (SSRC) profile and ultra shallow LDD junction were proposed to mitigate the short channel effects (SCE) [2]-[8]. However, halo implant can also result in degradation of drive current under certain conditions [9]. Since, the doping concentration in the halo region becomes very high for sub-100nm gate lengths, it is not clear whether there will be any significant performance enhancement especially with respect to unity gain frequency (f_t) and noise figure (NF). For analog/RF applications f_t and NF are two important metrics[10].

In this study, we have compared the non-uniformly doped channel MOSFET performance with the uniformly doped channel MOSFET in terms of these RF metrics.

Next section deals with the simulation methodology and gives details of the devices used in the simulation. In section 3, we discuss the results related to f_t and in section 4, the results related to NF. Finally we conclude by summarising the results.

2. Simulation Methodology

All the simulations are done using ISE-TCAD simulator. The transistors are defined using process simulation (DIOS). We have used the disposable spacer technique to control the short channel effect. NMOSFETs with poly gate length of 90nm, 0.12μm, 0.18μm and 0.25μm have been studied to compare and contrast the trends at different technology nodes. The gate oxide thickness, supply voltage (V_{DD}), and gate bias (V_{GS}) at different technology nodes are given in table .1.

Technology	V_{DD}/V_{GS} (V)	Gate Oxide Thickness ($\AA$)
90nm	0.9/0.45	15
0.12μm	1.2/0.6	20
0.18μm	1.8/0.9	30
0.25μm	2.5/1.25	45

Table 1. Table showing the bias voltages used for different devices

All the transistors in this study are designed to have I_{OFF}=1nA. Two different sets of transistors are studied in

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this paper. One set of transistors uses pocket halo and super steep retrograde channel (will be referred to as set I). Another set of devices does not use halo and SSRC (will be referred to as set II). Both the set of devices are identical in all other aspects. I_{OFF} constraint is met in set I by adjusting the pocket halo dose. In set II, the substrate doping concentration is adjusted to get the required I_{OFF}. Fig. 1 shows the lateral doping profile in the channel of 90nm transistors, for both set I and set II. The doping profile is taken along a cut-line, 100$\mathring{A}$ below Si-SiO_2 interface. The two halo peaks are very evident in fig. 1. Also, it is obvious from fig. 1 that the doping in the channel is uniform for the set II devices.

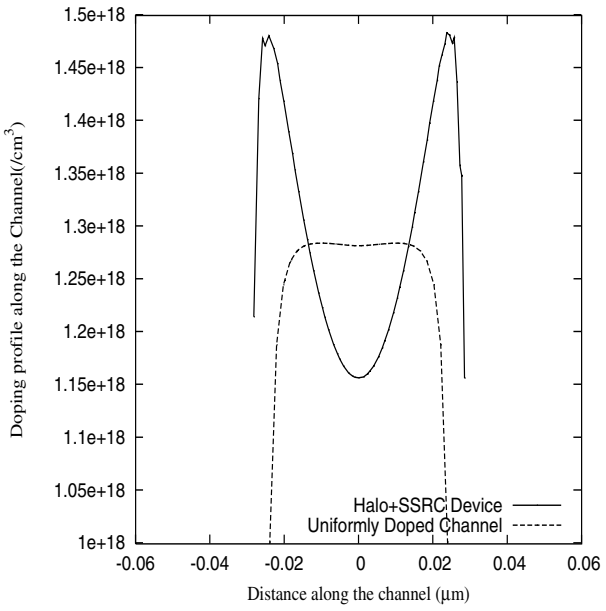

Figure 1. Doping profile along the channel, 100$\mathring{A}$ below Si-SiO_2 surface, for both set I (Halo+SSRC) and set II (Uniformly doped Channel) devices

DESSIS device simulator was used to extract f_t, G_m, mobility, threshold voltage, sub-threshold slope of devices and current noise spectrum at the terminals of the MOSFET. The physics section of the DESSIS includes the appropriate models for band to band tunneling, quantization of inversion layer charge, doping dependency of mobility, effect of high and normal electric fields on mobility, and velocity saturation. All the simulations are done at the 2D level and the results discussed in the paper are for transistor width of 1μm except noise figure related results wherein width of the transistor is varied.

The bias voltages are $V_{DS} = V_{DD}$ and $V_{GS} = V_{DD}/2$ for respective technologies (refer table. 1). Bias voltages are chosen to keep the devices in strong inversion and saturation, and to give maximum dynamic range. The standard AC simulations are done by applying a small signal at the gate, over a range of frequencies and the frequency at which $|\frac{y_{21}}{y_{11}}|$ equals to **1**, is taken as f_t [11]. Noise analysis was also done in DESSIS simulator for the same circuit setup and bias voltages. Source impedance (Z_S) of 50Ω (purely resistive) is assumed in order to calculate the noise figure.

3. Unity Gain Frequency

Fig. 2 shows the values of the f_t at different technologies (effective gate length is used for plotting, not the poly gate length), for set I and set II devices. We can see that at 0.25μm the set I devices i.e. devices with halo and SSRC implantation are offering higher f_t. Where as at 90nm the trend is different i.e. uniformly doped channel devices (set II) offer higher f_t.

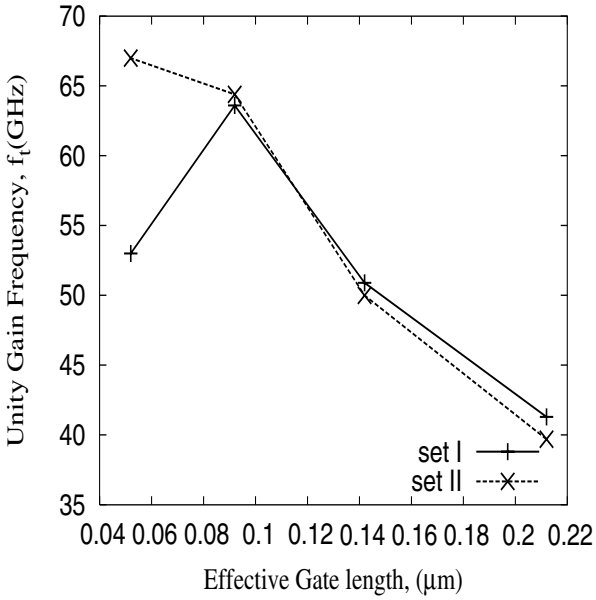

Figure 2. Unity Gain Frequency at different Technology Nodes (plotted against effective gate length, not the poly length) for both set I and set II devices, at the respective bias voltages as given in table. 1

We can understand this behaviour if we look at the transfer characteristics of these devices. The unity current gain frequency (f_t) obtained from $\mathbf{Y}$ parameters can be given in

terms of device parameters [12]

$$f_t \approx \frac{g_m}{2\,\pi\,C_{gg}} \quad (1)$$

where g_m is transconductance, and C_{gg} is total gate input capacitance. C_{gg} is the sum of gate to source intrinsic capacitance, overlap capacitance and fringing capacitance. Fig. 3 shows the $I_d - V_g$ characteristics of the 90nm and 0.25μm devices, having I_{OFF}=1nA.

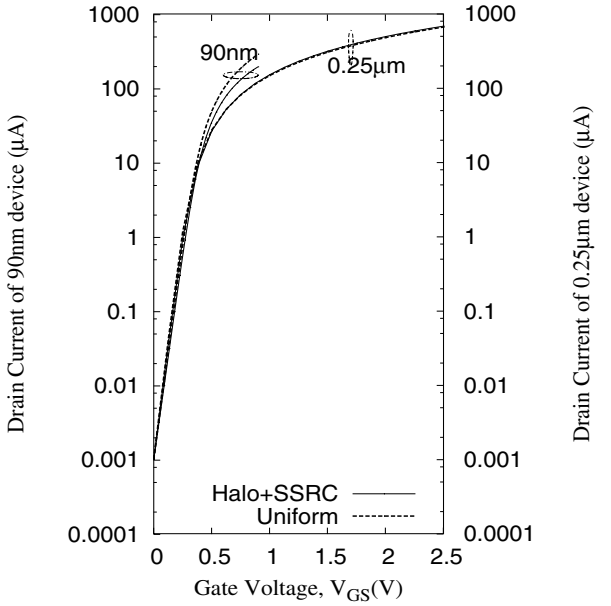

Figure 3. I_D - V_G characteristics for both set I and set II devices, at two different gate lengths, having I_{OFF}=1nA

It can be noticed from the above figure that at 90nm gate length set II devices give better $I_d - V_g$ characteristics than the set I devices. The very high halo dose at sub-100nm gate length results in degraded sub-threshold slope and mobility. This in turn results in better transconductance. Fig. 4 shows the transconductance of the 90nm and 0.25μm devices as a function of V_{GS} and fig. 5 shows the values of the g_m at different technologies, for set I and set II devices. All these devices have I_{OFF}=1nA. It is also interesting to see that in fig. 2, f_t of the set I devices does not increase monotonically and it is discussed in detail in [13]. Table. 2 gives the values of g_m and subthreshold slopes at two different gate lengths both for set I and set II devices, having I_{OFF}=1nA. Even though the results are shown only for I_{OFF}=1nA, the trend is same for I_{OFF}=10pA to 100nA. In summary, halo based devices are better at 0.25μm gate lengths whereas uniformly doped channel devices give higher f_t in 90nm devices.

Gatelength	g_m (μS)		Sub-threshold slope (mV/decade)	
	set I	set II	set I	set II
90nm	314	396	90.4	85.6
0.25μm	313	297	76.5	79.2

Table 2. Table showing the values of g_m and subthreshold slopes at two different gate lengths both for set I and set II devices, having I_{OFF}=1nA

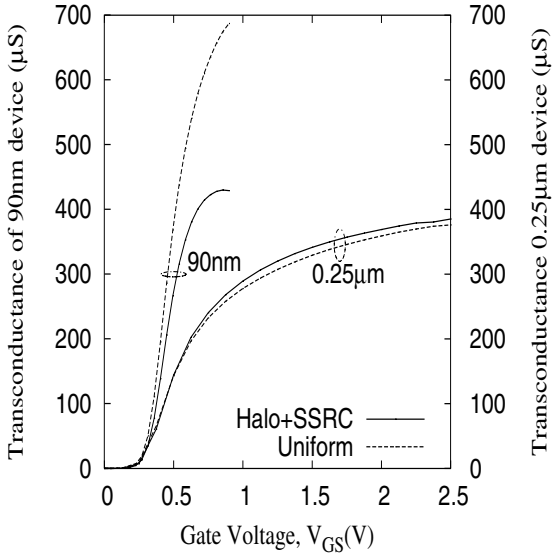

Figure 4. Transconductance as a function of V_{GS} for both set I and set II devices, at two different gate lengths, having I_{OFF}=1nA

4. Noise Figure

In order to calculate the noise figure the following formula was used [14]-[15]

$$NF = 1 + \frac{1}{{S_I}^S}({S_I}^{gg} + \mid \alpha \mid^2 {S_I}^{dd} - 2Re(\alpha {S_I}^{dg}) \quad (2)$$

$$with\ \ \alpha = (Y_S + Y_{gg})/Y_{dg} \quad (3)$$

where ${S_I}^S$ is the current noise spectrum of the noisy source admittance and is given by,

$${S_I}^S = 4k_BTRe(Y_S) \quad (4)$$

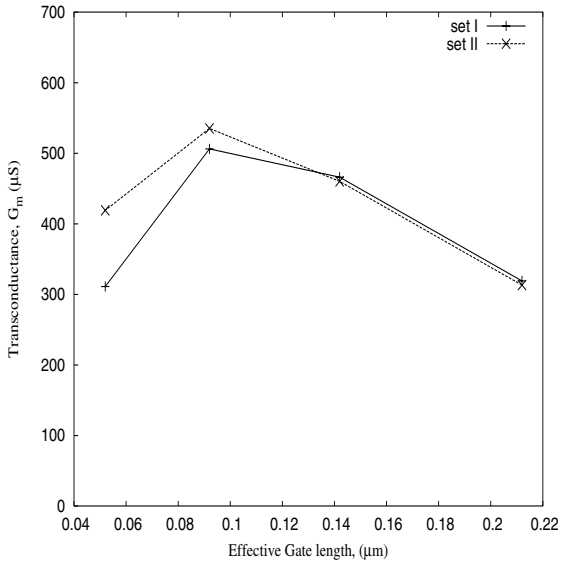

Figure 5. Transconductance at different Technology Nodes (plotted against effective gate length, not the poly length) for both set I and set II devices, at the respective bias voltages as given in table. 1

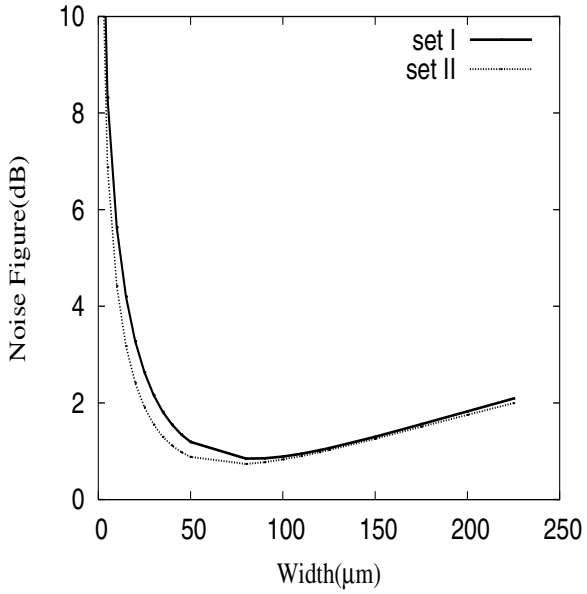

Figure 6. Noise Figure (@25GHz) plotted against Width of the transistor, for both set I and set II devices, at 90nm technology, at the respective bias voltages as given in table. 1

$S_I{}^{gg}$ and $S_I{}^{dd}$ are the current noise spectrum at the gate and drain terminals respectively, $S_I{}^{dg}$ is the cross-correlation current noise spectra between the drain and gate terminals, Y_{gg} and Y_{dg} are the respective admittance($\mathbf{Y}$) parameters. Fig. 6 shows the noise figure versus transistor width plot of 90nm devices, for both set I and set II.

We can notice for any given width, set II devices perform better. But at 0.25μm gate length the reverse is true and it is evident from the fig. 7. At 90nm gate length, set I devices due to their degraded transconductance (Fig. 5) produces higher $S_I{}^{gg}$ and α than set II devices. Therefore, as per equation (2), set I devices at 90nm gatelength result in higher NF.

5. Conclusion

We have compared the RF performance metrics, unity gain frequency and noise figure of the devices which used halo and SSRC implantation and the devices which used a uniform channel doping. We have shown that at 90nm gate length, the uniformly doped channel devices perform better than the halo-SSRC based devices in terms of these RF metrics. This is due to the fact that a very high halo doping concentration in the pocket halo regions results in worse sub-threshold slope and mobility, which inturn gives rise to degraded transconductance.

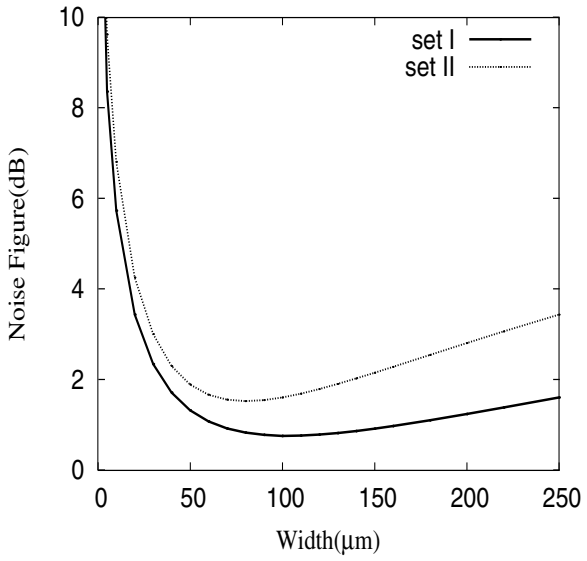

Figure 7. Noise Figure (@25GHz) plotted against Width of the transistor, for both set I and set II devices, at 0.25μm technology, at the respective bias voltages (table. 1)

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