A High Switching Frequency IGBT PWM Rectifier/Inverter System for AC Motor Drives Operating from Single Phase Supply

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Abstract—**A PWM rectifier/inverter system using insulated-gate-bipolar-transistors (IBGT's), capable of switching at 20 kHz is reported. The base drive circuit for the IGBT, incorporating short circuit protection is presented. The inverter uses Undeland snubber together with a simple energy recovery circuit, which ensures reliable and efficient operation even for 20 kHz switching. The front end for the system is a regenerative single phase full-bridge IGBT inverter along with an ac reactor. Steady-state design considerations are explained and control techniques, for unity power factor operation and fast current control of the front end converter, in a rotating as well as a stationary reference frame, are discussed and compared. Results from computer simulations as well as experimental results, for a 1.5-kW prototype system using GE IGBT's Type 6E20, are presented.**

I. Introduction

HIGH switching frequency inverters are desirable for ac motor drives, as they permit the operation of the drive with practically sinusoidal stator current and fast current control for high dynamic performance. In addition the audible noises can be reduced at switching frequencies of the order of 20 kHz.

Until recently, power bipolar transistors and MOSFET's have been commonly used for inverters driving ac motors. As a third possible alternative, insulated-gate-bipolar-transistors (IGBT's) have emerged recently. IGBT's offer low on resistance and require very little gate drive power. A 1.5-kW prototype PWM inverter using GE IGBTs Type 6E20 is reported in this paper. A gate-drive circuit which provides fast turn-on and turn-off, and adequate protection against overload/shoot through faults is presented.

Switching aid networks (snubbers) are necessary to limit the stresses on the IGBTs at turn-on and turn-off. At high switching frequencies, the snubber losses become an appreciable portion of the output power, necessitating an energy recovery circuit to improve the efficiency. A simple and efficient energy recovery circuit which operates reliably at 20 kHz switching frequency is reported.

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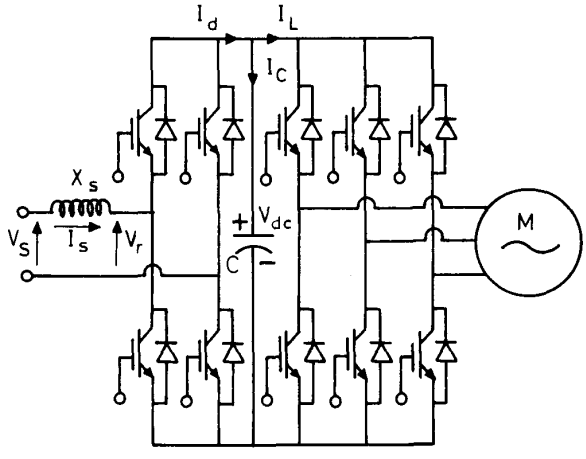

Fig. 1. IGBT PWM rectifier/inverter system.

The front-end converter feeding a PWM inverter, should, ideally, regulate the dc link voltage, draw sinusoidal current from the ac mains, without drawing reactive power, and should have bidirectional power flow capability. A PWM type front-end converter with an ac reactor at the ac input side meets all the requirements and has been used as a voltage source for PWM inverters driving ac motors [1]. Control techniques for three-phase PWM type front-end converters have been reported [2]–[4]. There are applications, including single-phase ac traction, where operation from a single-phase supply is of interest and techniques of control in this context have been reported [5], [6].

The ac motor drive system is shown in Fig. 1. The front-end for the system is a full-bridge IGBT PWM inverter with an ac reactor. The machine side converter is a high switching frequency IGBT three phase PWM inverter. The complete system operates from single-phase mains.

The steady-state design considerations are explained and the block diagrams of control in a rotating as well as a stationary reference frame of the single-phase PWM type front-end converter are developed. The complexities of control implementation for the two control techniques are studied and compared in this paper.

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II. 20-kHz IGBT Inverter

A. Gate-Drive Circuit

The IGBT combines some of the features of both bipolar-transistors and MOSFET's. It offers low saturation voltage and its voltage driven input, like that of a MOSFET, requires very little drive power. Its control terminals are the gate and emitter. The device turns-on when a voltage V_{GE} greater than gate-emitter threshold voltage V_{GEth} is applied between the gate and emitter. To turn-off the device a resistance R_{GE} must be connected between gate and emitter, which provides a discharge path for the gate-to-emitter capacitance. Unlike a MOSFET, the IGBT exhibits a long current fall time at turn-off. The fall time consists of two distinct intervals, one of which is constant and the other is a function of R_{GE}. The lower the value of R_{GE}, the smaller is the turn-off time. However, very low values of R_{GE} will result in high dv/dt at turn-off. This can, in turn, lead to the device latching 'ON' due to internal capacitive currents [7], unless a suitable dv/dt snubber is provided. For fast turn-on of the IGBT, a sharp rising pulse of voltage level well above V_{GEth} is to be applied between gate and emitter. Again, fast turn-on, while reducing the turn-on losses in the IGBT, can result in a large current spike due to the reverse recovery of the complementary feedback diode. A turn-on snubber is necessary to limit the diode reverse recovery current.

The gate-drive circuit developed for the IGBT is shown in Fig. 2. The speed-up capacitance C_p across R_{GS} provides a sharp rising edge while the device is turning-on. At turn-off the transistor Q_1 turns-on temporarily and brings down the gate-drive pulse sharply. The gate-to-emitter capacitance discharges through the transistor Q_1 and the device turns-off. The resistance R_{GE} improves the dv/dt capability of the IGBT in the off state.

The IGBT can latch to the ON state if the maximum controllable current is exceeded. The gate-drive circuit must therefore provide protection against overload/shoot through faults. The protection against overload/shoot through faults is provided by sensing the collector-emitter voltage through the diode D_1. In the gate-drive circuit of Fig. 2, the diode D_1 is forward biased, during the normal operation of the device, and the output of the comparator remains low. In the event of a fault V_{CE} increases and D_1 gets reverse biased. The output of the comparator goes high, if the potential at the positive input terminal (decided by $R_1 - R_2$ network) is greater than the threshold set at the negative input terminal. The transistor Q_2 turns-on and shuts off the gate-drive pulse. The device turns-off instantaneously. The opto-isolator gives out a trip-signal out of the isolated gate-drive circuit, which is used to diagnose the fault and take appropriate action in the controller. The protection is delayed to the extent of turn-on time of the device to avoid false tripping at turn-on.

B. Snubber and Energy Recovery Circuit

To achieve reliable switching and to reduce the switching losses in the IGBT's switching aid networks are necessary for limiting dv/dt and di/dt. The Undeland snubber [8] is used as it has fewer components and introduces lower additional stresses to the switching devices and freewheeling diodes. In addition it confines the losses to one resistor making energy recovery simpler. The basic switching aid network is shown in Fig. 3. The prototype 1.5-kW inverter is designed to operate from a 220-V dc bus, with a peak current of 20 A. The corresponding snubber component values are shown in Fig. 3.

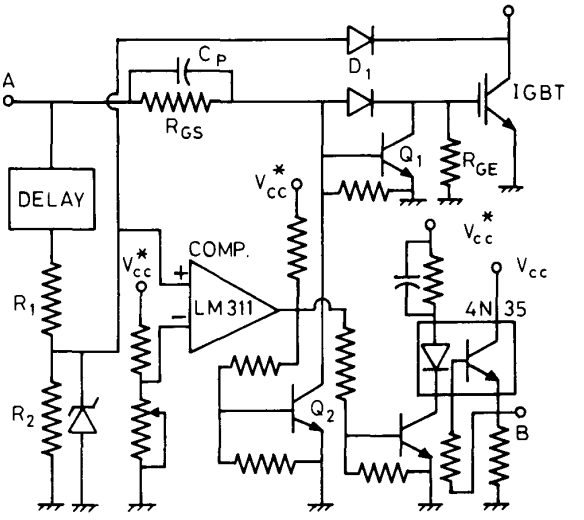

Fig. 2. Gate drive circuit for IGBT. A—Isolated gate pulse; B—trip signal. V_{cc}—common power supply. V_{cc}^*—isolated power supply.

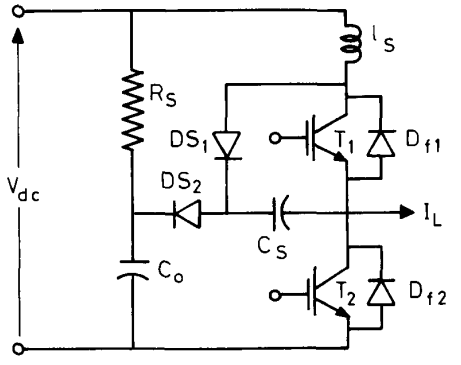

Fig. 3. Undeland snubber circuit. l_s = 15 μH; C_s = 0.1 μF; C_o = 0.47 μF.

At the end of each switching the snubber energy is transferred to l_s and is dissipated in R_s. The energy dissipation in R_s causes an overvoltage on the device that turns off.

The turn-on energy loss is given by

$$W_{on} = (1/2) l_s \Delta I_{max}^2 \tag{1}$$

where

$$\Delta I_{max}^2 = I_{rr}^2 + (C_s/l_s) V_{dc}^2 \tag{2}$$

I_{rr} reverse recovery current of the freewheeling diode in amps
V_{dc} dc bus voltage in volts.

The turn-off energy loss is given by

$$W_{off} = (1/2) l_s I_L^2, \quad (3)$$

where I_L-load current in amps.

The snubber losses, for the component values shown in Fig. 3, approximately turn out to be 96 W per leg at full load at 20-kHz switching frequency. The total power loss for the three-phase inverter, therefore becomes an appreciable portion (300 W) of the output power. Hence an energy recovery circuit is used. The snubber with the energy recovery circuit is shown in Fig. 4. The features of the recovery circuit used are as follows.

1) Uses fewer components, than the self oscillating push-pull type described in [9].
2) Problem of flux resetting in the recovery transformer is eliminated.
3) Operates reliably at 20-kHz switching frequency.
4) Recovery takes place automatically after each switching; no additional control is required.

The operation of the recovery circuit is as follows. At the end of each switching the excess energy in the inductor l_s has to be discharged. To start with some of this energy is transferred to C_o and the voltage across C_o rises above the dc bus voltage V_{dc}. When the voltage rise is sufficient to turn-on the MOSFET through the $R_1 - R_2$ network, the recovery transformer begins to conduct. The secondary winding N_s is clamped to the dc bus voltage V_{dc}, and therefore primary voltage gets clamped to $(N_p/N_s)V_{dc}$. This is also the voltage across l_s and therefore, the current in l_s drops at the rate of $[(N_p/N_s)V_{dc})]/l_s$. When the excess energy in the inductor is completely discharged the MOSFET turns off automatically. Any residual energy in the core is returned to the dc bus through the tertiary winding N_R. The overvoltage across the devices, during the recovery process is given by

$$\Delta V_o = (N_p/N_s)V_{dc} \quad (4)$$

where

N_p number of turns on the primary
N_s number of turns on the secondary
N_R number of turns on the tertiary.

A turns ratio (N_s/N_p) of 4 is used. Siemens Potcore Type No. B65696 T26 is used for the transformer.

C. Experimental Results

Fig. 5 shows the experimental current waveforms of the recovery circuit. Referring to Fig. 5, it is seen that the recovery process is not so pronounced at turn-off. This is because the load current is much less compared to the value of the excess current ΔI_{max} at the time of turn-on. The action of tertiary winding N_R, in resetting the transformer flux can also be clearly seen. From the device voltage waveforms in Fig. 6, it is seen that device voltage is

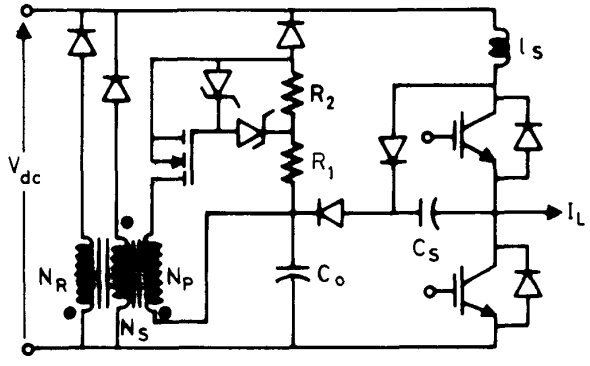

Fig. 4. Snubber with recovery circuit.

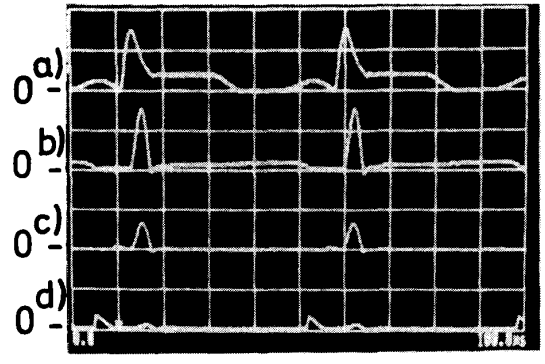

Fig. 5. Recovery circuit currents. Inductor 10 A/div; primary 7.5 A/div; secondary 4 A/div; tertiary 0.17 A/div; X: 10 μs/div.

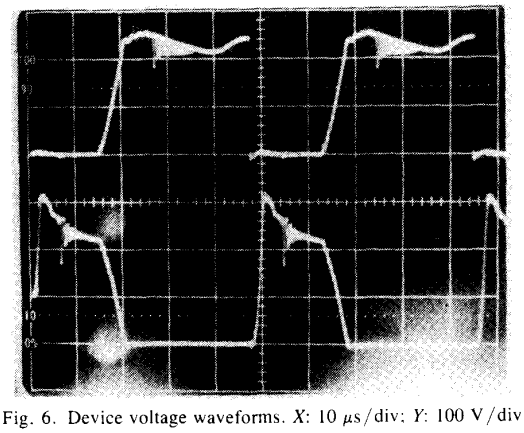

Fig. 6. Device voltage waveforms. X: 10 μs/div; Y: 100 V/div.

not clamped tightly to the value expected $(1 + N_p/N_s)V_{dc}$. This is because of the leakage inductance of the transformer. Also the capacitance C_o does not quite behave as a stiff voltage source. Therefore some additional oscillations are superimposed on the inductor current due to $l_s - C_o$ resonance.

It can also be seen from the inductor current waveform, that the overshoot ΔI_{max} at turn-on is less than the predicted value from (2). The reason is that the voltage across C_o tends to rise during the discharge of energy from C_s.

This brings the recovery transformer into conduction and part of the energy in C_s is transferred to the transformer leakage inductance. However, this energy along with the energy transferred to l_s is recovered through the recovery transformer. Measurement of the average values of the secondary and tertiary currents (using Yokogawa Analysing Recorder Model No. 3656) shows a total recovery of 54 W under the test conditions.

III. Regenerative Single-Phase Front-End Converter

A. Steady-State Design Considerations

The single-phase front-end converter shown in Fig. 1 consists of a full-bridge inverter using IBGTs, with an ac reactor at the ac input side. The inverter is operated in the PWM mode with sine-triangle modulation. The supply voltage V_s and the fundamental component V_r of the output voltage $v_r(t)$ at the ac terminals of the inverter are two sinusoidal voltages separated by a reactor. The power flow therefore depends on the phase angle displacement between the two voltage phasors. The phasor diagram is shown in Fig. 7.

Power transferred from the source to the converter ac terminals is given by

$$P_{SR} = (V_s V_r / X_s) \sin \delta \tag{5}$$

$$= V_s I_s \cos \phi \tag{6}$$

where

- V_s RMS value of the ac supply voltage (V)
- V_r RMS value of the fundamental component of the voltage generated at the ac terminal of the inverter (V)
- δ Phase-angle displacement between voltage phasors V_s and V_r
- X_s Reactance of the ac reactor at 50 Hz (Ω)
- ϕ Power factor angle.

If the dc link voltage V_{dc} is to remain constant then the input and output powers must be balanced.

From the phasor diagram of Fig. 7(a):

$$I_s \cos \phi = V_r \sin \delta / X_s \tag{7}$$

$$I_s \sin \phi = (V_s - V_r \cos \delta)/X_s. \tag{8}$$

If the reactive power drawn from the mains is to be zero, then the power factor must be unity. Hence from (7) and (8):

$$I_s X_s = V_r \sin \delta \tag{9}$$

$$V_s = V_r \cos \delta. \tag{10}$$

The phasor diagrams at unity power-factor operation for forward and reverse power flow are shown in Fig. 7(b) and (c), respectively. From (9) and (10):

$$V_r = \sqrt{V_s^2 + (I_s X_s)^2}. \tag{11}$$

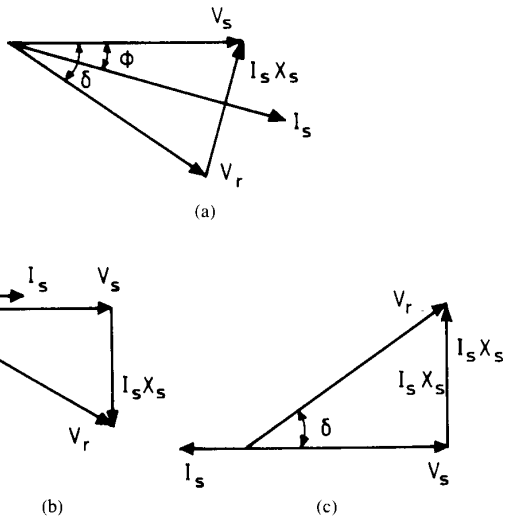

Fig. 7. Phasor diagrams of front-end converter. (a) Lagging power factor. (b) UPF forward power flow. (c) UPF reverse power flow.

Under full-load conditions

$$V_{rFL} = V_s \sqrt{1 + X_{pu}^2} \tag{12}$$

where

$$X_{pu} = (I_{sFL} X_s)/V_s \tag{13}$$

I_{SFL} full load rms ac current assuming unity power-factor (A).

Equation (12) implies that V_R is greater than V_s by a factor $\sqrt{1 + X_{pu}^2}$ known as the boost factor.

B. Design Considerations

The dc link voltage is decided by the line-to-line voltage rating of the motor. The dc link voltage together with the full-load power decides the voltage and current ratings of the power devices to be used. From the previous discussion the magnitude of V_r varies between a minimum of V_s to a maximum of $V_s\sqrt{1 + X_{pu}^2}$. This maximum value of V_r is decided by the maximum value of the phase separation δ which occurs under full load condition.

For a selected power device the minimum pulse or notch width that can be reliably reproduced in the inverter is decided by the device switching speeds and snubber relaxation times. The control technique adapted requires that the inverter always operate in full modulation, i.e., with modulation index (m) less than or equal to one where m is defined by

m = Amplitude of sine reference/Amplitude of triangular carrier. The minimum value of m is decided by the fact that the minimum value of V_r is equal to V_s,

$$\text{i.e., } m_{min} = V_s/(V_{dc}/\sqrt{2}). \tag{14}$$

It is desirable that, the reactor value is selected in such a way that, the maximum modulation index at which the inverter operates is as close to one as is permitted by the

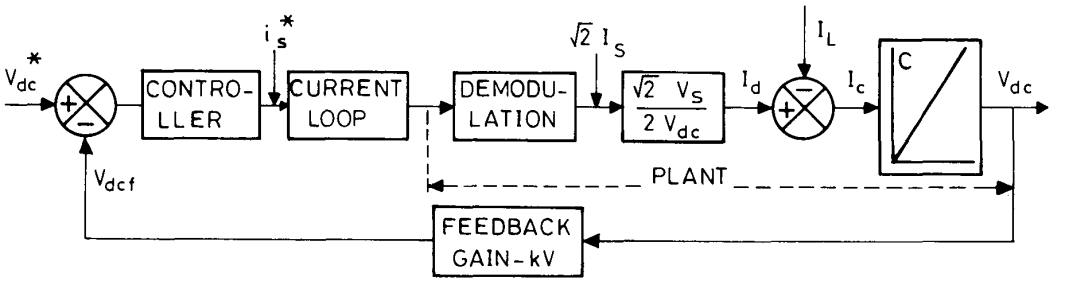

Fig. 8. Block diagram for dc voltage regulation.

minimum pulse or notch width capability of the device. This is because under this condition the magnitude of V_r varies over a wide range making the control less sensitive to the errors in the controller gains, compensations, etc. If a very low value of inductance is used the range of variation of V_r becomes very much limited and the control becomes very sensitive to the above errors. Moreover the switching frequency has to be increased for a smaller reactor size in order to limit the current ripple. For a given minimum pulse or notch width the switching frequencies can only be increased upto the point where the minimum modulation index condition given by (14) is not violated.

Hence for a selected switching device the switching frequency should be selected so as to obtain a modulation index (m) close to one, under full load condition. With this maximum value of m, the corresponding values of V_{rFL} and hence X_{pu} can be calculated from (12). The size of C is decided by the amount of ripple voltage and current allowed at the dc link.

C. Dynamic Control

The control philosophy is to regulate the dc link voltage, by matching the input power to the converter with the power demanded from the dc link, while maintaining the power-factor at unity for either direction of power flow. That is,

$$V_s I_s = V_{dc} I_d \tag{15}$$

i.e.,

$$(\sqrt{2}V_s \sqrt{2}I_s)/2 = V_{dc} I_d \tag{16}$$

or

$$I_d = (\sqrt{2}V_s / 2V_{dc})(\sqrt{2}I_s). \tag{17}$$

Therefore the amplitude of the ac input current must be controlled to balance the input and output powers of the converter, and it should be maintained in phase with V_s. The voltage regulation scheme can therefore be represented as shown in Fig. 8. The scheme consists of a fast inner current loop and an outer voltage loop.

The current loop of Fig. 8, can be realized by hysteresis current control of the PWM inverter [10]. However, the switching frequency is not constant in hysteresis control. Therefore the current harmonics injected into ac line are also not at fixed frequencies and cannot be filtered effectively. On the other hand, if the PWM inverter is operated as a voltage source inverter with sine-triangle modulation, the harmonics of the ac voltage and consequently the ac current occur at well defined frequencies. Therefore, filters can be designed to suppress the ac current harmonics. In case of high power drives the inverter can be split into several parts and harmonics can be canceled out between part inverters by phase shifting the carrier waveforms [11]. This realization has led to the investigation of voltage source operation for the front-end converter with sine-triangle modulation [2], [12]. In general, current control of voltage source inverters can be accomplished either in a rotating or a stationary reference frame [13]. Control in a stationary reference frame leads to ac control loops, with inevitable phase errors between inputs and outputs. In variable frequency application such as ac motor drives, the phase errors change with frequency and are therefore difficult to compensate. Therefore, control in a rotating reference frame, resulting in dc control loops, is preferred in such applications. For inverters operating from fixed frequency three-phase mains, there is no significant difference in the complexity of implementation between the two techniques [4]. However, control in stationary coordinates with correction for the phase-lag produced by the control loop seems to have been favored [2], [4].

The present work is focused on single-phase systems. This is because for low power drives, the input is more likely to be single phase. Many UPS systems also operate from a single phase supply and a single-phase front-end converter can be used [14]. Another important application for single-phase systems is that of ac traction.

In the following sections the current control of the single-phase voltage source PWM inverter is studied in a rotating as well as a stationary reference frame. The block diagrams of the control system are developed.

D. Control in Rotating (d-q) Reference Frame

The usual advantage cited for the use of rotating reference frame control is that the control loops work on dc quantities and the bandwidth requirements on the controllers are less demanding. However, all feedback quantities have to be translated into the rotating reference frame. In the present case, this implies isolating the direct (or active) component $i_{sd}(t)$ and the quadrature (or reactive) component $i_{sq}(t)$ of the ac current $i_s(t)$. The model-

ling of the system, for the d-q reference frame of control is carried out as follows. The instantaneous values of supply voltage v_s, supply current i_s and the average value of the converter ac terminal voltage, v_r, can be expressed as

$$v_s(t) = \sqrt{2}V_s \sin \omega_s t \tag{18}$$

$$i_s(t) = i_{sd}(t) \sin \omega_s t + i_{sq}(t) \cos \omega_s t \tag{19}$$

$$v_r(t) = v_{rd}(t) \sin \omega_s t + v_{rq}(t) \cos \omega_s t \tag{20}$$

where the subscript 'd' denotes the quantities in phase with V_s and 'q' denotes the quantities in quadrature with V_s.

The voltage equation for the single phase system is given by

$$v_s(t) = L_s \frac{di_s(t)}{dt} + v_r(t) \tag{21}$$

Substituting (18)–(20) into (21) and collecting sin ωt and cos ωt terms separately the following equations for the currents can be obtained.

$$L_s \frac{di_{sd}(t)}{dt} = \sqrt{2}V_s + \omega_s L_s i_{sq}(t) - v_{rd}(t) \tag{22}$$

$$L_s \frac{di_{sq}(t)}{dt} = -\omega_s L_s i_{sd}(t) - v_{rq}(t). \tag{23}$$

Considering (22), the plant for current loop can be represented as shown in Fig. 9 for the d axis. A similar diagram can be drawn for the q axis, by considering (23).

If the desired response of the current loop is a first-order lag of T, then the dynamics of the current loops can be described by

$$T \frac{di_{sd}(t)}{dt} + i_{sd}(t) = \frac{i^*_{sd}(t)}{K_i} \tag{24}$$

$$T \frac{di_{sq}(t)}{dt} + i_{sq}(t) = \frac{i^*_{sq}(t)}{K_i} \tag{25}$$

where

- T lag of the converter corresponding to the switching frequency
- K_i current feedback gain

superscript * denotes the control signals for the reference values.

Comparing (22) and (24) the control law for $v^*_{rd}(t)$ can be written as

$$v^*_{rd}(t) = \frac{\sqrt{2}V_s}{G} + \frac{\omega_s L_s (K_i i_{sq}(t))}{GK_i} - \frac{L_s}{T}\frac{1}{GK_i}[i^*_{sd}(t) - K_i i_{sd}(t)]. \tag{26}$$

Similarly comparing (23) and (25) the control law for $v^*_{rq}(t)$ is written as

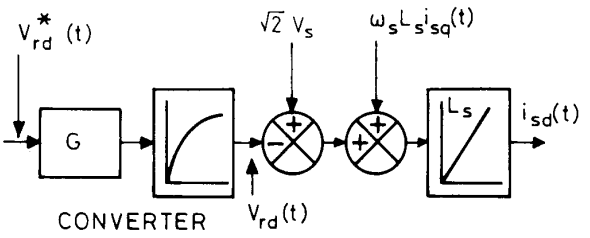

Fig. 9. Control plant for d-Axis current loop.

$$v^*_{rq}(t) = \frac{-\omega_s L_s (K_i i_{sd}(t))}{GK_i} - \frac{L_s}{T}\frac{1}{GK_i}[i^*_{sq}(t) - K_i i_{sq}(t)]. \tag{27}$$

The block diagram of the control scheme for the d axis according to (22) and (26) is shown in Fig. 10. An outer voltage control loop is provided to regulate the dc link voltage. The instantaneous value of the dc link voltage is compared with a reference, and the error after passing through a controller, is used as the reference signal for the d axis current. The feedforward load compensation is used, so that the system can be stabilized with a simple P controller for the voltage loop. The gain of the P controller is calculated, using classical linear control system theory.

The control scheme for the q axis is similar except that the reference for q axis current is fixed at zero, since for unity power factor operation the q axis current must be forced to zero.

As seen from the block diagram of Fig. 10, the control scheme requires the d- and q-axis components of the ac current as feedback signals. These components of the current are calculated as follows:

Multiplying (19) by sin $\omega_s t$

$$i_s(t) \sin \omega_s t = i_{sd}(t) \sin^2 \omega_s t + i_{sq}(t) \cos \omega_s t \sin \omega_s t = \frac{i_{sd}(t)}{2} - \frac{i_{sd}(t)}{2} \cos 2\omega_s t + \frac{i_{sq}(t)}{2} \sin 2\omega_s t. \tag{28}$$

Multiplying (19) by cos $\omega_s t$

$$i_s(t) \cos \omega_s t = i_{sd}(t) \sin \omega_s t \cos \omega_s t + i_{sq}(t) \cos^2 \omega_s t = \frac{i_{sd}(t)}{2} \sin 2\omega_s t + \frac{i_{sq}(t)}{2} + \frac{i_{sq}(t)}{2} \cos 2\omega_s t. \tag{29}$$

If the double-frequency components present in (28) and (29) are filtered, then $i_{sd}(t)$ and $i_{sq}(t)$ can be obtained. The calculation of $i_{sd}(t)$ and $i_{sq}(t)$ is shown in the block diagram of Fig. 11.

To eliminate the double-frequency components, it would appear that a simple low pass filter would be sufficient. However, with the introduction of low pass filters, the response of the current loops gets limited by the cor-

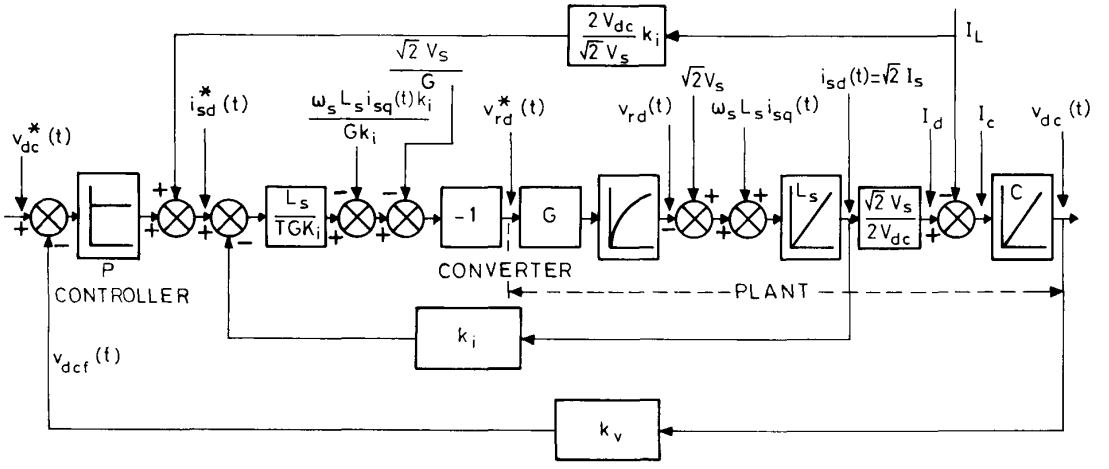

Fig. 10. Block diagram of voltage regulation scheme showing current loop in d-axis.

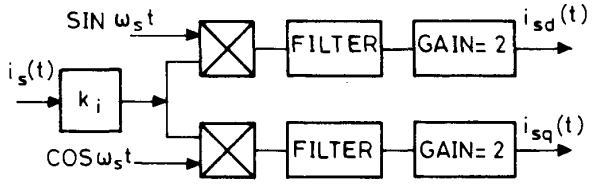

Fig. 11. Block diagram for calculation of i_{sd} and i_{sq}.

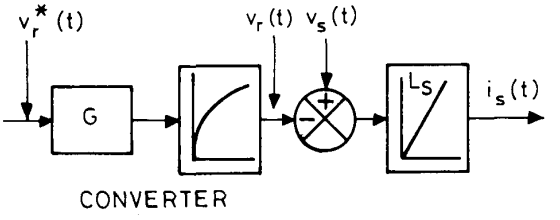

Fig. 12. Control plant for current control in stationary coordinates.

ner frequency of the filters, rather than the lag of the converter as assumed in (24) and (25). It was found through computer simulation that only a notch filter designed to eliminate the double frequency components gave satisfactory results.

E. Control in Stationary Reference Frame

In a stationary reference frame of control the inner current loop will be working with ac quantities, while the outer voltage control loop will be working with dc quantities. The modeling of the system is carried out as follows. The voltage equation (21) can be written as

$$L_s \frac{di_s(t)}{dt} = v_s(t) - v_r(t). \tag{30}$$

According to (30) the plant for the current loop can be represented as shown in Fig. 12.

As before, if the desired response of the current loop is a first order lag of T, then the dynamics of the current loop can be described by

$$T\frac{di_s(t)}{dt} + i_s(t) = \frac{i_s^*(t)}{K_i}. \tag{31}$$

The reference $i_s^*(t)$ is sinusoidal and hence the response $i_s(t)$ will also be sinusoidal with a phase lag of arc tan ωT. This phase lag can be compensated for by introducing a corresponding phase lead for the current reference $i_s^*(t)$. Comparing (30) and (31) the control law for $v_r^*(t)$ is written as

$$v_r^*(t) = \frac{v_s(t)}{G} - \frac{L_s}{T}\frac{1}{GK_i}[i_s^*(t) - K_i i_s(t)]. \tag{32}$$

The block diagram of the control scheme, in a stationary reference frame, according to (30) and (32) is shown in Fig. 13. This scheme also consists of an outer voltage control loop with a P controller and feedforward compensation for the load current. The current reference is given a phase lead, to account for the phase lag introduced by the loop. The gain of the P controller is calculated using classical linear control system theory.

F. Computer Simulation

The simulation results of the front-end converter are obtained using the simulation software TUTSIM [15]. The switching process of the front-end converter with sine-triangle modulation is represented in the simulation. Figs. 14 and 15 show the simulated results for the rotating reference frame control and the stationary reference frame control respectively. The results show that there are no significant differences between the two techniques of control described above, as far as the performance of the converter is concerned. Hence considering the difficulties in obtaining the d- and q-axis components of ac current as feedback signals in a rotating reference frame control, the stationary reference frame control is easier to implement. The phase error introduced by the control loop can be eas-

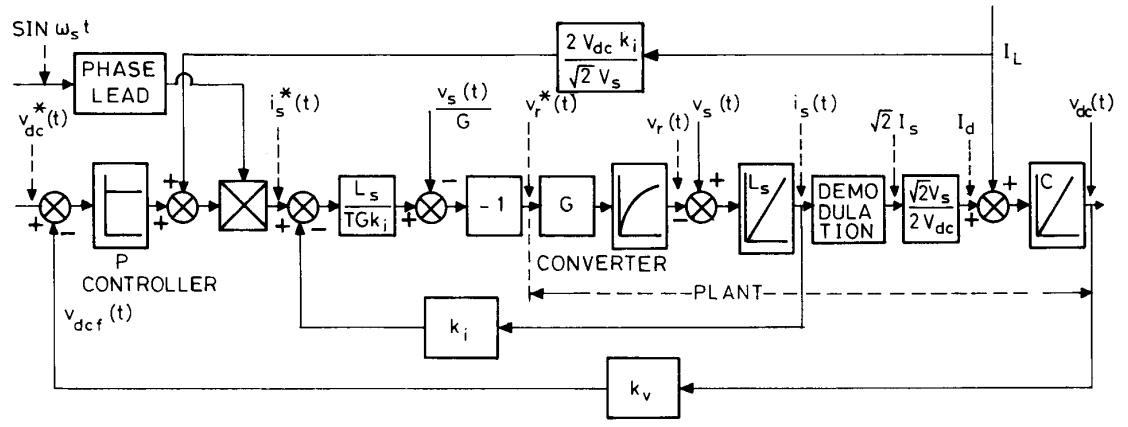

Fig. 13. Block diagram of voltage regulation scheme with current control in stationary coordinates.

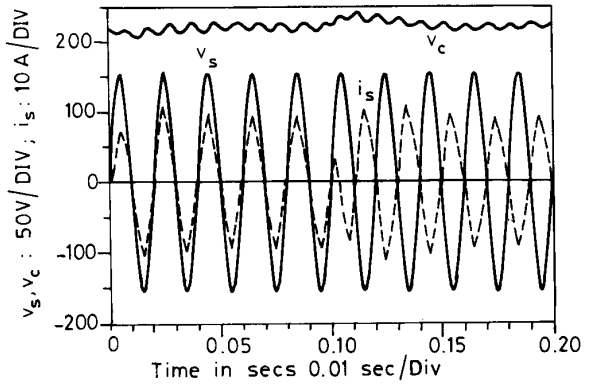

Fig. 14. Simulated waveforms for d-q reference frame control. Step reversal of load at 0.1 s.

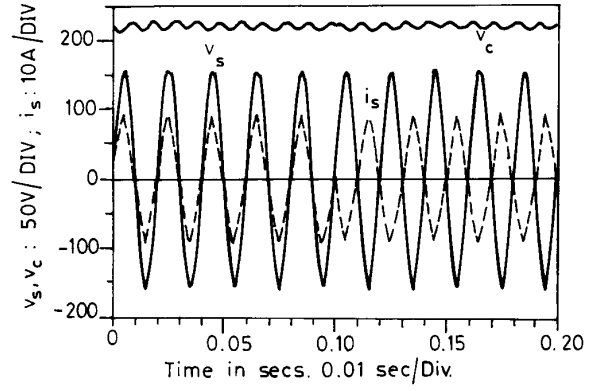

Fig. 15. Simulated waveforms for stationary reference frame control. Step reversal of load at 0.1 s.

ily compensated for as the front-end converter operates from a fixed frequency ac voltage source.

G. Experimental Results

A prototype 1.5-kW laboratory model of the front-end converter is made using GE IBGT Type 6E20. The ac current is sensed by a simple inexpensive current sensor.

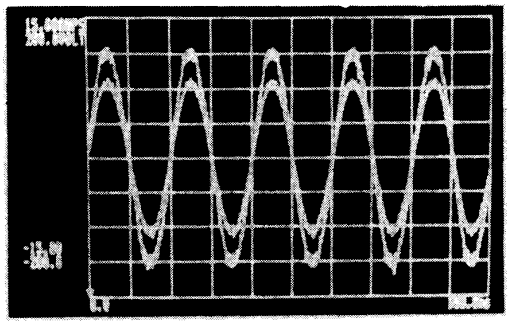

Fig. 16. AC voltage and current—forward power flow. X: 10 ms/div.; Y_1: 50 V/div.; Y_2: 3.75 A/div.

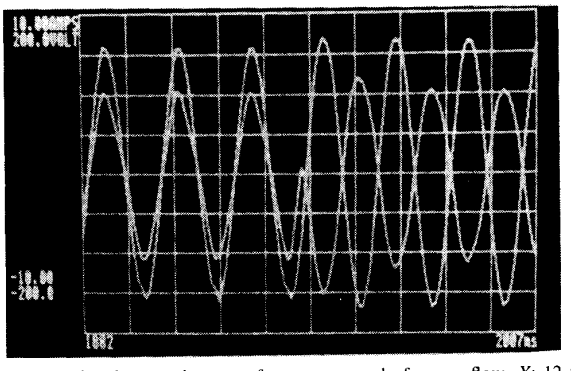

Fig. 17. AC voltage and current for step reversal of power flow. X: 12.5 ms/div., Y_1: 50 V/div., Y_2: 2.5 A/div.

The dc load current for feedforward compensation, is sensed by a Hall-effect current transducer. The reference sine wave is obtained through a potential transformer connected across the ac supply terminals. The control scheme is as shown in Fig. 13. The converter is operated with sine-triangle modulation with a carrier frequency of 1 kHz. The gains in the controller are adjusted for a nominal ac supply voltage of 110 V (rms) and a dc link voltage of 220 V and the proportional gain is adjusted to 5.

To start with, the dc link capacitor is charged through the diodes of the front-end converter itself with the gating

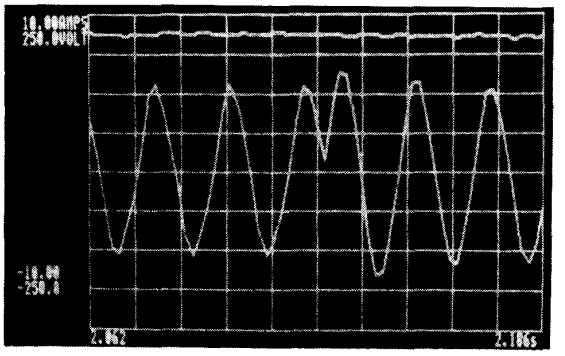

Fig. 18. DC link voltage and ac current for step reversal of power flow. X: 12.5 ms/div., Y_1: 62.5 V/div.; Y_2: 2.5 A/div.

pulses to the IGBT's being blocked. When the gate pulses are released, the dc link voltage builds upto the reference value set by the voltage control loop.

Fig. 16 shows the experimental waveforms of ac supply voltage and current at 45% of full load for forward power flow. It is seen that the ac current is nearly sinusoidal at unity power factor.

Fig. 17 shows the transient waveforms for a step change of load current from one direction to the other. The system responds as expected, and has a high dynamic performance. Fig. 18 shows that there is practically no change in the dc link voltage even when the load current changes from one direction to the other, in step fashion.

IV. Conclusion

An inverter/converter system operating from a single-phase supply has been described. The power device used in the system is the IGBT. The inverter can operate at switching frequencies up to 20 kHz. Snubber circuits along with energy recovery networks suitable for high frequency operation have been described and experimental results from a laboratory inverter have been presented.

The steady-state design considerations of the front-end converter have been discussed. The block diagrams for dynamic control in a rotating as well as a stationary reference frame have been developed. Experimental results from a laboratory converter with stationary reference frame control have been presented in support of the analysis.

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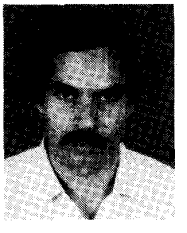

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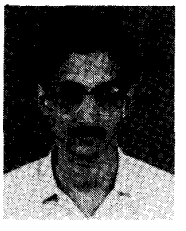

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