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APPLICATION OF ZnO VARISTOR PROTECTION TO CAPACITORS OF ARTIFICIALLY COMMUTATED INVERTER IN MTDC SYSTEM

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ABSTRACT

The dynamic analysis of a mesh type multiterminal HVDC (MTDC) transmission system including an artificially commutated inverter (ACI) with varistor protected series capacitors is carried out using digital simulation technique. The study shows that the varistor protection is feasible and improves the performance of normal rated inverters which connect weak ac systems. It reduces the magnitude of dynamic overvoltage and the peak direct current at the ACI during abnormal conditions resulting in a significantly improved dynamic performance of the MTDC system.

KEY WORDS

dc transmission, digital simulation, artificial commutation, transients, Zinc oxide varistor.

INTRODUCTION

The study of multiterminal HVDC (MTDC) transmission systems involving inversion into weak ac systems has been considered by several authors [1,2,3]. The inversion into weak ac system poses problems regarding ac voltage regulation and stability, dynamic performance, commutation during abnormal conditions, reactive power compensation and low order harmonics. A discussion on these problems and details of specific case histories of five dc projects are available in Ref. [4]. In each of these projects different remedial measures are implemented to achieve good performance of the interconnections inspite of the low short circuit ratio (SCR) of the concerned ac systems. These measures, in general, use advanced controls and/or additional devices like synchronous condensers, SVS, etc., making the system more complex and costly.

Artificial (forced) commutation forms a possible alternative solution to overcome the above problems. Different techniques of artificial commutation have been studied earlier [5,6,7,8]. In particular, the series capacitor commutated circuit has received much attention [9,10,11,12]. Although various properties such as steady state operation, valve stresses, converter faults, inversion into dead load, etc. have been investigated, there are many open questions that still need to be resolved. Some of the questions pertain to the dc harmonics, evaluation of the capacitor and its protection from overvoltages. The capacitor overvoltages not only increase the cost of insulation but also have severe effect on the dynamic performance of the artificially commutated inverter (ACI). In the present work, artificial commutation using series capacitors is used for inversion into a weak ac system. Further it is proposed to protect the series capacitors using ZnO varistor. The feasibility of this protection is verified from the performance analysis of an ACI, using a digital simulation technique.

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EVALUATION OF THE CAPACITOR

For inverting into weak ac systems, artificial commutation using series capacitors constitutes an attractive technique. This is because, the capacitors supply the reactive power consumed by the converter and increase the strength of the ac system by decreasing the overall ac system impedance. The capacitor voltage shifts the resultant commutating voltage from the ac source voltage. This helps in faster commutation and enables the operation of the converter over a wider range of firing angles than is possible with natural commutated converter (NCC). The magnitude of the commutating voltage shift depends upon the value of the capacitor chosen. The stability of operation improves for larger values of the phase shift. A smaller value of the capacitor gives a larger phase shift. However, with low capacitor value the voltage across the capacitor will be very high. In the present study, to evaluate the minimal value of the capacitor, it is proposed to carry out a parametric study over a reasonable range of 'C'. For this purpose, the earlier works of Vithayathil [9] and Neiman et al [10] are used as guidelines. Vithayathil has analysed the steady state performance of the 6P artificially commutated converter (ACC). Neiman et al have outlined a procedure to study 6P and 12P converters in steady state. Both the above studies involve parametric evaluation for a general system. In Ref. [10], it is also shown that the limiting values of overlap angle and firing angle are given by

$$U_{lim} = \pi - \pi\sqrt{1 - (6/\pi^2)\, x_s wC} \qquad (1a)$$

For rectifier,

$$\alpha_{lim} = -(U_{lim}/2) \qquad (1b)$$

For inverter,

$$\alpha_{lim} = 180 - (U_{lim}/2) \qquad (1c)$$

By appropriately choosing U_{lim}, equation (1a) can be used to find the value of capacitor. Thus for x_s = 28.0 ohm and U_{lim} lying between 12^o and 18^o, the capacitor value ranges from 25 μ F to 35 μ F. Accordingly, the present authors have numerically evaluated the dynamic performance of the ACI in MTDC system, for C = 25, 28, 30, 32, 35 μF and based on this study a value of C = 30 μF has been found to give satisfactory performance. This corresponds to U_{lim}=15^o α_{lim} = 173^o. The details of this parametric study are reported in Ref. [13].

APPLICATION OF ACI IN MTDC SYSTEM

In this analysis, four independent ac systems feed a mesh connected dc network. Each converter is rated for 500 MW. The details of the system are shown in Fig. 1. The two rectifiers and the inverter 1 are connected to strong ac systems. Inverter 2 feeds into a weak ac system with SCR = 2.0. When this inverter is natural commutated, even for a small disturbance in the ac system voltage there will be repeated commutation failures indicating difficult recovery of the system. In the present study interest is focused on the application of ACI to the normal rated inverter 2. The series capacitors are connected in each phase, on the valve side of the transformers.

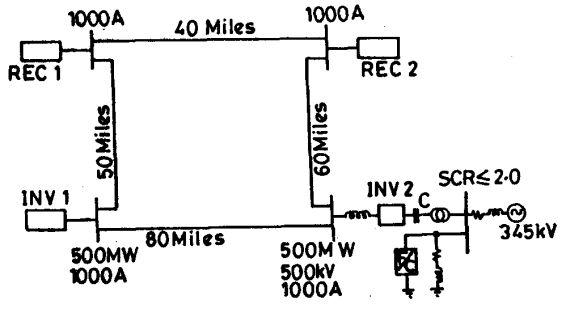

FIG.1 SINGLE LINE DIAGRAM OF THE MTDC TEST SYSTEM.

Each terminal is provided with ac filters. Eventhough the inverter 2 rating is not very high, the increased reactive power consumption because of high ac impedance, increases low order harmonics. This necessitates the provision of low order harmonic filters. At present, the effect of dc filters and transformer saturation are not taken into account.

The control strategy consists of current margin method. One of the terminal controls the voltage while the other three are in current control. The current margin ΔI is assigned to inverter 2 which is in minimum extinction angle control. The current controllers use conventional PI control.

ANALYSIS OF THE MTDC SYSTEM

The dynamic analysis of the above system is carried out by means of digital simulation technique. The complete system is subdivided into different modules. Thus, there is an ac module at each terminal and a dc module. The ac module consists of the ac source, converter transformer, ac filters [5th, 7th, 11th, 13th and HP), reactive power compensating equipment, static load, and a 12P converter. The dc module includes dc lines and a smoothing reactor. The numerical solution consists of solving the equations for ac module and dc module separately at every time step and interfacing the two solutions appropriately. The details of this analysis are available in Ref. [13]. The converter model [14] used in this analysis enables easy incorporation of series capacitors into the analysis.

PROTECTION OF SERIES CAPACITORS

The series capacitors for artificial commutation carry the full load current. During the ac system fault, the dc current and hence the current through the capacitors increases to a high value charging them to a voltage of about 5 to 7 times the normal value. Thus, to limit the capacitor voltage to an acceptable level of 2.0 to 2.5 times the capacitor peak voltage, it is necessary to provide suitable protection to the series capacitors. The zinc oxide varistor which can withstand continuous ac voltage stress without significant deterioration [15] is considered to be well suited for this purpose. The VI characteristics of the varistor is

$$V = KI^{\beta} \qquad (2)$$

The voltage and energy are the primary considerations in the design of varistors. The voltage rating and the related VI characteristics are established by the capacitor value and the maximum normal voltages anticipated across the capacitors. The energy rating is found for a given capacitor value and protective voltage level, from the disturbance criteria that cause the worst case energy. For a capacitor value of 30 μF, the varistor specifications are as follows.

Rated capacitor current	Id = 1000A
Maximum capacitor voltage/phase	MCV = 110 kV
Maximum continuous operating voltage	MCOV = 120 kV
Protective level of varistor	PLV = 2.5 * MCOV

These specifications give a value of K = 2.2781 and β = 0.04975 in equation (2).

SIMULATION OF ZnO VARISTOR

The zinc oxide varistor protective system consists of the varistor, air gap, a bypass switch and a discharge reactor as shown in Fig. 2 and is placed directly across the capacitor. In the simulation, the air gap and the bypass switch are modelled as ideal switches that are closed when the varistor conducts and open when varistor is not conducting. The effect of varistor protection is easily included in the numerical work through the characteristic given in equation (2). At every time step, knowing the value of the voltage across capacitor, the unknown current I through the varistor is computed using the above equation. In this computation, it may be noted that the varistor being purely resistive, carries positive current when the voltage is positive and negative current when voltage is negative.

RESULTS AND DISCUSSION

The performance of the varistor protective scheme for the series capacitors is studied from the functioning of the ACI during the following transient conditions:

1. balanced ac bus fault at inverter 2
2. unbalanced ac bus fault at inverter 2
3. dc line fault.

Balanced ac bus fault at inverter 2

Figures 3 and 4 show the various performance curves for a three cycle, balanced three phase to ground fault, without and with varistor protection for ACI. The fault is initiated at 0.005 sec and is simulated by shorting the static load at inverter 2 bus. The improved performance of the ACI due to varistor protection can be observed in these figures. During the fault, the varistor clips the capacitor voltage to 2.5 times its normal peak value. Accordingly the dc current reduces from 7.0 p.u. to 3.3 p.u. with varistor. It is seen that the dc voltage remains at an average value of 0.7 p.u. during the fault. This is because of the almost constant dc

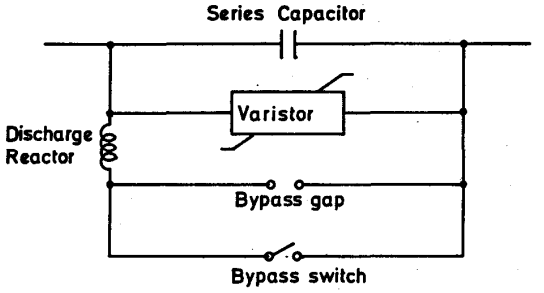

Fig. 2 Circuit of varistor protected capacitor

current, during this period. During recovery, the ac bus voltage is distorted significantly for the case without varistor, with the peak reaching a value as high as 2.3 times the normal value. Bus voltage with varistor has a remarkable improvement, with a voltage peak of 1.6 times the normal. It is also observed that the rectifier dc currents are reduced drastically. In either cases, the increased capacitor voltage gives a larger margin for commutation thus avoiding the occurrence of commutation failures.

The varistor conducts alternately during the transient with a peak current of 3.0 p.u. (3 kA) and absorbs an energy of 10.2 MJ. This gives a value of 33.2 kJ/kV and is comparable to the value used in practice albeit in a different context [15].

Unbalanced ac bus fault at inverter 2

From the performance curves of Fig. 5, single phase to ground fault at the ac bus of inverter 2, with varistor is seen to be less severe than the corresponding three phase fault. The varistor carries a peak current of 2.0 p.u. absorbing 2.65 MJ of energy.

DC line fault at inverter 2

The dc line fault is simulated by setting the line side dc voltage to zero over a duration of 20 msec. The fault is initiated at 0.1 sec and is detected at 0.012 sec. After the detection of the fault the rectifiers are delay fired at 110^{o} and the inverters are made to operate at minimum firing angles of 120^{o}. The fault current at the rectifiers reach a peak of 3.6 p.u. while the inverter 1 is starved of current for nearly 5 cycles. After de-energization of the dc system, the restart signal is delayed for 40 msec to allow for deionization. During the restart, the rectifiers are allowed to recover naturally. The inverter 1 alpha order is ramped to the normal value while inverter 2 recovers according to minimum extinction angle control. The effect of varistor is not felt during the fault and the system recovers smoothly without undue disturbances.

In all the three cases discussed above, it is observed that the conventional control strategies used are adequate to attain a satisfactory performance of the system.

CONCLUSION

The dynamic analysis of ACI in an MTDC system with zinc oxide varistor protection for capacitors has been studied using a modular digital simulation technique. The performance has been investigated for a few representative class of transient conditions. In these cases, it is observed that the protection provided limits the capacitor voltage and improves the performance of the ACI and the overall system. The numerical results obtained, points towards the usefulness of artificial commutation for inversion into weak ac systems and highlights the advantages of using varistor protection for the capacitors.

NOMENCLATURE

VD1	valve side dc voltage at rectifier	1
VD2	valve side dc voltage at rectifier	2
VD3	valve side dc voltage at inverter	1
VD4	valve side dc voltage at inverter	2
V5	line side dc voltage at rectifier	1
V6	line side dc voltage at rectifier	2
V7	line side dc voltage at inverter	1
V8	line side dc voltage at inverter	2
ID1	terminal dc current at rectifier	1
ID2	terminal dc current at rectifier	2
ID3	terminal dc current at inverter	1
ID4	terminal dc current at inverter	2
VB4	ac bus voltage at inverter	2
VC	capacitor voltage at inverter	2
EN	varistor energy	
IAR	varistor current	
xs	equivalent ac system impedance at inverter 2	
C	series capacitance	
U	overlap angle	
α	firing angle	

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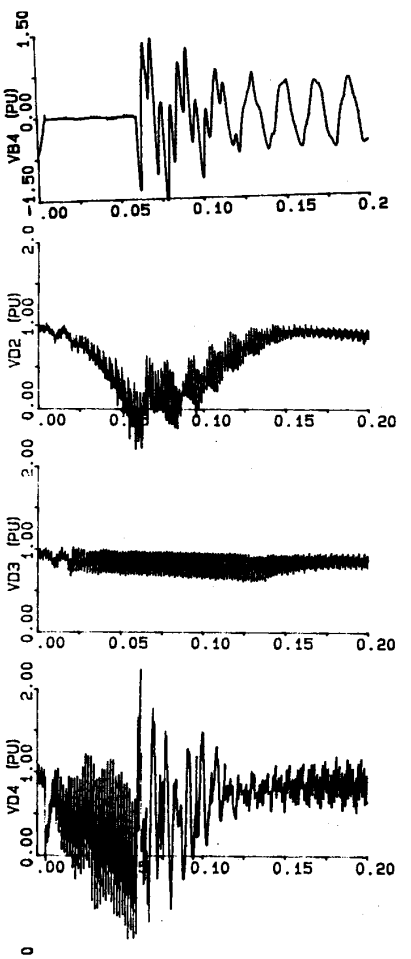


Fig. 3 Balanced ac fault at inv. 2 - Without varistor

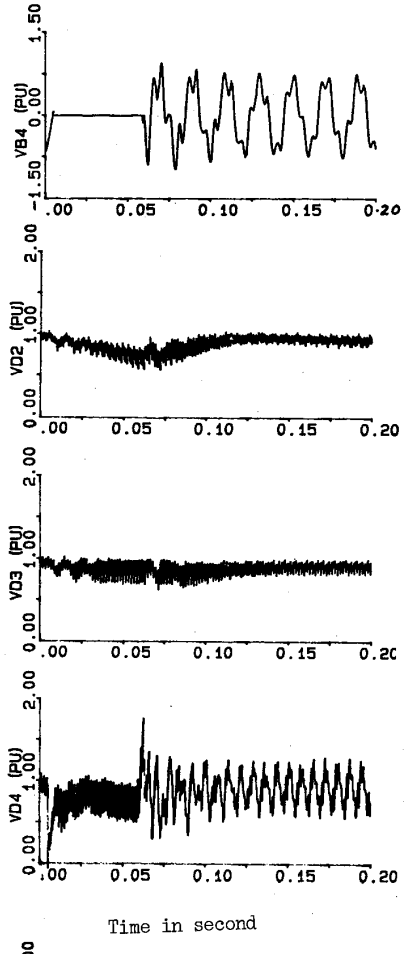


Fig. 4a Balanced ac fault at inv. 2 - With varistor

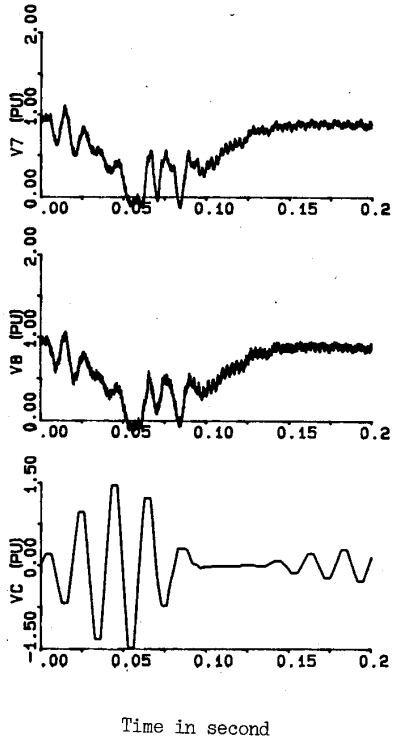


Fig. 3a Balanced ac fault at inv. 2 - Without varistor

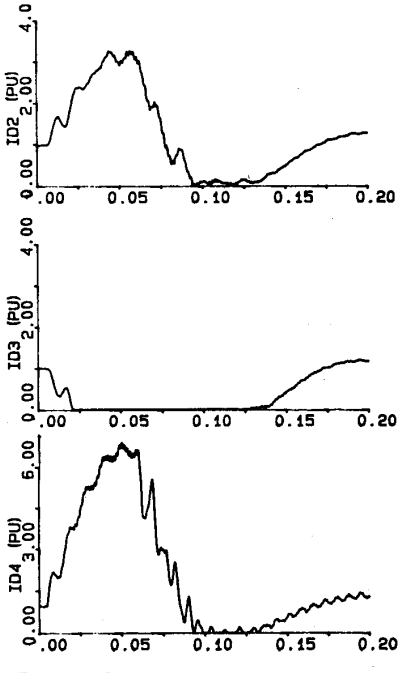


Fig. 3 Balanced ac fault at inv. 2 - Without varistor

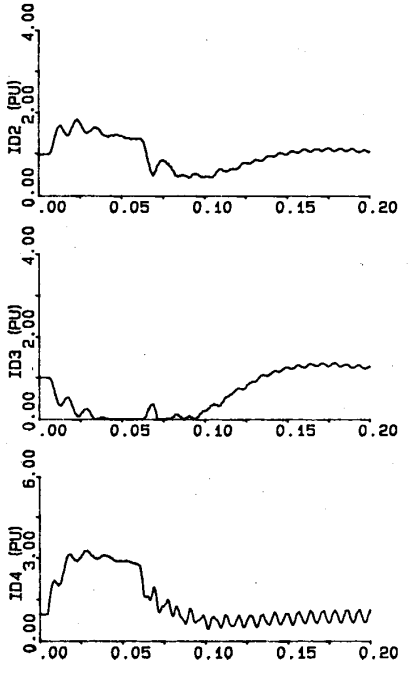


Fig. 4a Balanced ac fault at inv. 2 - With varistor

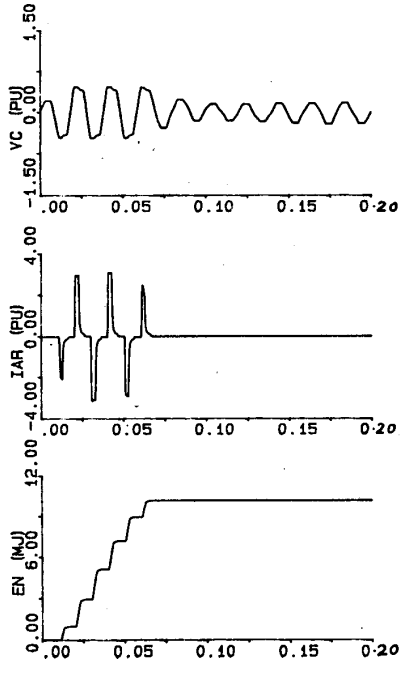
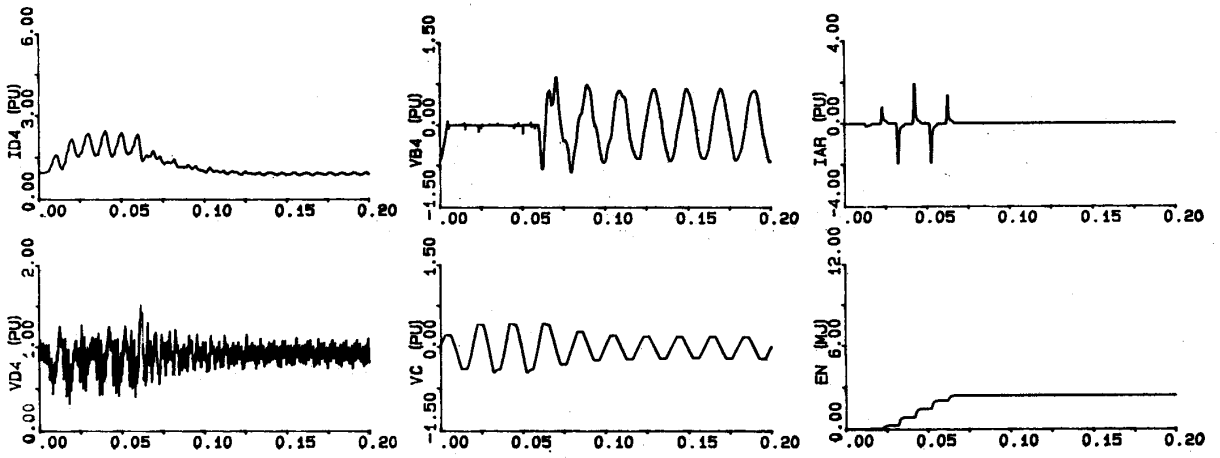
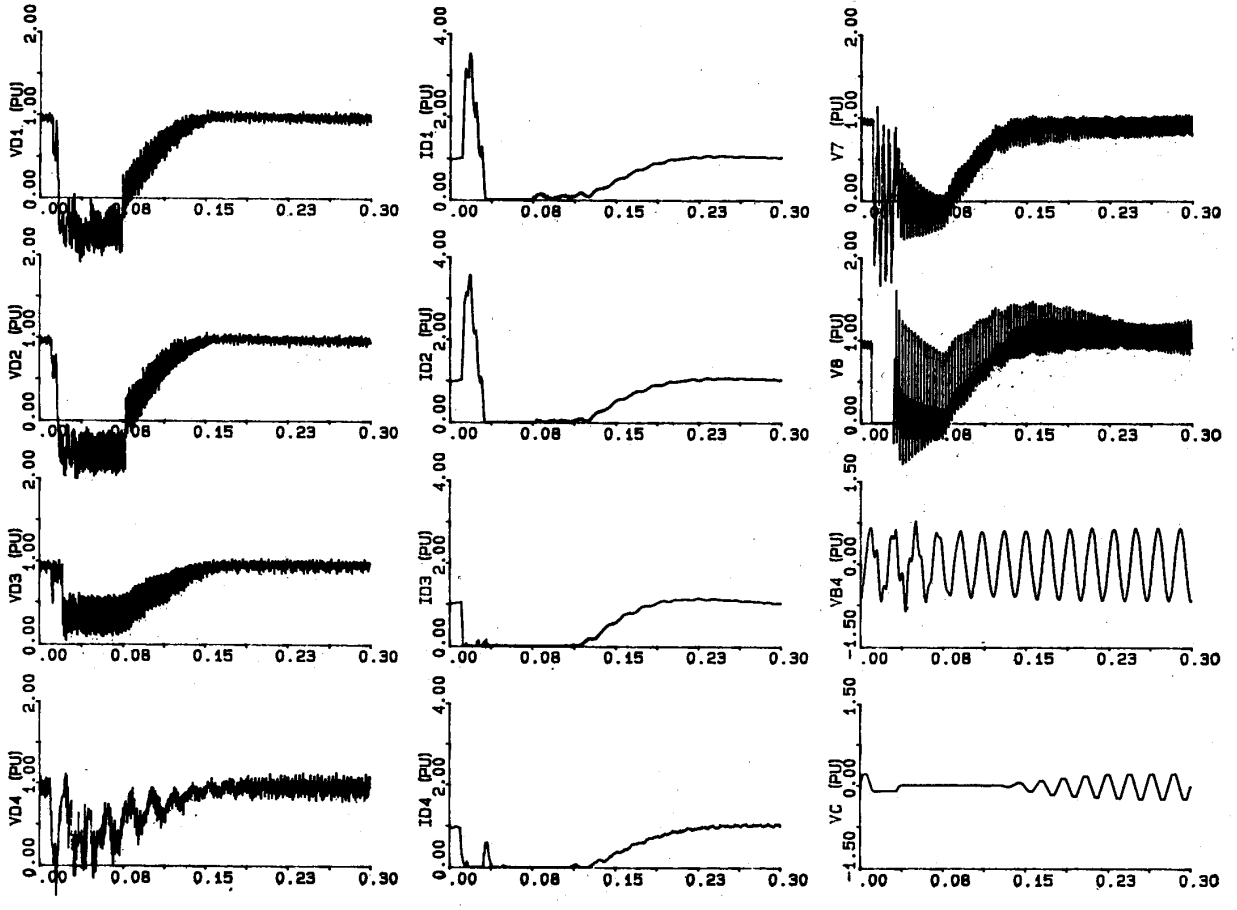


Fig. 4b Balanced ac fault at inv. 2 - With varistor



Time in second

Fig. 5 Unbalanced ac fault at inv. 2
- With varistor



Time in second

Fig. 6 DC line fault at inv. 2

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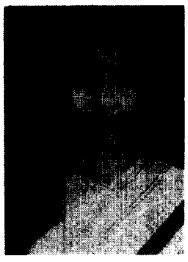

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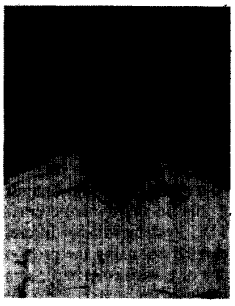

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DISCUSSION

R. S. THALLAM, Salt River Project, Phoenix, Arizona: Although series capacitors have been used in ac transmission systems for over 40 years, and the technology is well established, manufacturers have shown very little interest in applying them for HVdc systems. Artificial commutation using series capacitors has definite advantages in improving the HVdc converter performance. The authors have verified this in a multiterminal dc system and proposed a protective scheme using parallel MOV, similar to the ac series capacitor protection scheme. I have the following comments on results presented in the paper, and appreciate the authors reply.

1. The authors have investigated energy discharged by the varistor for three types of faults, balanced and unbalanced ac bus faults, and dc line fault, all at the inverter 2. The maximum energy discharge was found to be 33.2 kJ/kV, or 10.2 MJ total. An MOV with about four or five parallel columns of zinc oxide disks can easily withstand this energy. (A standard station arrester with a single column of zinc oxide disks is rated for 8 kJ/kV). Do the authors see any need for a parallel bypass gap protecting the MOV? If so, are there any other conditions more severe than described in the paper that will require protection of MOV by the parallel gap?

2. The authors have studied with an ac system SCR of 2.0 at inverter 2. How does the energy discharged by the varistor dependant on the short circuit ratio of the connected ac system? Is it possible that stronger the ac system (higher SCR), energy discharged by the varistor will be higher?

3. Line lengths of 40 to 80 miles used in the study are not typical for dc systems. Can the authors explain why such short line lengths are used in the study?

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J. REEVE, University of Waterloo, Waterloo, Ontario, Canada. The use of series capacitors for artificial commutation of HVDC converters was proposed many years ago. I appreciate the reference to a paper co-authored by me on the subject. New developments in ZnO devices which are suitable for capacitor protection permit a renewal of interest. The method is simpler, in terms of control and accommodation of circuit inductance, than some other potential forced-commutated circuits for dc transmission, and is worthy of serious consideration. The Authors have combined the considerations of capacitor protection with the application in a MTDC system. I would appreciate the Authors' response to questions on both aspects.

In a multiterminal system, the reason why a forced commutated terminal could be contemplated would be to reduce the vulnerability to commutation failures at a relatively lower power terminal and to minimize the disturbance. A low short-circuit ratio (SCR) at the same terminal compounds the problem. The Authors have used a 50% tap in their results. It is quite clear that the per-unit overcurrent, on a base of the rated terminal current, resulting from an ac fault at a small tap would be larger at a small tap than with the selected power distribution; the potential capacitor overvoltages would be correspondingly higher. Can the Authors provide test results and an evaluation of, say, a 20% tap of total inverter power and an ac system at this tap with an SCR of, say, 2.0?

The transient response of the terminal in question will be very much influenced by the controls at the rectifiers following an ac fault. It has been shown that the voltage-dependent current order limits (VDCOL) are effective in minimizing a disturbance. The Authors are requested to comment on the apparent omission of VDCOL functions in the presented waveforms.

Other questions are concerned with the assumptions made and the modeling of the bypass switches across the series capacitors. The paper states, "In the simulation, the air gap and the bypass switch are modeled as ideal switches that are closed when the varistor conducts and open when (the) varistor is not conducting." Also, the varistor is set to a protective level of 2.5 x MCOV. It seems that the switches will relieve the varistor at the point that the varistor is needed, and the capacitor voltage will be discharged at a time when it is needed for recovery. It would also seem possible for the model to permit multiple switching during one transient event as the varistor goes in and out of conduction. Unless the reactor is large, the varistor will hardly conduct at all; but, in such a case, the switches would be interrupting current in the reactor. Would the Authors explain how their model relates to a practical solution? Does the varistor energy dissipation depend on the size of the reactor? What value of inductance was used for the presented results? Since a spark gap would probably be inappropriate for modern arrester applications, is there a problem with dispensing with the gap, setting the ZnO arrester to a much lower protective level, and not relying on the bypass switch for recovery from ac faults? A lower protective level may increase the arrester duty but would maintain the capacitor voltage to a range compatible with transient recovery without the need for discharge circuits.

Manuscript received February 28, 1990.

Premila Manohar and **H. S. Chandrasekharaiah:** We thank the discussers for their interest in this paper.

In response to Prof. Reeve's discussion, the following is our reply.

1. It is true that a lower rated inverter at a low SCR station in MTDC system is more sensitive to transients than when its rating is high. The increased fault currents and the capacitor overvoltages would definitely increase the varistor rating. The effect of this on the dynamic performance of the inverter and the overall MTDC system will be different. A study with 40% and 25% tap is being carried out using the proposed method. The power is adjusted with the use of transformer tap setting. Without the ACI, the steady state performance is unsatisfactory in both the cases. With ACI a change in set current is carried out and it is seen that without commutation failure the new current level is reached in about .15 secs. For lower rated inverter the value of capacitor also has to be changed. The new value can be determined by the method proposed in this analysis. Analysis for fault conditions and fault recovery is under consideration. As an example performance for single line to ground resistive fault at the ac bus of lower rated inverter is shown in Fig. A. Further results and discussions will be published soon.
2. The aim of the present study was basically, to achieve a satisfactory performance of the inverter at low SCR station with the simple control characteristics. It was with this idea that VDCOL was not included. In fact, the numerical results indicate that during ac faults the drop in dc voltage is not significant and as such VDCOL may not be useful. However, the provision of VDCOL will be effective in minimizing the disturbances during dc line fault.
3. The authors would like to mention here that bypassing of the varistor is

not considered in the present simulation. The protective system is modelled only as the ZnO varistor and not other components are included. In the author's opinion, the triggered by-pass gap is useful, specially during long duration faults when the protection of ZnO varistor is a must. It is only a trade off between the increased varistor energy rating and the auxilliary equipment, needed for bypassing and depends purely on the specific case.

In response to Dr. R. S. Thallam's discussion, the following is our reply:

1. The bypass gap is not necessary as far as the transient cases investigated in the paper are concerned. However, if the fault persists for durations longer than that considered in the paper, the energy absorption would increase which in turn requires varistors of higher rating. In such cases, it is felt that the bypass gap would keep the varistor rating low.
2. The energy absorbed by the varistor increases as the capacitor value is reduced. This value of the capacitor, in turn, reduces as the strength of the ac system decreases. So with a stronger ac system it is expected that the energy discharged by the varistor will be higher.
3. The short line lengths of 40–80 miles represent dc cables as referred by Nozari et al [3]. We do not foresee any significant problem in handling longer lines.

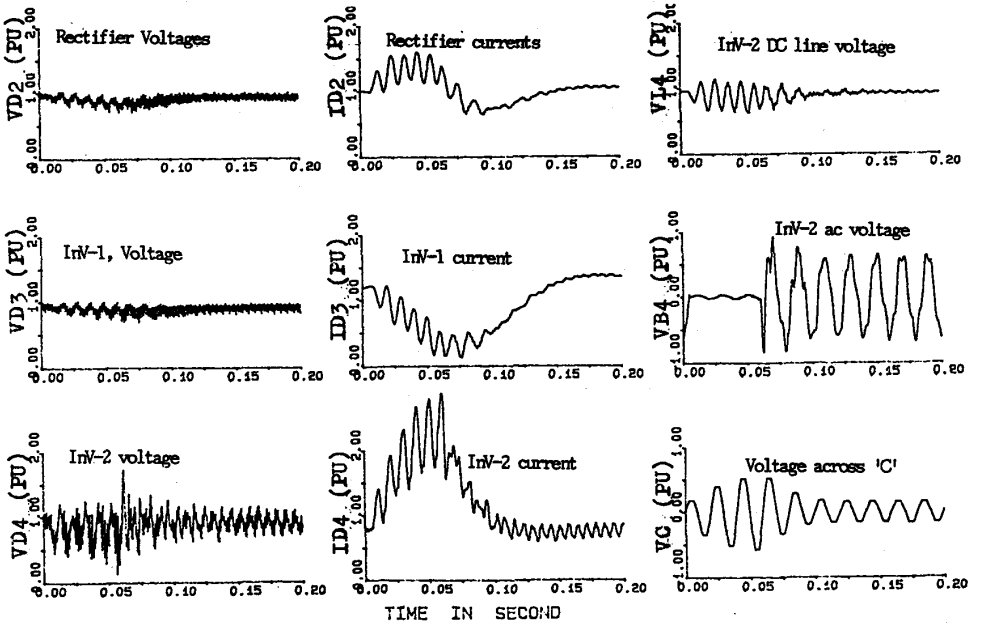

Fig. A. Voltages and currents in the MTDC system for SLG fault at Inverter-2