SOME NOVEL THYRISTOR CIRCUITS FOR CONTROLLED DC *AND* 3-PHASE AC OUTPUT FROM 1-PHASE SUPPLY FOR DRIVE APPLICATIONS

K.Venkata Ratam, Dinkar Prasad

1 Introduction

The paper describes the development of new topologies of thyristorised power converters for controlled dc as well as 3-phase ac output using single phase supply with possible application to electric traction. The input side power factor is kept high and the thyristors are load commutated with the help of two a.c. capacitors.The circuits can work at considerably high frequencies using not too fast thyristors. The turn-on and turn-off losses are kept low due to soft switchings. In all, three stages of power conversion are proposed. 'The first stage is a 1-phase ac to dc boost converter which converts the ac input into fixed dc voltage with a magnitude higher than the peak of the input voltage. This is followed by a second stage which is a fast response dc to dc chopper with reduced switching losses. The output of this stage can be directly fed to a dc motor (for dc traction). The third stage of power conversion consists of a new inverter circuit and is meant for ac motor drive. The inverter is directly connected to the output terminals of the second stage. The proposed inverter circuit does not need any commutation elements and the thyristors used can be of converter grade. Only one snubber circuit is needed. However the inverter needs **12** thyristors in place of the usual 6 thyristors and 6 diodes. In the following sections, the operation of the above circuits is explained briefly and the experimental oscillograms of currents and voltages at different stages as obtained from laboratory scale set-ups (along with necessary controllers) are given.

2 Thyristorised 1-phase AC to DC boost converter

This stage converts the ac input to fixed dc voltage with a magnitude higher than the peak of the input voltage and is shown in Fig. 1(a). The circuit is similar in principle to the conventional transistor boost converter, except that the transistor switch is replaced by a thyristor switch consisting of four thyristors and a high frequency capacitor (C_R). The moderately large dc capacitor (C_o) at the output end maintains a practically constant output voltage (V_{co}). The thyristor pairs (1,2) and (3,4) can alternately **be** fired to output a series of current pulses at moderately high frequency (1-3 kHz) because a good portion of the cycle time is available as turn-on time. The turn-on is soft due to the presence of L_R. The ac capacitor facilitates natural commutation of the thyristors. The circuit can be analysed assuming the input voltage (v_{an}) to be practically constant during the short period of each current pulse. With the turning on of each thyristor-pair (say, 1,2) a resonant current pulse is established through the source L_R and C_R. Due the previous charging, C_R is charged to V_{co} with polarity which aids the source voltage $|v_{an}|$. The sinusoidal rise of resonant voltage V_{CR} across C_R is checked at the instant $|V_{CR}| = V_{Co}$, since beyond this diode D gets forward biased and the inductor current finds a path into output, capacitor C_o. C_o being very large ($C_o \gg C_R$), the output voltage V_{CO} remains practically unchanged and the inductor current falls to zero linearly. Thyristors turn-off naturally with zero voltage across them. Thus the turn-off is also soft. The voltage across C_R remains at V_{CO} with a polarity which is opposite to the polarity when the cycle started. After the inductor current falls to zero, the alternate thyristor pair (3, 4) can be turned on with or without delay and another h.f. current pulse passes through L_R and C_R and the cycle repeats. Circuit analysis shows that the charge Q supplied by the source during each h.f. pulse is equal to

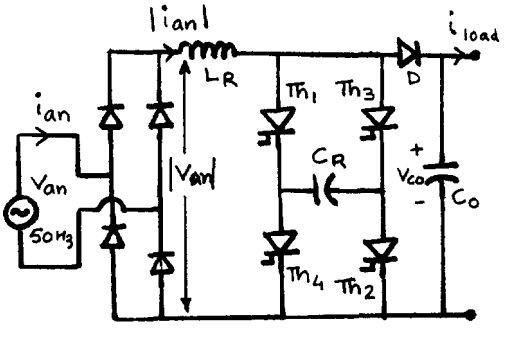

Fig. 1a Thyristorised AC to DC **boost converter**

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$$Q = 2C_R \frac{V_{CO}^2}{V_{CO} - |v_{an}|} \quad (1)$$

Now if the triggering frequency of the thyristors 'f' is made to vary with time, the a.c. source current $i_{an}(t)$, averaged over a small interval of time is given by

$$i_{an}(t) = 4f(t)\, C_R \frac{V_{CO}^2}{V_{CO} - |v_{an}|} \quad (2)$$

In the above equation the effect of high frequency ripple on the a.c. source current is neglected. In other words, $i_{an}(t)$ is the time average of the a.c. source current but this averaging is done over a very small time period (much smaller than the supply cycle period). The said h.f. ripples in the line current'

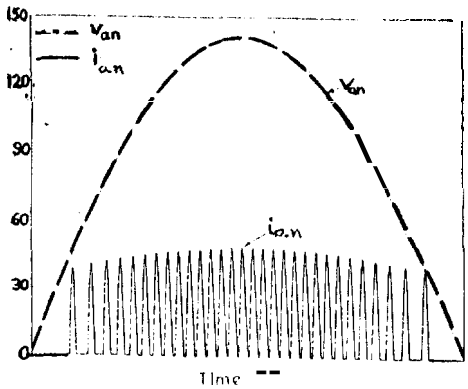


Fig. 1b Supply current pulses during one halt cycle (theoretical)

can be filtered easily using less bulky filtering elements. Barring h.f. ripples, the input current $i_{an}(t)$ can be made proportional to the instantaneous voltage $v_{an}(t)$ if the triggering frequency is chosen as

$$f(t) = K_G \frac{|v_{an}|\,(V_{CO} - |v_{an}|)}{V_{CO}^2} \quad (3)$$

where K_G is proportionality constant. With 'f(t)' modulated as per the above equation,

$$i_{an} = 4C_R\, K_G\, v_{an} \quad (4)$$

making the input current to be in phase with the supply voltage, thus making the input pf unity (except for the h.f. ripple). Fig 1(b) shows the theoretical distribution of supply current pulses during half cycle of the supply using the above control law. It can be seen that the pulse frequency is zero at either end of the half cycle and reaches its maximum value at the centre of the half cycle of the supply. The maximum value itself can be changed by changing the gain factor K_G, which in turn changes the rms current drawn from the supply.

2.1 Design considerations

It is shown in [3] that a choice of $V_{CO} = 2v_{an}$max is optimum from the consideration of thyristor ratings and available circuit turn-off time. The values of L_R and C_R decide the maximum attainable switching frequency and the maximum output power to the load for a given input voltage. The selection of C_o is based on permissible ripple voltage at the output. A design example worked out in [3] shows that a 1 MW converter using thyristors with 50 μs turn-off time from 1-phase 1500 V (rms) supply and with an output d.c. volts of 5000 V, requires $L_R = 61\,\mu$H and $C_R = 3.3\,\mu$F. For 10 % ripple, dc capacitor required is 1275μF. The thyristor ratings work out to be 1700 A, 5000 V.

An analog controller for closed-loop modulation of frequency as per eqn. (3) is built on laboratory scale and tested. The gain K_G is controlled depending on the departure of V_{CO} from a reference voltage V_{CO}^*. For protection against overloading and short-circuit at the output, the input side diode rectifier in Fig.1(a) is replaced by a semiconverter. The firing angle of the thyristors in the semiconverter is kept at zero for normal (healthy) conditions. During overload or short circuit as the output V_{CO} rapidly decreases and when it falls below a threshhold value, the thyuristor firing angles are delayed by nearly 180°, thus reducing the input voltage to zero. The oscillograms of the supply current (unfiltered) are shown in Fig. 2(a) and 2(b) for low load and high load conditions. The crowding of the current pulses at the instants the supply voltage reaches peak values can be clearly seen. Fig. 2(c) shows the waveform of the filtered and unfiltered supply current while Fig. 2(d) shows the waveforms of the supply voltage and supply current. The in-phase nature of the supply current can be clearly seen in Fig. 2(d).

3 Fast response DC to DC converter with reduced switching losses

The boost converter of the preceeding section is followed by a fast response dc to dc chopper with reduced switching losses and is shown in Fig. 3. This forms the second stage of power conversion. The circuit is a modified version of the load cornmutated chopper proposed by Dewan et al [1]. The modification is by way of putting small saturable reactors in series with each thyristor to reduce the turn-on losses without hampering the operating frequency of the original chopper. (Dewan's chopper has two important features: it can be operated at moderately high frequencies because a good portion of the cycle time is available as turn-off time and since the turn-off is soft, the corresponding turn-off loss is also small.)

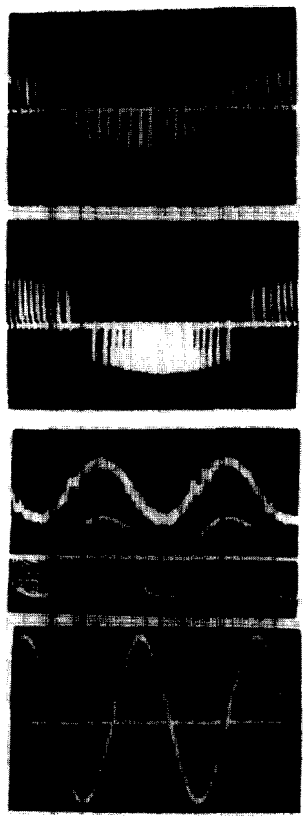


Fig. 2 Experimental oscillograins for **the** boost converter

(a) Supply current for low power output

(b) Supply current for high power output

(c) Unfiltered and filtered supply currents

(d) Input voltage arid (unfiltered) supply current

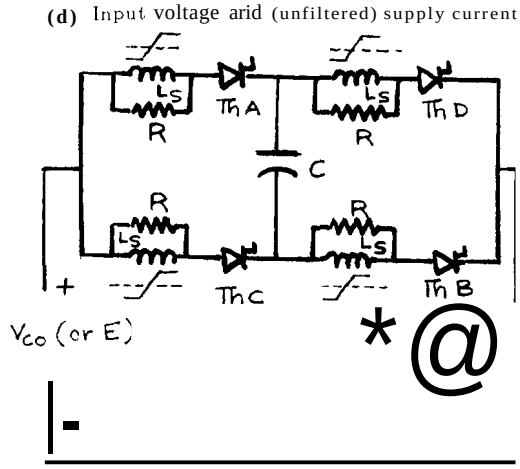


Fig. 3 **Load** commutated chopper **with** proposed modification

For inductive loads, the output consists of a series of saw-tooth shaped voltage pulses (with a peak value equal to twice tlie dc input value), each pulse delivering an energy of $2Cv_{co}^2$ to the load. The output power can be controlled by modulating the chopper frequency (usually in the range of 1 to 4 kHz). A detailed analysis of the chopper with saturable reactors is given in [3]. The reactors are designed to saturate at. a small portion (about 5 %) of the full load current.. The reactors not only limit the **turn-on** $ of tlie thyristors to a low value but also **keep** the turn-on losses low. The accompanying (high) parallel resistors R are put to suppress the transient voltage arising due to abrupt cessation of current in thyristors. Losses in the resistors (which take place only during turn-on time) can be kept low (to about 1.5%) of rated output if properly chosen. The output of the chopper can be used to directly feed a separately excited dc motor. An analog controller is designed and built to control the current (and hence torque) of a laboratory size dc motor. The controller is provided with safe guards against commutation failure and loss of field. The details are given in [3]. Fig. 4(a) shows the experimental oscillograrns of load current, and voltage when the chopper is operated at 4 kIIz with a passive R-L load. Fig. 4(b) shows the soft turn-off and characteristic of the chopper. The traces show the current and voltage of any one thyristor. It can be seen that the current falls to zero with negligible voltage across the device. Fig. 4(c) shows the traces of thyristor current and the voltage across the saturable reactor. It can be seen that at the turn-on, all the voltage appears across tlie reactor (as a spike) and the turn-on of the thyristor is soft. Fig. 4(d) shows the load current and chopper output voltage when the chopper is feeding a separately excited dc motor and when the armature current is maintained constant at a set value (5 **A)** by the controller. Fig. 4(e) shows the speed-time curve of the motor while accelarating from rest at constant set value of the armature current. Fig. 4(f) shows how the power input. to the motor is automatically reduced (by reduction of the chopper frequency) when there is an accidental loss of field while the motor is running.

4 A new thyristorised inverter without commutation elements

The third stage of power conversion (Fig. 5) consists of a new inverter circuit and is meant for ac motor drive. The inverter is directly connected to the second stage (dc to dc chopper). No additional commutation elements are needed and the thyristors used can be of converter grade. Only one snubber circuit at the input of the inverter **is** sufficient. How-

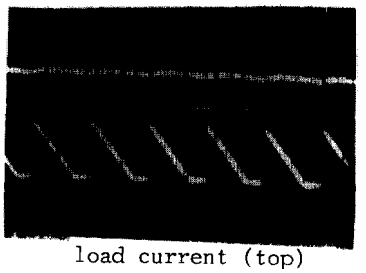
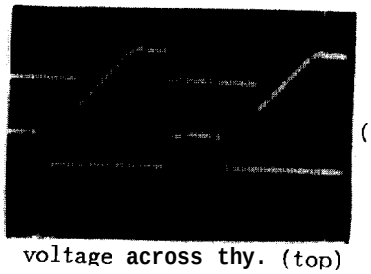


Fig.4

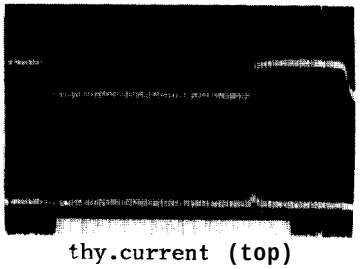
(a)

load current (top)
load voltage (bottom)



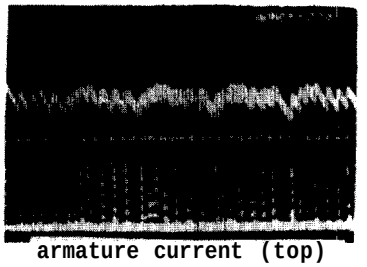
(b)

voltage across thy. (top)
current in thy.(bottom)



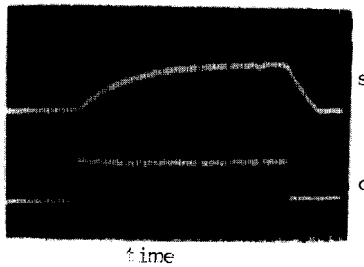
(c)

thy.current (top)
saturable reactor voltage (bottom)



(d)

armature current (top)
armature voltage (bottom)



speed

(e)

current

time

(f)

arm.current (top) & arm. voltage (bottom) under field loss

Fig. 4 Current and voltage oscillograms of the modified chopper

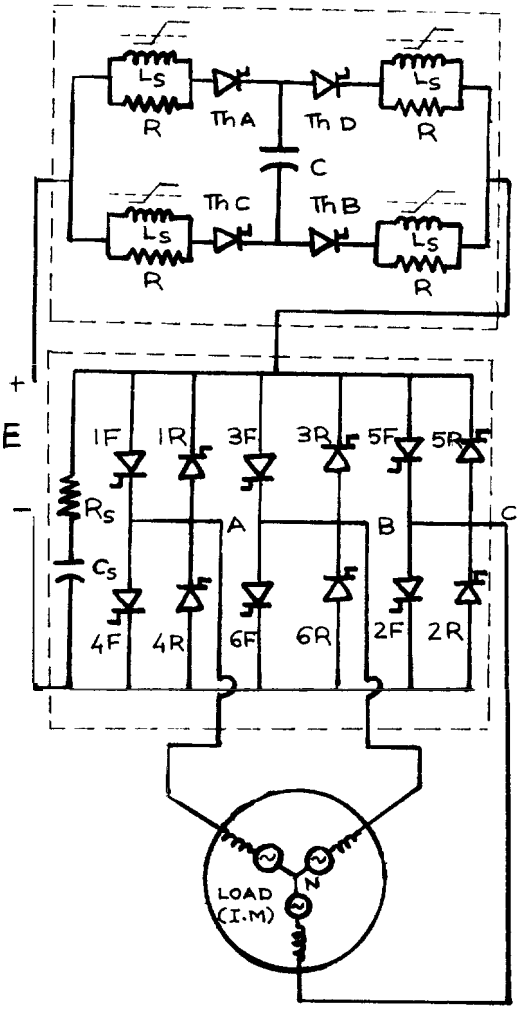


Fig. 5 Topology of the new inverter circuit

ever, the inverter requires 12 thyristors: 6 forward thyristors (Th_{1F} ....Th_{6F}) connected in usual fashion with the other 6 thyristors (Th_{1R}, ..., Th_{6R}), which can be of reduced current rating, connected in the reverse direction. The output voltage of the inverter has an envelope similar to that of a conventional quasi-square wave, with each subinterval of 60" consisting of a number of saw-tooth shaped h.f. voltage pulses output by the chopper circuit, Fig. **6** . The zero-voltage period between two successive h.f. pulses is controlled by turning on suitably the reverse connected thyristors to facilitate free-wheeling of the load current. While switching can be very fast within each 60^o interval, extended commutation time is required during the change over from one 60" period to the next ,i.e., when the forward thyristors undergo commutation. The schematic triggering pattern of the gate pulses to the different thyristors of the inverter and those of the chopper are shown in Fig. **7.** It can be seen that all the forward thyristors have gate pulses exactly like in a conventional inverter (i.e., nearly 180^o duration)and in the usual sequence **1,2,3,...6,1.**The reverse thyristors have basically gate pulses of 60" duration in the sequence **3,4,5,..2,3**. The reverse thyristors in addition to the above get gate pulses of short duration just before the corresponding forward thyristors are gated (Fig. 7). The operation of the inverter in steady state can be explained as follows. Consider **an** instant somewhere in the middle of the sub-interval of 60" when Th_{1F}, Th_{2F} and Th_{3F} are gated. During this sub-interval, gate pulse is also present for Th_{5R}. Now as soon **as** Th_A and Th_B of the chopper are fired, a voltage of amplitude **2E will** appear across the inverter input. This will result in the conduction of all the gated forward thyristors, i.e., Th_{1F}, Th_{2F} and Th_{3F}. If the load curent is assumed constant during **a** small interval of time, the inverter input voltage falls linearly, as the capacitor in the chopper starts charging towards opposite polarity. When the input voltage to the inverter becomes slightly negative, Th_{5R} gets automatically forward biased and starts conducting. Th_{2F}

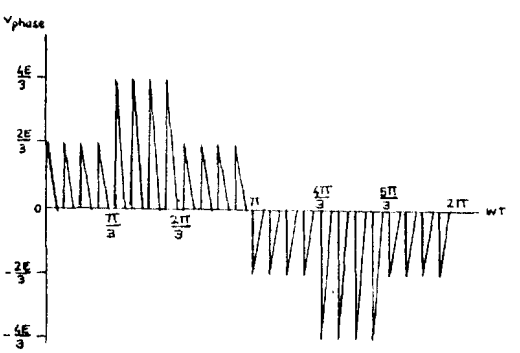


Fig. 6 Output phase voltage of **the** inverter (theoretiral)

gets reverse biased and turns off. At the same time the load current free-wheels through Th_{1F},Th_{3F} and Th_{5R}. Since Th_{2F} is off,Th_A and Th_B of the chopper also stop conduction. Subsequently, when gate pulses are given to Th_C and Th_D of the chopper, the inverter voltage jumps once again to **2E** and Th_{1F}, Th_{2F} and Th_{3F} start conducting and Th_{5R} turns off. This mode is once again followed by the freewheeling of the load through Th_{1F}, Th_{3F} and Th_{5R}. Thus, a series of saw-tooth shaped voltage pulses appear across the input of the inverter and the corresponding load terminals. Transfer of current from Th_{2F} to Th_{5R} and vice-a-versa can be very fast. Now, at the end of the 60^o period Th_{1F} is to be turned off and Th_{4F} is **to** be turned on. For this purpose the freewheeling of the load current is allowed through Th_{4R}, Th_{6R} and Th_{2F} by applying gate pulses to Th_{4R} and Th_{6R} and removing gate pulse to Th_{5R}. Th_{2F} gate pulse continues to exist. This mode is extended for considerable time so that Th_{1F} is turned off and regains its forward blocking capability. For the next 60^o, gate pulses are present for Th_{2F}, Th_{3F} and Th_{4F} and also for Th_{6R}. Gate pulse for Th_{4R} is removed (see Fig. 7). During this 60^o interval, the powering mode occurs when Th_{2F}, Th_{3F} and Th_{4F} are forward biased and freewheeling occurs through Th_{2F}, Th_{6R} and Th_{4F}. Because of the current lag, Th_{4F} may not conduct immediately even though it is gated, the current being carried by Th_{4R}. However after an angle ϕ (ϕ being the pf angle of the load), current flows through Th_{4F} and Th_{4R} turns off. Reference **[3]** gives more details regarding the different, modes of operation. In [3] an alternative inverter circuit using 6 forward thyristors, **2** reverse thyristors and 6 diodes is also presented. The power flow into the load is solely controlled by the chopper frequency, since each switching of the chopper thyristor pair results in a fixed amount of energy being transferred to the load. One limitation of the proposed inverter is that it cannot supply loads with pf less than **0.5** lag. Still this is not a serious limitation since the pf of the induction motor can be kept higher than **0.5** by feedback control of the slip-speed which is generally used in variable speed IM drive. An analog controller is built to provide the necessary gate pulses to the inverter (as mentioned above) and tested to control the speed of **a** laboratory size IM. Typical oscillograms of voltages and currents at different points are shown in Fig. 8. Reference **[3]** discuses the dynamic braking aspects of the motor as well.

5 Conclusions

The circuits proposed in this paper have tried to utilise the maximum switching capability of the thyristors and **as** a result even converter grade thyristors can be used while maintaining a high switching frequency(1 to **3** kHz). The supply(1-phase) side pf is high and the h.f. frequency ripple current can be filtered out **with** less bulky filtering circuits. The cir-

cuits have fast control over output current (including protection against overload and short circuit). The switching losses are kept low by soft turn-on and turn-off. No additional commutation circuits, apart from two h.f. power capacitors, are needed. However the circuits developed use larger number of thyristors than conventional circuits. The controllers, although more complex, can be realised with analog/ digital circuits as shown by experimental results. It is hoped that the circuits developed either in parts or as a whole may compete favourably from overall cost point of view with circuits utilising GTOs in high power applications like traction

References

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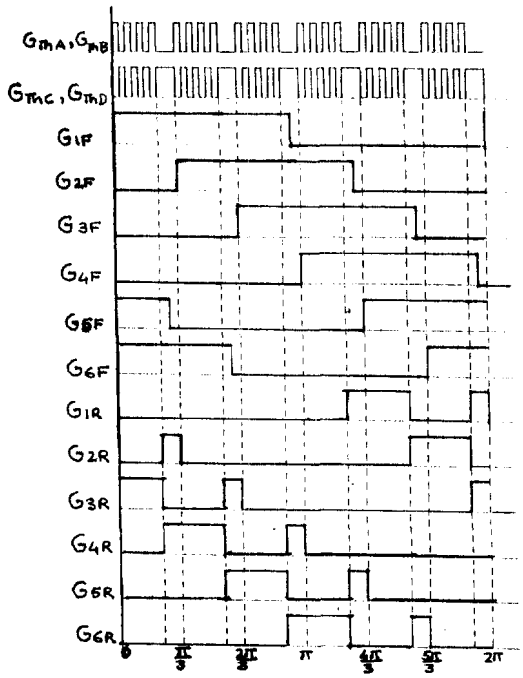

Fig. 7 Gate pulses to the thyristors of the proposed inverter

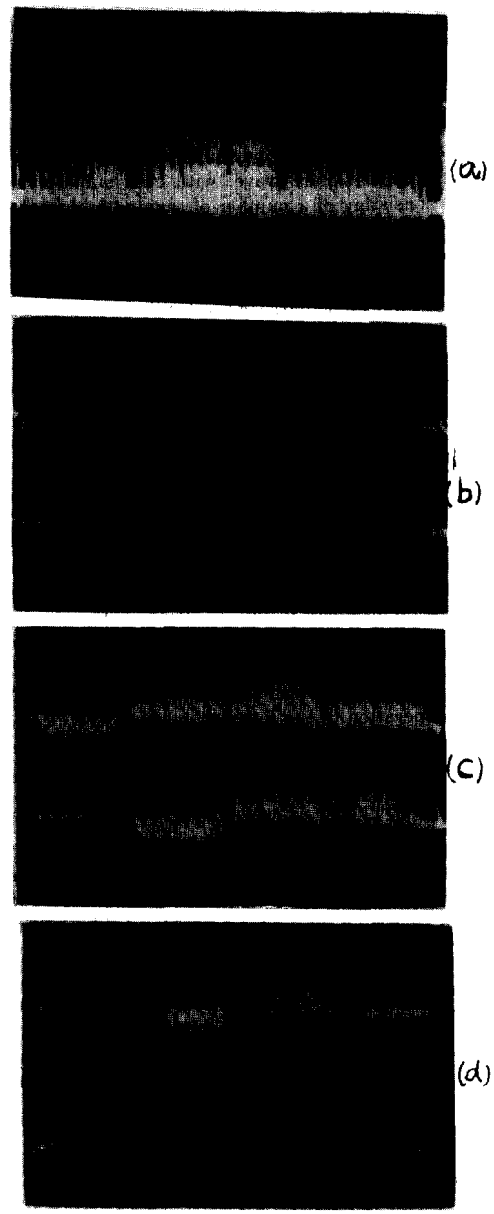

Fig. 8 Voltage and current oscillograms of the inverter circuit

(a) Input voltage pulses to inverter
(b) phase voltage at reduced output
(c) (phase voltage at higher output
(d) Line voltage and phase current in the ioad (induction motor)