# CONCEPTS OF VOLTAGE INSTABILITY AT CONVERTER BUS IN HVDC LINKS

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## INTRODUCTION

High voltage direct current (HVDC) links are increasingly used for asynchronous interconnection of AC systems apart from long distance bulk power transmission. The interconnection through HVDC links are generally characterized by weak AC systems. The relative strength of the AC system at the point of coupling is measured by short circuit ratio (SCR) which is defined as the equivalent admittance of the AC system on the base of DC power rating. The AC system is considered to be weak when SCR is less than three.

There are several operational problems associated with weak AC systems (1). one of the major problems is voltage instability at converter bus. Hammad and Kuhn *(2)* have used a simple measure called voltage stability factor (VSF) defined below:

$$VSF = \Delta V / \Delta Q_c \quad | \quad P_d = P_{do} \qquad (1)$$

where AV is the incremental change in the bus voltage due to a small change in the shunt reactive compensation $\Delta Q_c$. Large positive values of VSF imply problems of voltage regulation and negative values imply instability.

The solution to the problem of voltage instability can be through (i) strengthening the AC system (ii) novel converter control strategies or (iii) The application of static VAR compensator (SVC) at the converter bus (3-5). The steady state analysis of voltage stability using the measure of VSF is also useful in comparing the effectiveness of various controllers.

The computation of VSF has been primarily applied at the inverter bus. However, it is possible to give a general formulation for the computation of VSF which is also applicable to multi-terminal DC (MTDC) systems. This is done by treating VSF as a matrix defined by

$$\Delta \underline{V} = [VSF] \Delta Q_c \qquad (2)$$

where VSF(i,j) is the partial derivative of $V_i$ with respect to $Q_{cj}$. This generalization allows the definition of mutual VSF when i≠j, and this is not always zero.

This paper presents a general steady state analysis of voltage instability which is applicable to MTDC systems and also permits the comparison of various controller strategies. In a parallel connected MTDC system of which two terminal link is a special case, one of the terminals, called the voltage setting terminal(VST), sets the DC voltage reference for all other terminals acting on either constant current or constant power control. The VST can have different control strategies such as (A) Constant angle (CAC) (B) Constant power factor (CPF) (C) Constant reactive power (CRP) (D) Constant reactive current (CRC) (E) Constant direct voltage (CDV) and (F) Constant AC voltage (CAV).

A case study of an asynchronous two terminal HVDC link is presented to illustrate the analysis and compare the various novel converter control strategies.

## SYSTEM MODEL

A general 'n' terminal MTDC system is considered for the analysis. However the following assumptions are made to simplify the analysis and yet retain those aspects that are of relevance

(i) The HVDC system forms asynchronous interconnection between several unconnected AC systems.

(ii) The AC system connected to each terminal can be represented by Thevenin's equivalent (at fundamental frequency) viewed from the converter bus.

(iii) The on-load tap changers (OLTC) of the converter transformers are slow in action and hence the transformer taps are assumed to be constants during a transient.

(iv) Any converter terminal can act as the voltage setting terminal. However there is no loss of generality in assuming the 'n'th terminal as VST.

### Converter Eauations

At any converter terminal 'j', the following equations are applicable

$$V_{dj} = k_j a_j V_j \cos\theta_j - R_{cj} I_{dj} \qquad (3)$$

$$P_{dj} = m_j V_{dj} I_{dj} \qquad (4)$$

$$Q_{dj} = V_{dj} I_{dj} \tan\phi_j \qquad (5)$$

$$\cos\phi_j = V_{dj} / k_j a_j V_j \qquad (6)$$

where all the variables are expressed in per unit system that is more flexible than used in the past (6). $a_j$ is the off-nominal turns ratio of the converter transformer at terminal 'j'. The converter angle $\theta$ can be either the delay angle ($\alpha$) for the rectifier or the extinction angle ($\gamma$) for the inverter terminal. The current $I_{dj}$ and voltage $V_{dj}$ are assumed to be positive. Hence the coefficient $m_j$ is introduced which is +1 for the rectifier and -1 for the inverter.

### DC Network Eauations

Choosing the DC bus at the VST (nth terminal) as the reference bus, the DC voltage at terminal 'j' is given by

$$V_{dj} = \sum_{k=j}^{n-1} m_k R_{jk} I_{dk} + V_{dn}, \quad j=1 \text{ to } (n-1) \qquad (7)$$

where $R_{jk}$ is an element of the bus resistande matrix of the DC network with bus 'n' as reference. The current ($I_{dn}$) at VST is given by

$$m_n I_{dn} = -\sum_{k=1}^{n-1} I_{dk} m_k \qquad (8)$$

In the case of a two terminal HVDC link, the equations (7) and (8) reduce to

$$V_{dr} = V_{di} + R_d I_d \qquad (9)$$
$$I_{dr} = I_{di} \qquad (10)$$

Power Flow Equations at the Converter Bus:

Because of assumptions (i) and (ii), the AC system at the jth terminal can be represented as shown in Fig. 1. From Fig. 1, the following power flow equations can be written at converter bus 'j'.

$$P_j = m_j P_{dj} = V_j E_j g_j \cos\delta_j - V_j^2 g_j + E_j V_j b_j \sin\delta_j \qquad (11)$$

$$Q_j = Q_{dj} - Q_{cj} = V_j E_j b_j \cos\delta_j - V_j^2 b_j - V_j E_j g_j \sin\delta_j \qquad ...(12)$$

where $g_j = R_j/(R_j + X_j)$, $b_j = -X_j/(R_j + X_j)$

Controller Equations

As the transformer tap 'a' is assumed to be constant, the only control variable available at each terminal is 'e'. The control strategy is to maintain one of the scheduled variable at a preset value. At non-VST, the scheduled quantity can be current or power. Thus for terminals 1 to n-1, the following equations apply

$$W_j = P_{dj} \text{ or } I_{dj} = W_j^{spec}, j=1 \text{ to } (n-1) \qquad (13)$$

Where $W_j$ is the scheduled variable at terminal 'j'. At VST, there can be several possible control strategies. For a given control strategy, the following scalar equation applies

$$W_n = W_n^{spec} \qquad (14)$$

where $W_n$ can be (i) $e_n$ (ii) $\phi_n$ (iii) $Q_{dn}$ (iv) $I_{qn}$ (v) $V_{dn}$ or (vi) $V_n$.

The reactive current $I_{qn}$ (at terminal n) is given by

$$I_{qn} = k_n a_n I_{dn} \sin\phi_n \qquad (15)$$

VOLTAGE STABILITY ANALYSIS

The steady-state analysis of voltage-stability is based on linearized algebraic equations. It is essentially a part of the small signal stability analysis with dynamics neglected. It is assumed that the system is subjected to small perturbations around an operating point.

Linearising equations (3) to (8), and (13) we can obtain

$$\Delta P_d = F_{pd} \Delta V_{dn} \qquad (16)$$

$$\Delta Q_d = F_{qd} \Delta V_{dn} + [F_{qv}]\Delta \underline{V} \qquad (17)$$

After linearizing equations (11) and (12) and utilizing equations (16) and (17), we have

$$\Delta \underline{V} = [H]\Delta Q_c + \underline{g}\, \Delta V_{dn} \qquad (18)$$

where [H] is a nxn, diagonal matrix.

Linearizing equation (14), it is possible to get the following relationship

$$c_1 \Delta V_n + c_2 \Delta V_{dn} = 0 \qquad (19)$$

The above equation is applicable to all the six controllers at VST.
From (18), we have,

$$\Delta V_n = h_n \Delta Q_{cn} + g_n \Delta V_{dn} \qquad (20)$$

Combining (19) and (20) we obtain

$$\Delta V_{dn} = c_n \Delta Q_{cn} \qquad (21)$$

Substitutng (21) in (18), we get

$$\Delta \underline{V} = [VSF]\Delta Q_c = \{[H] + c_n \underline{g} \underline{e}_n\} \Delta Q_c \qquad (22)$$

where $\underline{e}_n$ is a row vector with only one non-zero element, $e_n(n) = 1.0$.

Comments: From the structure of the [VSF] matrix given in (22), the following observations are applicable.

1. For CDV control at VST, the VSF matrix is diagonal with entries VSF(j,j) = $h_j$.
2. The self VSF, $h_j$, at a terminal other than VST, is a function of the AC system strength or SCR at that terminal. It is independent of the control strategy at any converter.
3. The self VSF at VST is not only a function of the SCR at that terminal, but also of the converter control.
4. The mutual VSF ($\Delta V_j/\Delta Q_{cn}$) is a function of SCRs at the terminal j and the VST in addition to the control strategy.
5. When current control is used at all (non-VST) terminals (j=1 to n-1) then CRC control at the VST is equivalent to CPF control.

A CASE STUDY

The analysis presented in the previous section is applied to the example of a two terminal asynchronous HVDC link. The rectifier is assumed to be on either (I) constant current control or (11) constant power control. Six possible control strategies listed earlier are considered for the inverter.

Results and Discussion

Figure 2 shows the self VSF at the inverter as a function of the inverter SCR for case I for different inverter control strategies. It is seen from Fig.2 that CDV control is the best and CRP control is the worst. CRC or CPF control is slightly better than CEA control.

Figure 3 shows the self VSF at the inverter for case 11 (constant power) as a function of SCR and for different inverter controls. Here CEA control is the worst and CDV control is again the best. The curve marked 4 corresponds to the case with CEA control and the DC line resistance neglected. Figure 4 shows the variation of mutual VSF as a function of inverter SCR for case I. It is interesting to observe that the mutual VSF is negative with CAV control. Figure 5 shows the variation of self VSF at the rectifier

for the three cases (a) with inverter as VST (b) with rectifier as VST (i) inverter on constant current Control and (ii) inverter as constant power control. In case (a) the self VSF is independent of the control. It is assumed for case b, that the rectifier is an constant delay angle control.

## CONCLUSIONS

In this paper, a general formulation for the steady state analysis of voltage stability is presented with a case study of a two terminal HVDC link. The analysis is also applicable to MTDC systems. The following conclusions can be drawn from the analysis and the case study.

1. The voltage instability is a more severe problem at the voltage setting terminal compared to other terminals irrespective of whether it is rectifier or inverter.

2. While in general, the voltage collapse (instability) at a terminal occurs as the AC system strength is reduced at that terminal, it is also influenced by the SCR at the VST and the control strategy used. The constant current control results in a lower value of critical SCR (corresponding to the onset of instability) than the constant power control.

3. The use of novel converter control at the inverter results in improved voltage stability compared to the CEA control. The constant DC voltage (CDV) control gives the best results followed by constant reactive current (CRC) control. Another advantage of CDV control is that voltage instability at a terminal is unaffected by the AC system strength at VST.

4. Although constant AC voltage (CAV) control at the VST can improve voltage stability at that terminal, it does not help in overcoming voltage instability at other terminals.

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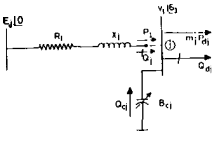

Figure 1 Equivalent system at converter j

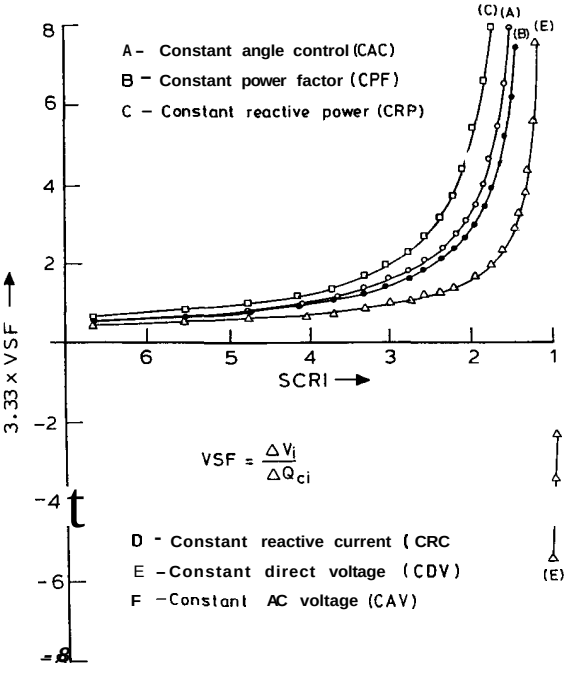


Figure 2 Self VSF at inverter terminal - case I

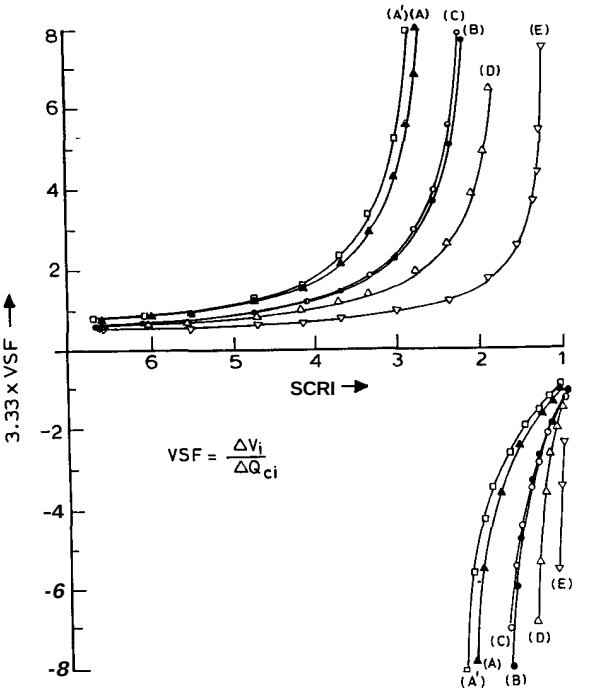


Figure 3 self VSF at inverter terminal - case II

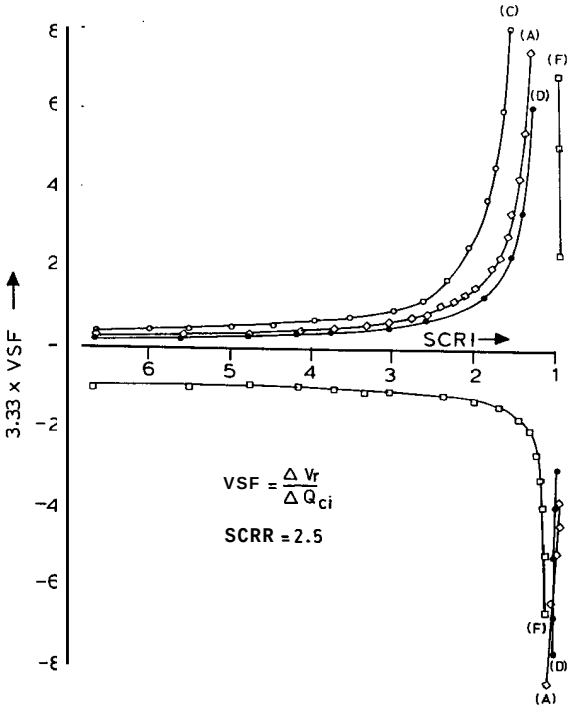


Figure 4 Variation of mutual VSF

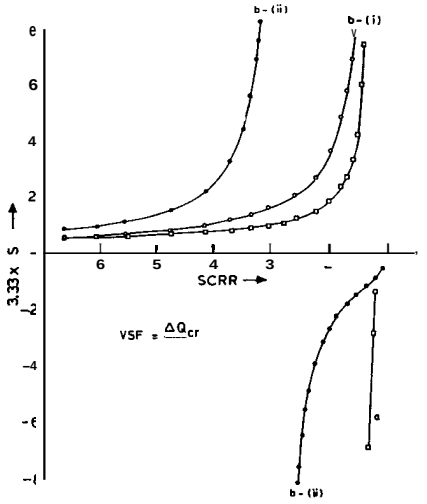


Figure 5 self VSF at rectifier terminal