tooth waves. Here the speed is proportional to the frequency of the sawtooth waves and the resolution is increased by decreasing the frequency of the sawtooth waves. Thus for practical purposes, one has to look for a compromise between resolution and the speed of conversion. Moreover, the speed of conversion is constant in this system and this is an advantage over other A/D converters. We observed that the measurement starts from approximately 50 mV, because of the V_{ce} saturation voltage. The capacitor does not discharge to 0 V. In order to overcome this problem one can connect the emitter of transistor BC 109 to negative voltages so that the minimum level of the sawtooth voltage can be set at zero or even at negative voltages. When doing this one has to take care that the transistor does not enter into conduction without the triggering pulse from the previous stage.

ACKNOWLEDGMENT

The authors thank K. J. S. Sawhney, H. S. Vora, and A. K. Tickoo for discussions.

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Transducer Output Signal Processing Using Dual and Triple Microprocessor Systems

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Abstract—**The application of dual-port memory (DPM)-based dual and triple microprocessor systems for improving the speed of transducer output signal processing which involves corrections, using interpolating polynomials, for input-output nonlinearities and effects of disturbing variables, is presented. Significant processing speed improvement over single microprocessor implementation is shown by analytical evaluation.**

I. INTRODUCTION

A technique to correct transducer nonlinearities and disturbing variable effects using an 8-bit microcomputer has been described by Mahana and Trofimenkoff [1]. They have shown how interpolating polynomials may be used to fit calibration data, and then compute the actual value of a primary variable in two alternative methods: 1) direct computation of the polynomials and 2) use of a multidimensional look-up table. The first method is more accurate but takes a long time for computation (of the order of a few seconds), while the second method, though faster, is not very accurate. In this paper, we consider an alternative approach for 1), which uses dual and triple microprocessor systems for improving the processing speed so that higher accuracy is not traded off with processing speed as in 2). The details of interpolating polynomials, architectural, and operational aspects of dual and triple microprocessor systems, task allocation, and an analytical evaluation of processing speed improvement are given in the following sections.

Manuscript received March 15, 1988; revised September 30, 1988.

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IEEE Log Number 8927418.

II. INTERPOLATING POLYNOMIALS

Let P_x be the primary variable, and P_y and P_z be two disturbing variables. Corresponding to P_x, P_y, and P_z, let x, y, and z, respectively, be the transducer output values after A/D conversion. Let f be the value of P_x if the effect of nonlinearities and the two disturbing variables is taken into account. Then, the interpolating polynomials are as follows:

$$f = a_0(y, z) + a_1(y, z)\,x + a_2(y, z)x^2 + \cdots + a_n(y, z)x^n \tag{1}$$

where $a_i(y, z)$ $(i = 0, 1, \cdots, n)$ are given by

$$a_i(y, z) = b_{0i}(z) + b_{1i}(z)y + b_{2i}(z)y^2 + \cdots + b_{mi}(z)y^m \tag{2}$$

where $b_{ji}(z)$ $(j = 0, 1, \cdots, m;\ i = 0, 1, \cdots, n)$ are given by

$$b_{ji}(z) = c_{0ji} + c_{1ji}z + c_{2ji}z^2 + \cdots + c_{pji}z^p \tag{3}$$

where c_{kji} $(k = 0, 1, \cdots, p;\ j = 0, 1, \cdots, m;\ i = 0, 1, \cdots, n)$ are constant coefficients.

The calibration protocol to determine the c_{kji} coefficients has been detailed in [1]. Once the c_{kji} coefficients have been determined, they can be stored in the ROM, and the value of the primary variable f may be computed for any measured values of x, y, and z as follows:

a) compute $b_{ji}(z)$ coefficients from (3);
b) compute $a_i(y, z)$ coefficients by substituting the values of $b_{ji}(z)$ coefficients, computed above, in (2);
c) compute f by substituting the values of $a_i(y, z)$ in (1).

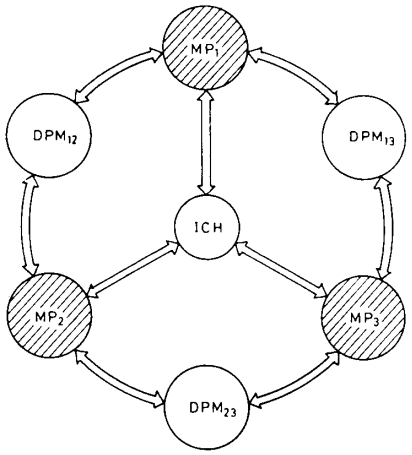
For the case of one disturbing variable, (1) and (2) only apply, and the $b_{ji}(z)$ coefficients in (2) are constants. If correction for nonlinearity only is required, then, (1) with constant a_i coefficients should be used. In general, the range of polynomial coefficients in (1)-(3) can be so large that the use of floating-point arithmetic becomes necessary. Also, in practice, x, y, and z values should be properly scaled before proceeding with the computation.

III. DUAL AND TRIPLE MICROPROCESSOR SYSTEMS

The proposed triple microprocessor system architecture for transducer output signal processing is shown in Fig. 1. For a dual microprocessor system, the microprocessor 3 (MP_3) and the associated hardware are eliminated. Under normal operation, simultaneous access to the same DPM location, which results in access conflict, is not allowed, and simultaneous sharing of data is achieved by data duplication, and the passing of results is performed by means of predefined signaling protocols. The interprocessor communication hardware consists of 8-bit token registers for information token passing, tri-state buffers, and interrupt flip-flops for interprocessor signaling.

Suppose microprocessor 2 (MP_2) wants to signal microprocessor 1 (MP_1), then, MP_2 loads an appropriate token into the token register of MP_1. This action, simultaneously, causes the interrupt line of MP_1 to be activated. In response to the interrupt, MP_1 reads the token, simultaneously deactivating the interrupt signal. This completes the interprocessor signaling protocol.

In the triple microprocessor system, mutually exclusive access to the DPM is permitted in terms of memory segments of fixed size. The size and the number of memory segments must be fixed up depending upon the application so that at no time a microprocessor has to wait for long periods for the availability of a memory segment. In applications wherein a microprocessor has to pass a large amount of common data to the other two microprocessors, much time is wasted in duplicate writing of common data. To avoid this, memory segments called blackboard memory segments (BMS) are identified. Each microprocessor MP_i is allotted a BMS_i in the DPM



MP1 - MP3 : Microprocessors
DPM12 - DPM23 : Dual - Port Memories
ICH : Interprocessor Communication Hardware

Fig. 1. Triple microprocessor system architecture.

TABLE I
DUAL MICROPROCESSOR TASK ALLOCATION CONSIDERING ONE DISTURBING VARIABLE

COMPUTATION PHASE	MP_1 COMPUTATION	MP_2 COMPUTATION
Case 1 : Odd n		
1	$a_0, a_1, \ldots a_{(n-1)/2}$	$a_{(n+1)/2}, a_{(n+3)/2}, \ldots a_n$
2	$f_1 = a_0 + a_1 x + \ldots a_{i-1} x^{i-1}$	$f_2 = a_i x^i + a_{i+1} x^{i+1} + \ldots a_n x^n$
3	$f = f_1 + f_2$	-
Case 2 : Even n		
1	$a_1, a_2, \ldots a_{n/2}$	$a_{n/2+1}, a_{n/2+2}, \ldots a_n$
2	$a_0 = b_{00} + b_{10} y + \ldots b_{m0} y^m$ $f_1 = a_0 + a_1 x + \ldots a_{i-1} x^{i-1}$	$f_2 = a_i x^i + a_{i+1} x^{i+1} + \ldots a_n x^n$
3	$f = f_1 + f_2$	-

modules to which it is connected. For example, MP_1 has BMS_1 which corresponds to identical memory blocks in DPM_{12} and DPM_{13}. The address decoding and read-write control logic for MP_1 with respect to DPM_{12} and DPM_{13} is so designed that whenever MP_1 writes into BMS_1, the data is written into both DPM_{12} and DPM_{13}. The use of BMS results in considerable time saving in applications that demand short real-time response time.

IV. Computation Cycle and Task Allocation

Basically, a computation cycle consists of the following three steps.

1) The microprocessors acquire values corresponding to x, y, and z through the ADC's interfaced to them, and after necessary scaling, store them in the DPM's. MP_1 after receiving signals from MP_2 and MP_3, stores data necessary for MP_2 and MP_3 in the corresponding DPM's, and signals MP_2 and MP_3 to start the computation.

2) The three microprocessors compute, concurrently, the polynomial coefficients and part of (1), performing interprocessor signaling whenever necessary.

3) MP_1 computes the value of f using the results produced by the three microprocessors.

Under task allocation, the computational load of each microprocessor, and the order of computation is determined. The most optimal task allocation depends on the relative values of m, n, and p in (1)–(3). For illustration, shown in Table I is the task allocation for the dual microprocessor system for the case of one disturbing variable. In this table, $a_i(y)$ is abbreviated as a_i. The choice of i, in the table, is made as follows. Let a = floating-point multiplication time, b = floating-point addition time, k = largest integer $\leq \log_2 i$, and h = number of 1's in the binary representation of i. Then, the value of i for odd n is chosen so that the value of the expression

$$E1 = \max\left\{\left[(n-i)(a+b) + (k+h)a\right], (i-1)(a+b)\right\} \tag{4}$$

is a minimum. Similarly, for even n, the value of i is chosen so that the value of the expression

$$E2 = \max\left\{\left[(n-i)(a+b) + (k+h)a\right] \left[m(a+b) + (i-1)(a+b)\right]\right\} \tag{5}$$

is a minimum. In the above expressions, k and h appear because, MP_2 computes x^i by first finding terms of the form x^w, where w is a power of 2, by repeated multiplications of the form $p := p * p$, and then multiplying the selected terms to make x^i.

The task allocation for the dual microprocessor system for the two disturbing variables, and for the triple microprocessor system is also made so that the overall computational load distribution among the microprocessors is uniform, and the computation time is minimized.

V. Analytical Evaluation of Processing Speed

The analytical evaluation of speed of computation for the dual and triple microprocessor systems, with respect to a given task allocation, is carried out by individually finding analytical expressions for the computation time for each phase of computation for each microprocessor, and the expression for the least time taken to complete the cycle of computations is determined. For the task allocation of Table I, the dual microprocessor computation time, T_d, is given by the following expressions:

Case 1: n Odd

$$T_d = \max(T_1, T_2) + T_s \tag{6}$$

where

$$T_1 = (mn/2 + m/2 + i - 1)a + (mn/2 + m/2 + i)b \tag{7}$$

$$T_2 = (mn/2 + m/2 + n - i + k + h)a + (mn/2 + m/2 + n - i + 1)b \tag{8}$$

and,

T_s = interprocessor signaling time.

Case 2: n Even

$$T_d = \max(T_3, T_4) + T_s \tag{9}$$

where

$$T_3 = (mn/2 + m + i - 1)a + (mn/2 + m + i)b \tag{10}$$

$$T_4 = (mn/2 + n - i + k + h)a + (mn/2 + n - i + 1)b. \tag{11}$$

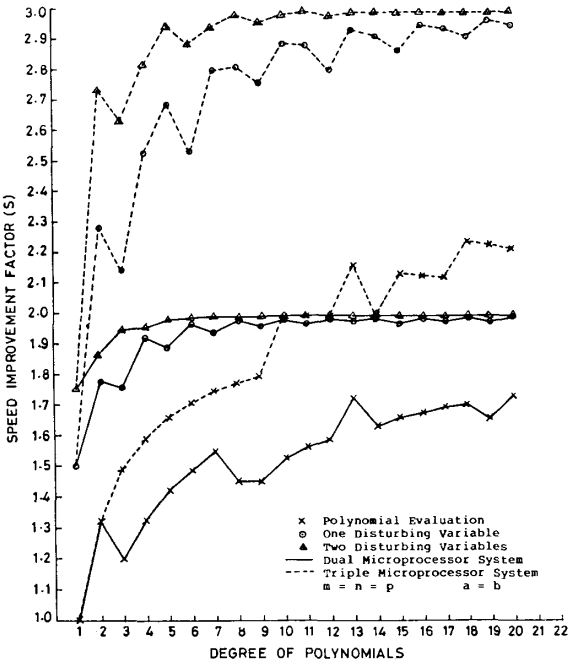


Fig. 2. Speed improvement using dual and triple microprocessor systems.

It is estimated that, for 8085-microprocessor-based systems operating at 3 MHz, and for software implementation of floating-point operations, the worst-case time for the completion of signaling protocol once is of the order of 0.15 times b, and for the transducer output processing task under consideration, interprocessor signaling is performed only two times. Therefore, as we are interested in viewing the general trend of speed improvement by the dual and triple microprocessor systems, T_s is negligible in (6) and (9).

The ratio of the computation time for a single microprocessor system to the computation time for the dual (triple) microprocessor system, defined here as the speed improvement factor (s), is now evaluated and used as a measure of the performance of the dual and triple microprocessor systems. Fig. 2 shows the plotted values of s, obtained analytically, for the dual and triple microprocessor systems with respect to the tasks of polynomial evaluation, and transducer output signal processing under the cases of one and two disturbing variables. It is clear from this figure that significant processing speed improvement is possible by the use of the dual and triple microprocessor systems.

VI. Conclusion

A technique to correct transducer nonlinearities and disturbing variable effects using dual and triple microprocessor systems has been described. In the architecture of the triple microprocessor system, a new concept of BMS for passing a large amount of common data among the microprocessors has been introduced. The results of analytical evaluation have shown significant processing speed improvement over a single microprocessor-based implementation.

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