STUDY OF HVDC CONTROLS THROUGH EFFICIENT DYNAMIC DIGITAL SIMULATION OF CONVERTERS

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INDIAABSTRACT

This paper describes the converter model for 6/12 pulse operation and presents its applications for the study of the performance of converter controls. The simulation is simplified by representing the converter as a time varying equivalent circuit on the DC side which is derived on the basis of graph theory. Elimination of the need to store connection matrices and an efficient way of generating the converter equations are further innovations introduced here.

The converter control based on digital techniques has been considered along with representation of voltage dependent current order limit. The results of various test simulations considering both weak and strong ac system characteristics are represented to illustrate the simulation capability.

Keywords : HVdc, Digital Simulation, Converter, Digital Control

INTRODUCTION

As the applications of the HVdc systems grow, the need for a detailed investigation of the potential problems increases. As an example, one could consider the problems of system operation with dc links feeding weak ac systems. There are various aspects of the problem such as voltage dependent current order limit, var compensation etc. But it is well recognized that a suitable converter control is the most significant factor in the optimum and secure operation of the system.

While converter control and optimization are usually carried out using HVdc simulators, the reduced cost and increased availability of digital computers makes it attractive to use digital simulation. The simulation of HVdc converters is characterized by the fact that the network to be solved changes with the commencement and cessation of valve conduction. To handle this time varying topology of the network various approaches have been reported [1-7]. The system models thus derived are well suited for dynamic studies in the frequency range upto 1kHz which is appropriate to investigate the converter control response. However for high frequency transient studies, EMTF type simulation is necessary [8].

This paper describes a converter model for 6/12 pulse operation and presents its application for the study of performance of converter controls. The simulation is simplified by considering a time varying equivalent circuit on the dc side, which is derived on the basis of graph theory. Elimination of the need to store connection matrices and a fast and efficient way of generating the converter equations are further innovations introduced here. For the simulation of the

HVdc system the approach employed is to model each component separately and in a modular fashion. These models are interconnected using appropriate interface variables. The control of converters based on digital scheme has been considered along with voltage dependent current order limit (VDCOL). Results for a two terminal HVdc system under normal operation and a few abnormal conditions like severe AC side voltage dips, are presented primarily to illustrate the capability of the simulation method.

CONVERTER MODEL

A three phase bridge converter system is shown in Fig. 1. This includes the resistances and inductances of the converter transformer (R_a, R_b, R_c and L_a, L_b, L_c) and dc smoothing reactor (R_d, L_d). Both the ac and dc voltage sources are not constant and are actually output of ac and dc network models. The effect of the converter on the ac and dc networks is represented by the injection of currents into the respective network. The graph of the converter system is shown in Fig. 2. In total there are γ elements, of which the first 6 represent the valves. Elements 7 and γ correspond to the equivalent circuit representation of the ac system feeding the converter [9]. The element 8 includes the series combination of R_d, L_d and V_c . From the graph it is clear that there are 4 tree branches and 5 links. A tree is so chosen such that it includes elements 7, 9 and any two of the conducting valves. Consequently, the tree branches are partitioned into two sets, one set (T_1) consisting of elements 7 and 9 and the other (T_2) consisting of the two conducting valves. The link elements are partitioned into 3 sets. The first set (L_1) corresponds to element 8 and the other two sets (L_2 and L_3) consist of conducting and non-conducting valves in the links respectively.

The voltage (v) across and current (i) through the branch and link elements are related as

$$[\underline{i}_{T1} \ \underline{i}_{T2}]^t = -B_L [\underline{i}_{L1} \ \underline{i}_{L2} \ \underline{i}_{L3}]^t \quad (1)$$

$$[\underline{v}_{L1} \ \underline{v}_{L2} \ \underline{v}_{L3}]^t = B_L^t [\underline{v}_{T1} \ \underline{v}_{T2}]^t \quad (2)$$

where, t denotes the transpose and B_L is the fundamental cutset matrix corresponding to link elements. Based on the subdivision of the set of branch and link elements described earlier, B_L can be partitioned as

$$[B_L] = \begin{matrix} & \begin{matrix} L_1 & L_2 & L_3 \end{matrix} \\ \begin{matrix} T_1 \\ T_2 \end{matrix} & \begin{bmatrix} B_{L11} & B_{L12} & B_{L13} \\ B_{L21} & B_{L22} & B_{L23} \end{bmatrix} \end{matrix}$$

For elements 7 and 9, the circuit equation is

$$\underline{v}_{T1} = Z \underline{i}_{T1} + \underline{e} \quad (3)$$

and that for element 8

$$\underline{v}_{L1} = (R_d + L_d p) \underline{i}_{L1} + V_c \quad (4)$$

where, $\underline{v}_{T1} = [v_7 \ v_9]^t$; $\underline{i}_{T1} = [i_7 \ i_9]^t$; $Z = R(1+cp)$

$\underline{e} = [(e_c - e_b) \ (e_a - e_b)]$; $c = L_a/R_a = L_b/R_b = L_c/R_c$

$$p \triangleq d/dt ; \quad [R] = \begin{vmatrix} R_a + R_b & & \\ & R_c + R_b & \end{vmatrix}$$

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FIG.1 CONVERTER SYSTEM

FIG.3 6 PULSE EQUIVALENT CIRCUIT

FIG.2 GRAPH OF FIG.1

FIG.4 12PULSE EQUIVALENT CIRCUIT

FIG.5 VDCOL CHARACTERISTICS

c , the time constant of transformer impedance is assumed to be the same in all the phases. Assuming the valves to be ideal switches with zero forward impedance and infinite reverse impedance, the elements 1 to 6 are governed by the following equations

$$v_k = 0, \quad k \in K; \text{ set of conducting valves} \quad (5)$$

$$i_m = 0, \quad m \in L_2; \text{ set of nonconducting valves}$$

It is, therefore, evident that $i_{L3} = 0$; $v_{T2} = 0$; $v_{L2} = 0$

Substituting this in (1) to (4) gives

$$i_{T2} = -B_{L21} i_{L1} - B_{L22} i_{L2} \quad (6)$$

$$v_{L3} = (B_{L13})^t v_{T1} \quad (7)$$

$$v_{L1} = -R_1(1+cp) i_{L1} - R_2(1+cp) i_{L2} + (B_{L11})^t e \quad (8)$$

$$(1+cp) i_{L2} = -R_4^{-1} R_3 (1+cp) i_{L1} + R_4^{-1} (B_{L12})^t e \quad (9)$$

$$\text{where, } R_1 = (B_{L11})^t R B_{L11}; \quad R_2 = (B_{L11})^t R B_{L12}$$

$$R_3 = (B_{L12})^t R B_{L11}; \quad R_4 = (B_{L12})^t R B_{L12}$$

$$\text{Eqn. (8) can be further simplified by using (9) to get} \quad v_{L1} = -z_{eq} i_{L1} + e_{eq} \quad (10)$$

$$\text{where, } z_{eq} = (R_1 - R_2 R_4^{-1} R_3) (1+cp) = r_{eq} (1+cp)$$

$$e_{eq} = [(B_{L11})^t - R_2 R_4^{-1} (B_{L12})^t] e_{11}$$

v_r is the voltage across element 8 which is the dc voltage before smoothing reactor of the bridge. Eqn. (10) can be viewed as an equation for an equivalent circuit having voltage source e_{eq} behind an impedance z_{eq} . The complete model of a 6 pulse converter is, thus, as shown in Fig.3. The dynamic equation which gives the dc current (i_{L1}) of the converter is

$$p i_{L1} = -(R_t/L_t) i_{L1} + (e_{eq} - v_c)/L_t \quad (11)$$

$$\text{where, } R_t = r_{eq} + R_d; \quad L_t = c r_{eq} + L_d$$

In addition to (11), (9) has to be solved for the case of three and four valve conduction mode. The currents in the conducting valves in the branches and links are given by (6) and (9) respectively, whereas the voltage across the non-conducting valves is given by (7).

Twelve Pulse Converter Representation

A 12 pulse converter comprises of two six pulse bridges connected in series with one six pulse converter fed by a wye/wye transformer and the other by a delta / wye transformer so as to produce a 30° phase shift between the corresponding phase voltages. Each 6 pulse bridge can be represented by the equivalent circuit of Fig.3 (eqn.10) and the series connection of two such circuits with R_d , L_d and V_c gives the model for 12 pulse converter as shown in Fig.4. The circuit of Fig.4 can be reduced to the form of Fig.3 with the equivalent circuit parameters given by

$$E_{eq} = \sum_{j=1}^2 e_{eqj}; \quad R_{eq} = \sum_{j=1}^2 r_{eqj}; \quad L_{eq} = \sum_{j=1}^2 c_j r_{eqj}$$

where e_{eqj} and r_{eqj} are equivalent circuit parameters

for the bridge j . The dc current equation for the 12 pulse converter is identical to (11) with the following substitution

$$R_t = R_{eq} + R_d; \quad L_t = L_{eq} + L_d; \quad e_{eq} = E_{eq}$$

The resulting dynamic equation is solved at every integration time step for the dc current of 12 pulse converter. In addition, (9) is solved for each of the 6 pulse bridges which constitute the 12 pulse converter, to obtain the current through the

conducting valves not included in the tree. The change in the status of valves in the link can be considered by rearranging the columns of matrix B_L . The matrix B_L has to be changed whenever any valve included in the tree ceases to conduct.

The six pulse converter model presented here is conceptually simple and as illustrated can be easily extended to represent converters having series connected 6 pulse bridges. The number of state equations per converter terminal will vary depending on the number of conducting valves per bridge (N_i) and is given by $1 + \sum_{i=1}^b (N_i - 2)$, where, b is the number of bridges per converter terminal. The model is flexible enough to include a) forward voltage drop across a valve, b) unequal time constants of the transformer phases and c) grading and damping circuit across a valve.

CONTROL REPRESENTATION

HVdc converters are generally equipped with constant current and constant extinction angle (CEA) controllers. Analog techniques have traditionally been used for this purpose. However, digital techniques have become quite popular because of the flexibility, accuracy and reliability. The control of the converters considered here is based on the digital techniques [10,11]. The firing scheme is essentially an Equidistant Pulse Control Scheme with Pulse Frequency Control. The interval between two successive firing instants, called the Inter Firing Period (IFP), is calculated as

$$\text{IFP} = 60^\circ + Q \quad (12)$$

where, Q is the firing correction obtained as the output of either the current or extinction angle controllers. In steady state, $Q = 0$ and firing takes place at every 60° interval for a six pulse converter. For a 12 pulse converter, both the bridges have an independent calculation of their respective IFP's and, in steady state, firing occurs alternately in each bridge spaced apart by 30° . In case of current controller, Q is determined as

$$Q = K E_c \quad (13)$$

where, K is the gain and E_c is the control signal obtained as

$$E_c = K_1(i_d - I_{ref}) + K_2 \cdot di_d/dt \quad (14)$$

In case of CEA operation, the controller action takes place through two completely independent loops, Inverter Safety Control (ISC) and Inverter Optimum Control (IOC). ISC acts when the measured extinction angle (γ) is less than reference and it can only reduce the firing angle. The firing correction is given by

$$Q = K_3 (\gamma - \gamma_{ref}) \quad (15)$$

IOC attempts to bring back the system to its optimum operating condition. However, it acts only when safety is guaranteed. To facilitate this, a record is kept of the measured extinction angles in a cycle and if the minimum of these measured values is greater than the γ reference, the firing angle is increased. Thus, the IOC operates only once per cycle and the firing correction is

$$Q = K (\gamma_{\min} - \gamma_{ref}) \quad (16)$$

If $\gamma \geq \gamma_{ref}$ in ISC and $\gamma_{\min} \leq \gamma_{ref}$ in IOC, $Q=0$. In (14) to (16), K_1 to K_4 are the controller gains whose values are judiciously chosen [11].

The rectifier control comprises of both minimum alpha and constant current control. For minimum alpha operation the valve conduction is prevented till the voltage across it rises to a required level. For the constant current control, Q is derived at every time step based on the converter dc current and its

derivative (eqn. 11). This is used for calculating IFP and the valve is fired when the elapsed time after the last firing instant equals IFP. This procedure offers the distinct advantage that the firing pulse is generated based on the latest available sample of the control variable. However, in [10], the use of the control variable information available immediately after each firing is recommended. In the above firing scheme with pulse frequency control, as the phase of the firing continues to increase, it may cause the rectifier to move into the inverter region of operation. In order to avoid this, or worse still, a commutation failure at rectifier, an end stop is incorporated at alpha equal to 120° . The exact mechanism is to fire valve i immediately after the commutation voltage of valve $i+2$ goes positive.

For the implementation of CEA control, the extinction angle is measured as the time interval between current zero instant and the instant at which the voltage across the valve goes positive again. The instant is actually measured as the commutation voltage zero crossing instant of the valve which has ceased conduction prior to the valve for which extinction angle is being measured. This approach has the advantage that even if a valve continues to conduct due to fault, say commutation failure, a voltage zero crossing instant would still be obtained and the occurrence of the fault will be detected. For example, in the converter circuit of Fig. 1, suppose valves 2 and 3 are conducting and valve 4 is fired. In normal operation this would commutate valve 2, the voltage across which will now be $(e_a - e_c)$. This voltage is same as the commutation voltage for valve 1. Now if valve 4 fails to commutate valve 2, the latter continues to conduct and the voltage across it continues to be zero. However, the commutation voltage for valve 1 would still give a zero crossing instant thereby indicating the occurrence of a fault. But as the valve 2 current does not go to zero, extinction angle cannot be measured.

At the inverter, the dc current is also continuously monitored and the operation is changed to constant current control mode if the dc current falls below the reference setting. The reverse transition from constant current to CEA control takes place when extinction angle for any valve is less than the reference value.

VDCOL Representation : As a part of the converter control system, voltage dependent current order limit has also been considered to modify the current reference setting as a function of dc voltage during fault. A typical VDCOL characteristic is shown in Fig. 5. The characteristic is represented as series of points which are then connected through straight lines. VDCOL does not operate unless the converter is operating in constant current control mode. Once operation in constant control mode begins, the VDCOL samples the dc voltage after the smoothing reactor through a first order time delay element. When this sampled value reaches a value below that specified by the first corner point (C and O in Fig.5), the VDCOL operation begins and current reference at each subsequent instant is calculated by interpolating between the corner points (C,D and O,P). The increase and decrease in current setting is respectively governed by T_{UP} and T_{DN} time constants of the delay element.

AC AND DC NETWORK MODEL

A three phase schematic representation of the ac system and harmonic filters, associated with a particular terminal is shown in Fig. 6. The ac system is represented by ideal voltage sources (e_1, e_2, e_3) behind a T-equivalent circuit of the ac network [12]. F denotes tuned filters for 5th, 7th, 11th and 13th harmonics along with a second order high pass filter.

ceases conduction. The exact instant of cessation is determined by linear interpolation using the valve current measurement. At each integration time step, the converter state is checked and the dynamic equations corresponding to the various subsystems are solved using modified Euler's integration method. Some of the salient features of the program are :

- (1) Both 6 pulse and 12 pulse operation of converter can be simulated.
- (2) At present, there are three choices of converter controls viz., constant alpha, current control and CEA control. The firing pulse generation scheme is based on IPC and EPC (analog and digital techniques).
- (3) The simulation can begin either from zero initial condition or from steady state operating condition derived using AC/DC load flow.

RESULTS OF SIMULATION

various test simulations of a two terminal dc

FIG 8 12 PULSE STEADY WAVEFORM WITH AC SYSTEM SCR 15 AT RECTIFIER SCR 3 AT INVERTER

FIG 9 STEADY STATE AC WAVEFORMS AT INVERTER SCR 3

FIG. 10 CURRENT WAVEFORM ON RECOVERY FROM COMMUTATION FAILURE

FIG. 11 99%, SINGLE PHASE, 1 CYCLE DIP AT INVERTER (no d/dt)

FIG. 12 99%, SINGLE PHASE, 1 CYCLE DIP AT INVERTER (d/dt)

FIG. 13 50%, 3 PHASE, 10 CYCLE DIP AT 12 PULSE INVERTER.

link are carried out both with and without detailed ac system representation to investigate the system response and control performance following a disturbance. The system parameters and operating conditions are given in the Appendix.

Fig. 8 shows the steady state waveforms for a two terminal dc system with 12 pulse converter operation. The rectifier end ac system SCR is 15 and inverter end SCR is 3. Fig. 9 shows the resulting waveforms of the ac system voltages and currents to demonstrate the satisfactory operation of the system with weak ac system at the inverter.

Transient Response with Strong AC System

Reduction in the ac voltage at the inverter end has a predominant effect on the performance of the HVdc link. To investigate the effectiveness of the control under such conditions, results of the various test simulations are given in Figs. 10 to 12. At both

FIG 14 20%, SINGLE PHASE, 10 CYCLE DIP AT INVERTER
SCR 15 at Rectifier, SCR 3 at Inverter

FIG 15 20%, SINGLE PHASE, 10 CYCLE DIP AT INVERTER
SCR 15 at Rectifier, SCR 15 at Inverter

FIG 16 50%, 3 PHASE, 5 CYCLE DIP AT RECTIFIER
SCR 15 at Rectifier, SCR 3 at Inverter

FIG 17 50%, 3 PHASE, 5 CYCLE DIP AT RECTIFIER
SCR 15 at Rectifier, SCR 3 at Inverter

ends of the dc link, the ac system is assumed to be strong and hence its detailed representation is ignored. The six pulse converter operation is considered. Fig. 10 shows the current waveforms on recovery from commutation failure following a 20% dip in phase A voltage for 10 cycles. The first and the latest sample refer to the sampling of the dc current immediately following the previous firing [10] and the latest possible instant respectively. It is seen that inclusion of a derivative term in current control (eqn. 14) leads to a substantial reduction in current oscillations. Advancing the sampling instant to the latest possible instant causes a further improvement. To further illustrate the effect of the derivative term in the current control, the computed waveforms of the rectifier and inverter end average dc voltage and current (average taken over every 30°) following a single phase voltage collapse (99% dip) at the inverter for one cycle, are shown in Figs. 11 and 12.

With a view to demonstrate the versatile nature of the control scheme and illustrate the program

capability in simulating 12 pulse converter operation, a 50%, 3 phase, 10 cycle ac voltage dip at inverter end has been considered. The results are shown in Fig. 13. As is evident the control action helps the system to recover rapidly and the duration of the short circuit is limited to only 3 cycles. In 12 pulse operation the dc voltage level is higher and so, the severity of the fault is also increased. In this case study, a 12th harmonic double tuned filter has also been considered on the dc side at both ends.

Transient Response with Weak AC System

The effectiveness of the control system can be thoroughly examined only by detailed representation of the ac system characteristics. In the following studies, two different ac system characteristics having SCR 15 and 3 have been considered. The various voltage disturbance cases simulated are

- 20% dip in phase A voltage at inverter for 10 cycles. AC System SCR = 15 at rectifier and 3 at inverter.
- 20% dip in phase A voltage at inverter for 10 cycles. AC system SCR = 15 at both rectifier and inverter.
- 50% dip in all the 3 phases at rectifier for 5 cycles. AC system SCR = 15 at rectifier and 3 at inverter. VDCOL not considered.
- Same as case (c) but with VDCOL at both ends having characteristics as given in Appendix.

The results for the cases (a) to (d) are shown in Figs. 14 to 17. From the comparison of various responses (cases a, b) it is observed that the recovery in case of strong ac system (SCR 15) is much faster than for weak ac system (SCR 3) which has many successive commutation failures and the system does not recover until the voltage dip is removed. It may be noticed in Fig. 14 that rectifier voltage goes negative which is indicative of its operation in the inverter region. The rectifier, however, is equipped with end stop limit on its firing angle ($=120^\circ$).

From responses shown in Figs. 16 and 17 (cases c and d), it is evident that the introduction of VDCOL causes a drastic improvement in the performance and the current peak is considerably reduced causing smaller oscillations and quicker restoration of steady operating conditions. Also, presence of VDCOL avoids undesirable excursion of rectifier into inverter region and vice versa.

The various case studies primarily illustrate the capability of the program in properly simulating the behaviour of HVdc system. As an indication of the program efficiency, it may be mentioned that to simulate 1 ms of real time, the program takes around 0.6 to 1.0 sec of computation time on MicroVAX II computer depending upon the details considered.

CONCLUSIONS

The converter equivalent circuit based on graph theory approach is developed. The converter model has a modular structure and hence can be used to simulate a converter terminal with any number of 6 pulse/12 pulse bridges in series. Elimination of the need to store connection matrices and a fast and efficient way of generating the converter equations are some of the advantages of this method. Based on this converter model, a computer program has been developed incorporating the detailed representation of the ac system, digital converter control scheme and voltage dependent current order limit. Results of various test simulations are presented to illustrate the program capability for studying the controller response under severe disturbances.

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APPENDIX SYSTEM DATA

Rated power of DC link = 240 MW for 12 pulse and 120 MW for 6 pulse system. AC system frequency = 50 Hz.

Converter Transformer :

Resistance $R_{C1} = R_{C2} = 0.5$ Ohms

Commutating Reactance $X_{C1} = X_{C2} = 6.283$ Ohms

Smoothing Reactor :

Resistance $R_{d1} = R_{d2} = 0.1$ Ohm, Inductance $L_{d1} = L_{d2} = 1.0$ H

Transmission Line :

Resistance = 8.64 Ohms, Total inductance = 0.50148 H

Total capacitance = 54.1645 micro farads

Digital controller (adapted from ref. [11]) :

a) Constant Current Controller :

$K_1 = 0.4$ rad/p.u. current, $K_2 = 0.4$ rad²/p.u. current

b) CEA Controller : $K_3 = 1.0$; $K_4 = 0.25$

AC system Details :

RMS AC Voltage (L-N) : $E_1 = 42.78$ kV, $E_2 = 38.51$ kV

Valve turn off time = 3 degrees

AC system impedance angle = 85 degrees

VDCOL Time Constants :

Rectifier : $T_{DN} = 0.00008$ sec; $T_{UP} = 0.03$ sec

Inverter : $T_{DN} = 0.00008$ sec; $T_{UP} = 0.04$ sec

VDCOL Characteristics (Fig. 5) :

Rectifier : C = (1.0, 0.2), D = (0.4, 0.2)

Inverter : O = (0.9, 0.6), P = (0.3, 0.2)

DC Filter Parameters :

R = 15.0 Ohms, $L_1 = 0.084$ mH, $L_2 = 246.5$ mH

$C_1 = 0.801$ micro farads, $C_2 = 2.31$ micro farads

Operating conditions:

a) 12 pulse : $I_{d1} = I_{d2} = 1000$ Amps
 $\gamma_{min} = 5^\circ$, $\gamma_c = 10^\circ$, $\alpha_1 = 21.46^\circ$, $\alpha_2 = 148.39^\circ$

b) 6 pulse : $I_{d1} = I_{d2} = 1000$ Amps
 $\gamma_{min} = 5^\circ$, $\gamma_c = 10^\circ$, $\alpha_1 = 12.88^\circ$, $\alpha_2 = 148.38^\circ$

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BIOGRAPHY

K.R.Padiyar received the BE degree in Electrical Engineering from Poona University in 1962, ME and Ph.D degrees from I.I.Sc. Bangalore and University of Waterloo in 1964 and 1972 respectively.

He worked with the Department of Electrical Engineering, IIT Kanpur initially as Assistant Professor (1976-1980) and later as Professor (1980-July 1987). Since August 1987 he has joined Indian Institute of Science Bangalore where he is currently Professor of Electrical Engineering. His teaching and research interests include HVdc Transmission, Reliability, System Stability and Control.

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Discussion

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The authors present an interesting paper about the simulation of a converter in a digital computer program and how the program is used for the study of the performance of the converter control.

However, as a number of different digital computer programs for the simulations of converters have been presented during the last years, it should be of great value, if the authors also could give some comparison to other similar computer simulations e.g. comparisons with simulations in the EMTP and the EMTDC programs.

With regard to the simulation of the control it must be stressed that the performed simulation by necessary is very much simplified. The results have because of that to be treated with some caution. The presented control principles give basically a non-linear system, as the adjustment in delay angle at each firing instant is proportional to the control signal. By including a derivative term in the control signal a proportional term will also be included in the current control loop, which explains that the constant K_2 has to be non-zero in order to obtain an acceptable damping of the control response.

It would be of interest to know if the authors have made some comparisons with other computer programs, if it is planned to further develop the program and if some comparisons have been made with oscillograms from real HVDC plants or from HVDC simulator test

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We wish to thank Mr. Åke Ekstrom for the interest shown in the paper. He has raised some pertinent points to which our response is given below.

Although there are several computer programs that have been reported in the literature for converter simulation, most of them are based on the modifications of EMIP which was primarily developed for the study of network transients in AC systems. While there are some advantages in having a general purpose program, with detailed subsystem models, which can be used for all types of studies, we feel that this approach is computationally more complex and inefficient. The general philosophy of simulation of

a complex system should be, in our opinion, to use simplifications wherever possible without sacrificing accuracy. Actually, this philosophy is already being used in AC system simulation. For example, although EMIP can be used for transient stability studies, a separate program, where network transients are neglected is used.

The major objective of the simulation program reported in the paper is to carry out studies on controller performance under various system conditions. We believe that there is a need for a special purpose program which can supplement the HVDC simulator (a physical model). The major emphasis in our paper is the use of graph-theoretic analysis for the development of converter model. The concept of an equivalent circuit given in the paper is, in our opinion, more efficient than the time-varying impedance model of a valve used in EMIP or EMTDC. As a matter of fact, this representation of a valve can lead to numerical problems unless snubber circuits are represented (although they don't play any role in the determination of the controller response).

While it is true that the controller models given in the paper are simplistic, this has the advantage of highlighting the factors that determine the response for different types of disturbances. As the example considered in the paper is not based on a specific DC link, the optimization of the controller parameter is not attempted. In this context, we would like to stress the importance of establishing a benchmark model and standardization of DC link controller blocks which will then enable the various computer programs to be tested in terms of accuracy, computing times, etc. In the absence of such test systems, the comparison of the different programs is not meaningful. However, we have also developed a simulation program along the lines of EMIP for comparison. We hope to publish the comparisons between different modelling approaches in future. Also with the availability of a HVDC simulator and the commissioning of HVDC projects in India, we intend to do detailed comparisons with the digital programs and updating of controller models.

Finally, we wish to state that the development of a reliable and fast simulation tool in the form of an inexpensive computer program, will remove much of the mystery surrounding the HVDC controllers and stimulate innovations in control strategies which can benefit the utilities who wish to optimize the performance of HVDC systems.

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