

# Ultracapacitor Based Ride Through System for Control Power Supplies in High Power Converters

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**Abstract**—High power converters are used in variable speed induction motor drive applications. Riding through a short term power supply glitch is becoming an important requirement in these power converters. The power converter uses a large number of control circuit boards for its operation. The control power supply need to ensure that any glitch in the grid side does not affect any of these control circuit boards. A power supply failure of these control cards results in shut down of the entire system. The paper discusses the ride through system developed to overcome voltage sags and short duration outages at the power supply terminals of the control cards in these converters. A 240VA non-isolated, bi-directional buck-boost converter has been designed to be used along with a stack of ultracapacitors to achieve the same. A micro-controller based digital control platform made use of to achieve the control objective. The design of the ultracapacitor stack and the bidirectional converter is described the performance of the experimental set-up is evaluated.

## I. INTRODUCTION

The power line disturbances like voltage sags and blackouts affect the continuous process industries to a great extent, the severity being dependent on the magnitude and duration of the sag. Faults lasting even less than 0.5s can have detrimental effects on the production. Each industrial equipment reacts to voltage sag in different ways [2]. A voltage sag is defined as a momentary dip in voltage - below 10 % lasting from a few cycles (10ms) to 150 cycles (0.3s) [3]. Voltage sags cause disruption of services but do not cause damage to sensitive loads. On the other hand, the voltage swells, which may exist cause damage but a limited one does not disrupt sensitive loads. More than 62% of the disturbances are due to voltage sags with duration less than half a second [3]. A severe voltage sag is one where voltage falls below 85 %. Voltage sags are caused by faults within the system, starting currents of motor.

In the induction motor drive shown in Fig. 1, voltage sags on the control power supply feeding the control DSP, gate drive cards, current and voltage sensing cards might cause the entire motor drive system to shutdown. So a ride-through system consisting of DC-DC converter, an energy source has been designed to overcome the effect of these voltage sags and momentary black-outs.

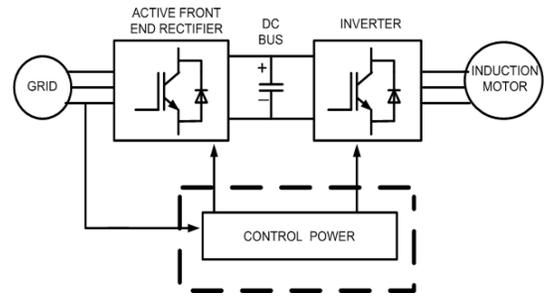


Fig. 1. Block diagram of an induction motor drive.

### A. The Ride Through System

The ride through system consists of a stack of ultracapacitors charging and discharging through a bi-directional buck-boost converter. The system has been designed to provide back-up over a period of 10s for a load of 78W. The ride through system is shown in Fig. 2. The main power to the control cards is fed through the PFC boost converter circuit, consisting of a transformer-rectifier system in cascade with boost converter to make the input current continuous, feeding the bi-directional converter and the sensing cards in parallel. The ultracapacitor stack is charged through the converter at

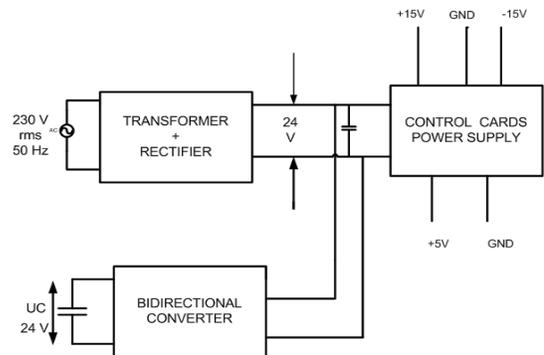


Fig. 2. Block diagram of the ride through system.

constant current when the main power is available, and during surges/blackouts the capacitor bank discharges through the

boost converter providing a constant voltage to the output.

## II. ULTRACAPACITORS - MODELLING, DESIGN AND SIZING

Ultracapacitors store energy in electrostatic form unlike batteries which store energy in electrochemical form. The result being faster charging of ultracapacitors and longer cycle life. These ultracapacitors differ from ordinary electrolytic capacitors with respect to their constructional features. A Ragone's plot [7] shows distinctly the applications of the various energy storage devices. The ultracapacitors have power densities greater than batteries but lesser than electrolytic capacitors, and energy densities greater than electrolytic capacitors but lesser than batteries and fuelcells. Literature study [4] reveals that ultracapacitors find applications best in starting of automobiles, trapping energy during regenerative braking of motors and some pulsed power applications where very high power is required in short time with substantial energy. In such applications drawing high power from batteries shortens its life and electrolytic capacitors cannot supply energy for more than few milliseconds without compromising on cost and volume. Another advantage of ultracapacitors is its large number of charge/discharge cycles of over 1,00,000; the number being slightly around 1000 for lead-acid batteries, making ultracapacitors more suitable for applications involving riding through voltage sags and short duration blackouts as the frequency of occurrence of these faults is high, potentially occurring almost one every hour.

An ultracapacitor consists of two active excited porous carbon electrodes. The active excitation increases the diameter of pores on the surface of carbon electrode, aiding the absorption of more ions resulting in very high capacitance per unit volume. Electrolyte acts as the ionic conductor flowing between the plates. The very high capacitance is due to the small thickness of the layer separating the charges. The electrolyte type and the number of pores determine the typical voltage withstand ability of a single ultracapacitor cell. The electrolytes used can be both aqueous and non-aqueous. The decomposition voltage of aqueous electrolytes like sulphuric acid is about 1.2V and that of the non-aqueous electrolytes are 4V [5]. Typical capacitance of an ultracapacitor varies from a few to 3000 Farads.

### A. Design of the Ultracapacitor Stack for the Ride Through System

The power requirement of the control cards of the inverter has been calculated to be 78W for a 250kVA 3-phase inverter in the laboratory. This also considers a safety factor of 2 for the total steady current drawn by the cards. For the above power drawn, assuming an efficiency of 70% for the converter, the ultracapacitor is sized to provide 125W for 10s.

1) *Number of Ultracapacitor cells:* Prior to calculating the number of ultracapacitor cells required, it would be good to know the discharge characteristics [1] of ultracapacitors under constant power through the use of power converter.

The discharge characteristics of the ultracapacitor is given by Fig. 3. As per the system specifications,

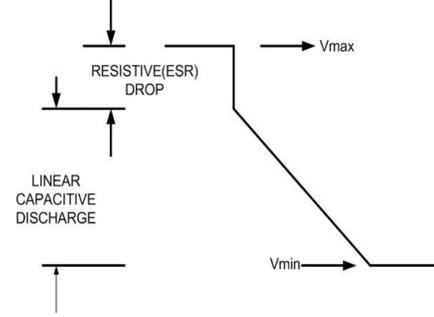


Fig. 3. Discharge profile of an ultracapacitor.

$$V_{max} = 30V, V_{min} = 13.7V, V_{nominal} = 24V. \quad (1)$$

$$dV = V_{nominal} - V_{min} \quad (2)$$

$$I_{max} = \frac{P}{V_{min}} \quad (3)$$

$$I_{min} = \frac{P}{V_{max}} \quad (4)$$

The maximum current is decided from the ultracapacitor datasheet, which fixes the minimum voltage to which the ultracap can drop to. This maximum current level is also limited by the current ratings of the bidirectional DC-DC converter.

$$dV = \frac{I_{avg}}{C_t} * (t + \tau) \quad (5)$$

In equation 5,  $\tau$  is the timeconstant of the ultracap which is taken normally as 1.1s and  $t$  is the time for the ultracap to provide ride through, in this case being 10s. Also  $I_{avg}$  is the average of the maximum and minimum ultracapacitor currents but for design purposes, it can be chosen to be equal to the maximum current. Using 1 to 5 the required capacitance is calculated to be 11F.

The number of cells required in series and parallel is calculated as:

$$C_t = C_{cell} * \frac{\text{parallel cells}}{\text{series cells}} \quad (6)$$

The number of series cells is determined by the voltage rating of the stack.

$$\text{series cells} = \frac{V_{max}}{V_{cell}} \quad (7)$$

The number of cells in series and parallel are calculated to be 12 and 1 respectively. Hence *the total number of ultracapacitor cells was chosen to be 12*. The ultracapacitors used were *Maxwell BCAP0150* capacitors of capacitance 150F.

2) *Ultracapacitor voltage management*: The rated voltage of the Maxwell BCAP0150 ultracapacitor is 2.7V and surge voltage is 2.85V [1]. The series connection of the ultracapacitor leads to unbalance in the voltage across each cell because of the differences in self-discharge rates and parameter tolerances. This can lead to excess voltage on one cell and a lesser voltage on some other cell. To prevent overvoltage across a particular cell, voltage equalization is done. The

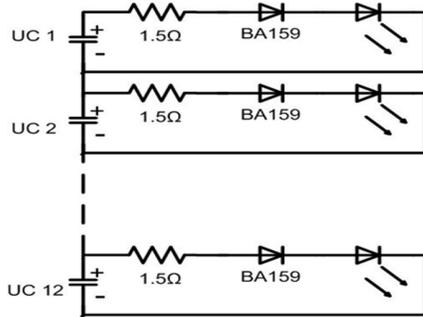


Fig. 4. Ultracapacitor cell voltage balancing network.

equalization method adopted here is connecting a series string of diodes, LEDs and a resistor of appropriate value in parallel with each cell. When the voltage across each cell is more than forward voltage drop of the diodes plus that of the LEDs, the LEDs starts glowing thereby discharging the cell. A 1.5Ω resistor was chosen to be used along with one diode (BA159) and one LED. The ultracapacitor hardware is shown in the Fig. 5

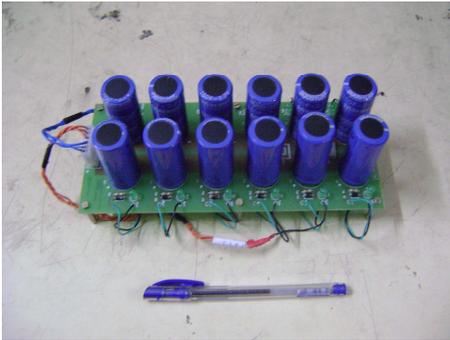


Fig. 5. Hardware of 12 series ultracapacitors and balancing network.

### III. HARDWARE DESIGN

#### A. Power Circuit

The the bidirectional DC-DC power converter circuit used is a 240VA bi-directional buck-boost converter. It comprises the choice of switching devices, design of the filter elements, switch gate drive circuit, and controller.

1) *Power Devices Selection*: The minimum voltage to which the stack of ultracapacitors can be discharged is determined by the maximum current rating of the ultracapacitors and the power devices chosen must carry this current. The

switches selected for this topology were IRF540N, the blocking voltage and current rating of which are 100V and 33A respectively. External anti-parallel diodes are not used with the MOSFETs, the body diodes of these devices are made use of.

2) *Gate Drive Circuit*: The driver circuit for the MOSFET consists of an optocoupler IC HCPL3101 to isolate the control circuit from the power circuit and IR2110 which is the driver with separate high and low side referenced output channels.

3) *Filter Inductor and Capacitor Selection*: The switching frequency is chosen as 100kHz. The inductor is designed for a current ripple of 0.2A as follows

$$V = L * \frac{dI}{dt} \quad (8)$$

$dI$  is the current ripple of 0.2A.  $dt$  is the on/off time of the switch. The value of  $V$  is chosen such that the product  $V*d$  is maximum. This occurs at the minimum value of the ultracapacitor voltage. The required inductance is calculated as 300μH. The filter capacitor is chosen depending on the voltage ripple which is chosen to be less than 0.1%. The capacitance is calculated to be 5000μF. Hence five 1000μF, 63V Electrolytic capacitors are chosen with a 1μF, 63V high frequency polystyrene capacitor. A +12V, 3A power supply IC, LM-2576 from National Semiconductor, is used to power the gate drive circuit and the control and sensing circuits. Microchip dsPIC30F2023 processor board for control.

#### B. Current and Voltage Sensing Circuit

To perform the controller action, all the voltages and currents should be converted into the processor's voltage range, here this being 5V. For this purpose, a LM-324 quad Op-amp based current and voltage sensing circuit was designed. The power for the LM-324 is fed through the LM 2576 power supply IC. Hence the op-amp's power supply terminals are +12V and Ground. Negative potentials cannot be represented. The output of these cards are fed to the ADC pins of the processor through an anti-aliasing filter circuit with a cut off frequency less than 1kHz. The two voltages, DC bus voltage and ultracapacitor voltage are sensed and are stepped down by a magnitude of 10 using a non-inverting amplifier circuit. The current is sensed through a current sense resistor of value 0.1Ω. A capacitor is used in parallel with the resistor, the resultant time constant being very less than the switching time of the converter.

The current sensing part is used to produce a voltage as per the equation

$$V_{Oadc} = 2.5 + (0.167 * I) \quad (9)$$

Equation 9 is used to produce a output of 5V for a maximum current of 15A and 0V for a maximum negative current of -15A.

### IV. CONTROLLER DESIGN

The control structure adopted is the normal two loop hierarchical control: outer voltage loop and the inner current loop The controllers are designed based on the small-signal analysis.

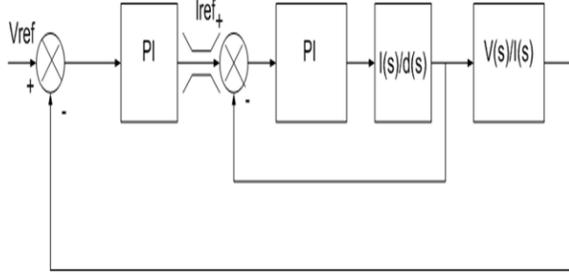


Fig. 6. Closed loop control structure of the bi-directional DC-DC converter.

#### A. Buck Converter Controller for Charging Ultracapacitors

The control structure adopted for charging ultracapacitors is the same as shown in Fig. 6. The bandwidth of the inner control loop is chosen as 10krad/sec.

##### 1) Inner Current Loop:

$$\hat{g}(s) = \frac{\hat{i}(s)}{\hat{d}(s)} = \frac{V_g C s}{L C s^2 + s \frac{L}{R} + 1}$$

Here the charging was done at  $V_g = 10V$ ,  $C = 12.5F$ ,  $L = 300\mu H$ ,  $R = 0.2\Omega$ . Where,  $R$  is the total ESR of the Ultracapacitor stack obtained by measurements made on a per cell basis using a network analyser.

$$\hat{g}(s) = \frac{\hat{i}(s)}{\hat{d}(s)} = \frac{125s}{1 + \frac{s}{667} + \frac{s^2}{16}} \quad (10)$$

The PI controller used to achieve the control objective is

$$\hat{h}(s) = \frac{\hat{d}(s)}{\hat{e}_i(s)} = \frac{1 + \frac{s}{1000}}{\frac{s}{253}} \quad (11)$$

2) Outer Voltage Loop: In this case the outer voltage loop controller can be just a proportional controller. The small signal transfer function of voltage to current is given by

$$\hat{g}(s) = \frac{\hat{v}(s)}{\hat{i}(s)} = \frac{1}{C s} \quad (12)$$

$$\hat{g}(s) = \frac{\hat{v}(s)}{\hat{i}(s)} = \frac{1}{12.5s}$$

The voltage loop P controller is chosen for a bandwidth of 1000 rad/sec. The transfer function of the P controller used is

$$\hat{h}(s) = \frac{\hat{i}_{ref}(s)}{\hat{e}_v(s)} = 12500 \quad (13)$$

#### B. Boost Converter Controller

The boost converter control structure implemented is just a voltage loop control. If inductor current has to be limited then an inner current loop is required. Here, in addition to a PI controller, a lead compensator is used to improve phase margin at the gain cross over frequency. The voltage to control transfer function is given by

$$\hat{g}(s) = \frac{\hat{v}(s)}{\hat{d}(s)} = \frac{V_g}{R(1-D)^2} \frac{1 - s \frac{L}{R(1-D)^2}}{1 + s \frac{L}{R(1-D)^2} + \frac{LC}{(1-D)^2} s^2}$$

In the experiment done, the values used were  $C=5000\mu F$ ,  $V_g=15V$ ,  $V_o=24V$ ,  $L=300\mu H$ ,  $R=20\Omega$ ,  $D=0.375$ . The transfer function is calculated to be

$$\hat{g}(s) = \frac{\hat{v}(s)}{\hat{d}(s)} = 38.4 \frac{1 - \frac{s}{26042}}{1 + \frac{s}{26042} + \frac{s^2}{510}} \quad (14)$$

$$\hat{h}(s) = \frac{\hat{d}(s)}{\hat{e}_v(s)} = \frac{1 + \frac{s}{510}}{\frac{s}{208}} \frac{1 + \frac{s}{510}}{1 + \frac{s}{10000}} \quad (15)$$

$\hat{e}_v(s)$  in (15) is the voltage error which is given by the difference in the voltage between the set reference value through the processor and the sensed value from the system. The boost converter controller is designed to achieve a bandwidth of 6000rad/sec. Both the controllers are implemented digitally using dsPIC30F2023 processor which has four pairs of PWM channels of which two channels have been made use of for pulse generation. The sensed voltages and currents are fed to six analog channels, with each signal given to two channels.

## V. EXPERIMENTAL RESULTS

#### A. Buck Converter Results - Charging of Ultracapacitors

The following describe the waveforms captured on the scope in the buck mode of operation of the bidirectional DC-DC converter.

- 1) Blue Waveform – DC bus voltage
- 2) Red Waveform – Ultracapacitor voltage
- 3) Brown Waveform – Ultracapacitor current

1) Charging at 1A: The input voltage was kept fixed at 24V. The charging was done with a charging current reference of 1A. The scope waveform shows the ultracapacitor bank getting charged from 7V to 23V in almost 175secs. This is validated below. For an ultracapacitor current of 1A, output from sensing circuit should be 2.67V which can be seen on scope. Fig. 7 shows the charging at 1A.

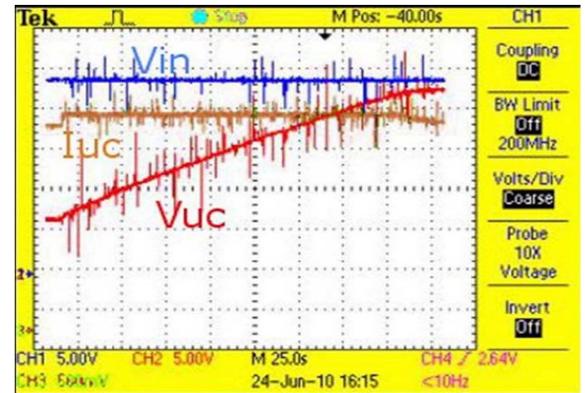


Fig. 7. Charging of the ultracapacitor bank at the rate of 1A.

$$I = C \frac{dv}{dt} \quad (16)$$

$$I_{adc} = 2.5 + (0.167 * 1) = 2.67V \quad (17)$$

$$t = dv * \frac{C}{I} = (23 - 7) * \frac{12.5}{1} = 200s \quad (18)$$

2) *Charging at 2A:* The input voltage was kept fixed at 24V. The charging was done with a charging current reference of 2A. The scope waveform shows the capacitor getting charged from 4V to 23V in almost 90secs. For an ultracapacitor current of 2A, output from sensing circuit should be 2.83V which can be seen on scope. Fig. 8 shows the charging at 2A.

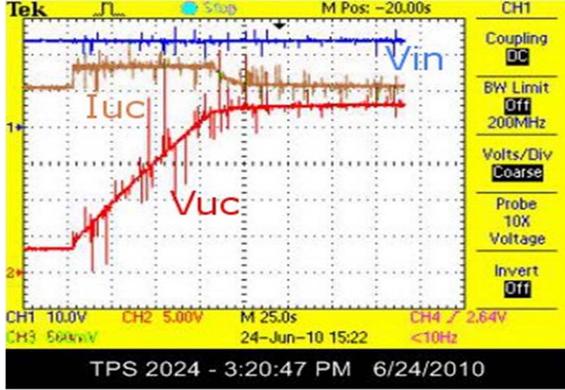


Fig. 8. Charging of the ultracapacitor bank at the rate of 2A.

$$I = 2A \quad (19)$$

$$I_{adc} = 2.5 + (0.167 * 2) = 2.83V \quad (20)$$

$$t = dv * \frac{C}{I} = (23 - 4) * \frac{12.5}{2} = 125s \quad (21)$$

### B. Boost Converter Results - Discharging of Ultracapacitors

The following describe the waveforms captured on the scope in the boost operation

- 1) *Blue Waveform* – Ultracapacitor voltage
- 2) *Red Waveform* – DC bus voltage

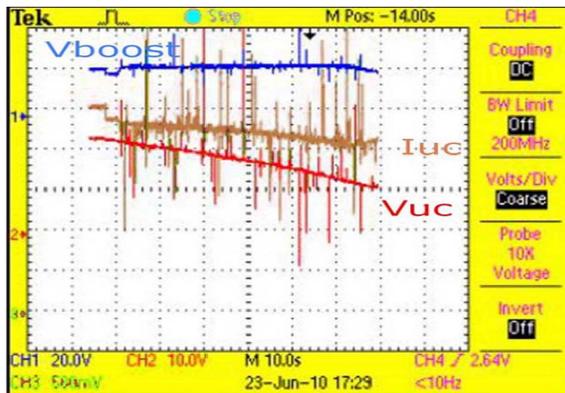


Fig. 9. Boost mode operation with 25W load.

1) *Boost Converter Operation with 25W (23V, 20Ω) load:* The Fig. 9 shows the discharge profile of ultracapacitors under a 25W (23V, 20Ω) load. It can be seen that the discharge takes place for almost 50secs, after which the PWM is turned off because the ultracapacitor has discharged to its minimum

voltage level which has been set as 15V. This is seen by the blue waveform starting to follow the ultracapacitor voltage after the 50secs period.

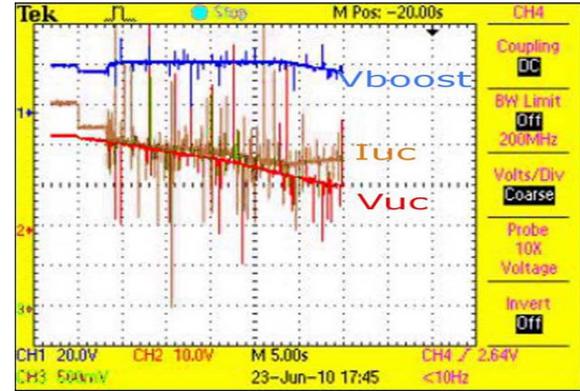


Fig. 10. Boost mode operation of the bidirectional DC-DC converter with 50W load.

2) *Boost Converter Operation with 50W (23V, 10Ω) load:* The Fig. 10 shows the discharge profile of ultracapacitors under a 50W (23V, 10Ω) load. It can be seen that the discharge takes place for almost 25secs, after which the PWM is turned off because the ultracapacitor has discharged to its minimum voltage level which has been set as 15V.

### C. Integrated Operation of Buck and Boost converter

The following describe the waveforms captured on the scope in the integrated operation of the converters

- 1) *Blue Waveform* – Ultracapacitor voltage
- 2) *Red Waveform* – DC bus voltage

The integrated operation is about creating the effect of voltage sag at the terminals of the ultracapacitor-converter and the loads by switching off the power supply and letting the ultracapacitor discharge and the power supply would be turned on, whence the capacitors start charging once again. Fig. 11

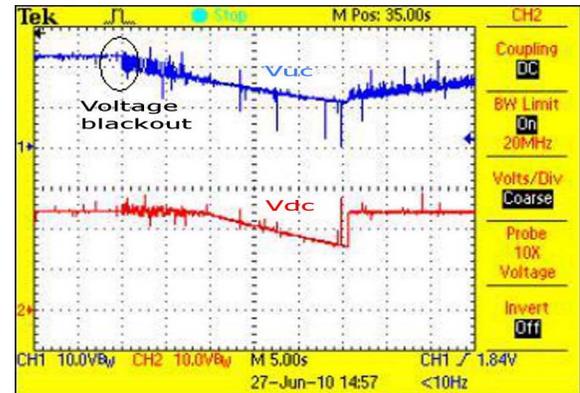


Fig. 11. Integrated bidirectional power flow mode of operation at 75W (23V, 7Ω.)

shows the integrated operation of the ride through system with

a 75W load. It can be seen that the voltage outage is detected almost instantaneously and the boost converter operates for almost 9s. After 9s, the ultracapacitor has discharged to the minimum voltage limit at which the PWM is turned off and thereafter the DC bus voltage starts drooping. The Fig. 12 shows two capacitor discharge and charge cycles.

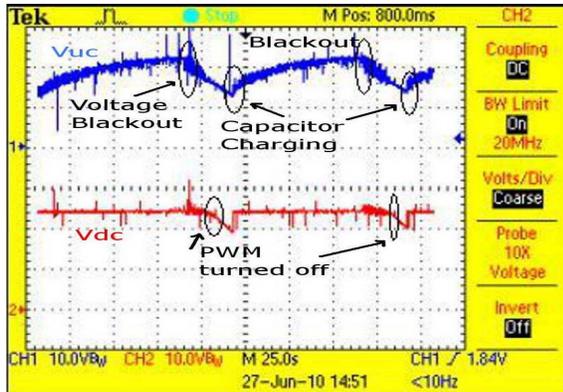


Fig. 12. Integrated charge and discharge operation for two sequential charge and discharge cycles.

## VI. CONCLUSION

The design of an ultracapacitor based power supply for a system controller ride through application is explained. The testing of the ride through power supply was done successfully with the tests carried out at three different loading modes allowing the ultracapacitor to feed the load during blackouts and charging back to the set reference during the presence of mains power. The controller design has been explained and tests indicate the seamless operation of the controller in the various operating modes.

The back up durations offered by the power supply for various

TABLE I  
RIDE THROUGH SYSTEM RESULTS.

Load	Backup Period
25W	50s
50W	25s
75W	9s

loads is shown in table I. It is seen that for 75W load the backup is almost 9secs that nearly meets the objective of the design.

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