Dual two-level inverter scheme for an open-end winding induction motor drive with a single DC power supply and improved DC bus utilisation

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Abstract: A dual two-level inverter fed open-end winding induction motor drive with a single DC-power supply is proposed. The proposed scheme produces voltage space vector locations identical to those of a conventional three-level inverter. In the conventional neutral-clamped three-level inverter, the series-connected DC link capacitors carry the load current, resulting in a fluctuating neutral point. Also, a three-level inverter requires bulky DC link capacitors. In the proposed scheme, the DC link capacitors carry currents of higher frequency and hence the neutral point fluctuations are reduced. A PWM switching strategy to suppress the zero sequence currents for all the voltage space phasor combinations is also proposed. This strategy is an improvisation of the one that uses a switched neutral to eliminate the triplen harmonic currents and results in an improved DC bus utilisation.

1 Introduction

Pulsewidth modulated (PWM) voltage source inverters are widely being used in industrial applications owing to their control flexibility and satisfactory spectral performance. Low switching frequency is preferred in high power applications to reduce the switching losses [1–3]. Power circuit complexity and cost increase as the number of output levels increase in multilevel configurations [1–3]. One of the main drawbacks of neutral point clamped multilevel inverters is that the neutral point fluctuates as the tapped capacitors carry the load current. Also, there is an ambiguity regarding the voltage rating of the power semiconductor devices, which are connected to the neutral point [4]. In the scheme proposed in [4], a clamping capacitor is added across the neutral clamping diodes of the conventional three-level inverter scheme [1] to reduce the neutral point fluctuation. Multilevel inverters with series-connected H-bridges have been suggested for high-resolution voltage vector generation [5–7]. However, the power circuit components and the complexity of gate drive circuit increase with such circuit configurations.

Many of the PWM schemes, when used for multilevel inverters, generate common-mode (zero sequence) voltages that are undesirable. A PWM scheme to suppress common-mode voltages in motor phases in an open-end winding induction motor drive is described in [8], with reduced DC bus utilisation. It has been shown in [9] and [10] that a combination of two-level inverters with half the DC link voltage (compared to a conventional single inverter scheme) with open-end winding for three-phase induction motors is capable of producing space-vector locations similar to that of a three-level inverter. In the scheme described in [10], the individual inverter switching frequency is equal to half the motors phase switching frequency, resulting in low inverter switching with reduced power circuit complexity.

The scheme suggested in [11] eliminates the necessity for bulky harmonic filters or isolation transformers for the suppression of zero sequence currents. The PWM strategy proposed in [11] is based on the observation that certain voltage space-vector combinations in the scheme proposed in [10] do not produce zero sequence voltages and hence zero sequence currents. While using other space-vector combinations, the zero sequence currents are eliminated by creating an isolated switched neutral using bidirectional auxiliary switches. However, the space vector combinations situated at the vertices of the outer hexagon cannot be utilised in this scheme, resulting in reduced DC bus utilisation [11].

In this paper, an alternative switching strategy is proposed for the circuit topology described in [11]. The proposed PWM strategy ensures that the DC bus utilisation for the proposed scheme is on a par with that of the conventional three-level inverter. A switching scheme is suggested that utilises all the space phasor combinations from the dual inverter scheme, with a single DC power supply, without having to employ bulky harmonic filters or isolation transformers for the suppression of the triplen harmonic components.

2 Dual inverter fed induction motor with open-end winding

A schematic of an open-end winding induction motor is shown in Fig. 1. Each inverter can produce its own voltage space phasor locations, resulting in a combined voltage space phasor locations and combinations as shown in Fig. 2 [10, 11]. There are a total of 64 space phasor combinations possible from the drive scheme of Fig. 1. But due to the open-end winding structure for the motor, the drive scheme of Fig. 1 can introduce a substantial number rof triplen harmonic currents in the motor phase windings. A detailed analysis of triplen harmonic contributions from various

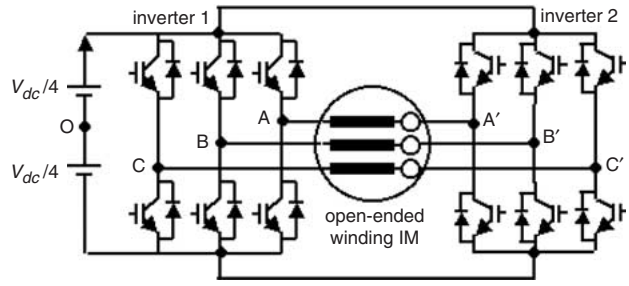

Fig. 1 *Dual inverter fed induction motor with open-end winding*

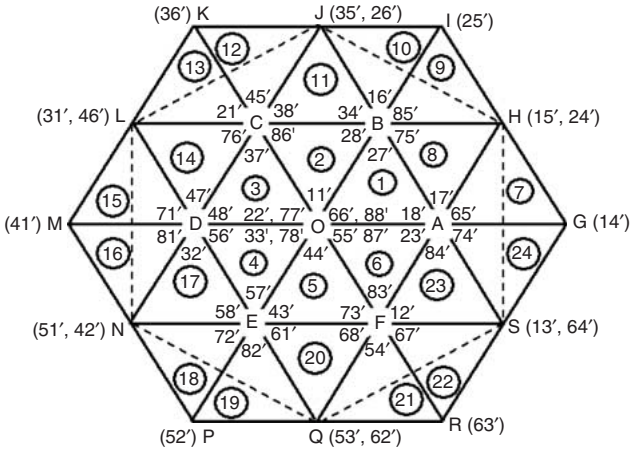

Fig. 2 *Voltage space phasor combinations from dual-inverter scheme*

space phasor combinations is presented in [10, 11]. Different space vector combinations will have different triplen harmonic voltage magnitudes and Table 1 shows the 20 space phasor combinations with zero triplen voltages in the motor phase voltage. This can be verified by assuming a particular space phasor combination for the dual inverter scheme. For example, a combination 3–5′ implies that the switching state for inverter 1 is (− + −) and that for inverter 2 is (− − +). A '+' indicates that a top switch in an inverter leg is turned on and a '−' indicates that the bottom switch in an inverter leg is turned on. For the 3–5′ combination the motor phase voltages are:

$$v_{aa'} = v_{ao} - v_{a'o} = -\frac{V_{dc}}{4} - \left(-\frac{V_{dc}}{4}\right) = 0$$

$$v_{bb'} = v_{bo} - v_{b'o} = +\frac{V_{dc}}{4} - \left(-\frac{V_{dc}}{4}\right) = \frac{V_{dc}}{2}$$

$$v_{cc'} = v_{co} - v_{c'o} = -\frac{V_{dc}}{4} - \left(\frac{V_{dc}}{4}\right) = -\frac{V_{dc}}{2} \qquad (1)$$

Table 1: Space phasor combinations with zero triplen contribution

Combinations with zero triplen voltages		
8–8′	5–5′	5–3′
3–5′	3–3′	4–4′
5–1′	3–1′	4–6′
4–2′	1–5′	1–3′
6–4′	2–4′	1–1′
6–6′	6–2′	2–6′
2–2′	7–7′	

The triplen harmonic voltage is given by:

$$v_{triplen} = \frac{(v_{aa'} + v_{bb'} + v_{cc'})}{3} \qquad (2)$$

For the combination 3–5′, the triplen harmonic content is calculated as:

$$v_{triplen}(3-5') = \frac{(v_{aa'} + v_{bb'} + v_{cc'})}{3} = \frac{1}{3}\left(0 + \frac{V_{dc}}{2} - \frac{V_{dc}}{2}\right) = 0 \qquad (3)$$

If the space vector combinations from Table 1 are exclusively used, the inverters of Fig. 1 can be used with a single DC link. But the magnitude of the maximum fundamental component gets reduced and the resultant voltage space phasor combinations lie at the vertices of a hexagon resulting in a PWM control similar to a conventional two-level inverter drive [8].

In [11] a three-level PWM control for the open-end winding drive is achieved by introducing a switched neutral with auxiliary bidirectional switches (Fig. 3). This will result in reduced DC link utilisation, because the extreme vertices of Fig. 2 are not used for PWM operation. In the present work, full DC link utilisation is achieved by properly controlling the auxiliary bidirectional switches, resulting in operation similar to conventional three-level PWM operation.

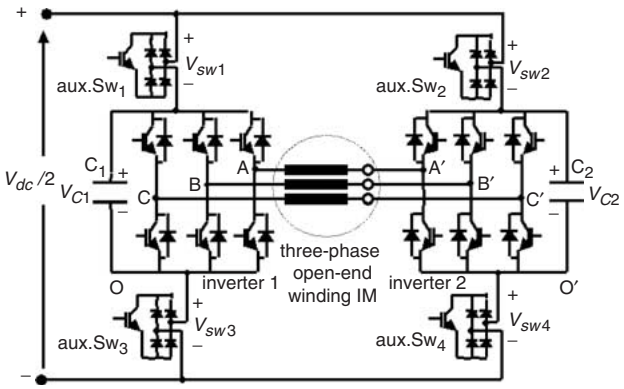

Fig. 3 *Proposed power circuit schematic*

3 Dual inverter with switched neutral

The power circuit schematic for drive operation with a single DC link is shown in Fig. 3 [11]. An isolated switched neutral is created using bidirectional auxiliary switches Sw_1 to Sw_4. With this topology all the space vector locations inside the hexagon, including and formed by the vertices H,J,L,N,Q and S of Fig. 3, are used for PWM operation, without resulting triplen harmonic currents in the motor phases. The hexagonal region used for PWM operation in [11] is highlighted by the dotted line in Fig. 3. It can be observed that space vector combinations at the vertices H,J,L,N,Q, S and O′ will not contribute to the zero sequence voltages (Table 1). Hence, for these combinations Sw_1 to Sw_4 can be closed without resulting in zero sequence currents [11]. For other locations, at the vertices A,B,C,D,E and F, the space phasor combinations with a zero inverter vector state (+ + + or − − −) for any one inverter is chosen for PWM operation. When one of the inverters is in zero vector state the corresponding bidirectional auxiliary switch pair is opened, and thereby denying a return path for the triplen currents.

This effectively creates a switched neutral for the drive scheme of Fig. 3.

In the work presented in [11], the space vector combinations at the vertices of the outer hexagon, namely G (1–4′), I (2–5′), K (3–6′), M (4–1′), P (5–2′) and R (6–3′), are not effectively utilised for PWM operation. Consequently, the region of operation in this strategy is limited to the hexagon HJLNQS (shown dotted in Fig. 2) [12]. This means that the DC bus utilisation would be inferior to a scheme in which these six combinations could be used. In this paper, an alternative space vector PWM scheme and control strategy for the bidirectional auxiliary switches are presented using all the space phasor locations. This will result in a motor output phase voltage waveform similar to a conventional three-level inverter scheme with full DC bus utilisation.

3.1 Improvement in DC bus utilisation

When the extreme space phasor locations G, I, K, M, P and R are used, as in this paper, the triplen harmonic components need to be suppressed. This is achieved by either using harmonic filers/transformer isolation as in the scheme described by [10] or by devising a switching strategy as described in the next Section. In this case, if the required peak value of the fundamental component (325 V) is to be obtained, the length of the reference voltage space vector $\boldsymbol{v}_{sr}$ must be equal to the radius of the largest circle inscribed in the hexagon GIKMPR (Fig. 2).

The radius of the largest circle inscribed in the hexagon GIKMPR is equal to $(\sqrt{3}/2)\ V_{dc}$. The instantaneous phase voltages can be obtained using (4):

$$\begin{bmatrix} \boldsymbol{v}_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} 2/3 & 0 \\ -1/3 & 1/\sqrt{3} \\ -1/3 & -1/\sqrt{3} \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{4}$$

where $\boldsymbol{v}_{sr} = (v_\alpha + jv_\beta)$.

Now for a maximum phase voltage of 325 V from the dual-inverter system, the DC link voltage required is when

$$|\boldsymbol{v}_{sr}| = \left(\frac{\sqrt{3}}{2}\right) * V_{dc},\ \left(\frac{2}{3}\right) * \left(\frac{\sqrt{3}}{2}\right) * V_{dc} = 325\,\text{V}$$

Threrefore $V_{dc} = 563$ V.

In the earlier work, in order to get the required peak value of the fundamental component (325 V), the maximum length of the reference voltage space vector '$\boldsymbol{v}_{sr}$' must be equal to $\left(\frac{\sqrt{3}}{2}\right) * \left(\frac{\sqrt{3}}{2}\right) V_{dc} = \left(\frac{3}{4}\right) V_{dc}$, the radius of the largest circle inscribed in the hexagon HJLNQS (Fig. 2) [11]. Hence, $\left(\frac{2}{3}\right) * \left(\frac{3}{4}\right) * V_{dc} = 325$ V and therefore $V_{dc} = 650$ V. Therefore, the percentage boost required in the DC bus voltage for the case in which the space vector combinations at the points G, I, K, M, P and R are not employed is given by $\frac{(650-563)}{563} * 100 \approx 15.45\%$, and by employing the space vector combinations at the points G, I, K, M, P and R, the DC bus utilisation could be improved by about 15%.

4 Improvised switching strategy to enhance the DC bus utilisation

In the switching strategy adopted in this paper, the pairs of auxiliary switches connecting the respective inverters to the DC bus are switched alternatively with a fixed frequency. This means that the auxiliary switches Sw_2 and Sw_4 are turned off while Sw_1 and Sw_3 are turned on, and vice versa (Fig. 3). In other words, the frequency with which a given inverter is connected to, or disconnected from, the DC bus is determined by the frequency with which the auxiliary switch pairs toggle. This would isolate one of the inverters from the DC bus while the other inverter is connected to the DC bus. Thus, the zero sequence currents (currents of the triplen harmonic order) are denied a path to flow, and the positive and the negative sequence currents flow without any impediment, as in the earlier switching strategy. The DC link capacitor of the inverter that is isolated from the DC bus would slightly discharge when the motor is loaded, and the voltage across the DC link capacitor belonging to the inverter that is connected to the DC bus remains relatively unaltered. For a conventional neutral clamped inverter, the ripple in the voltage across the DC link capacitors corresponds to the fundamental component of the load current, which could be very significant at lower speed range [4, 9]. The ripple in the voltage across the DC link capacitors in the present scheme always corresponds to the switching frequency of the auxiliary switches. It may therefore be expected that the neutral point fluctuation with the present switching strategy is considerably less than that of the conventional neutral clamped three-level inverter. In the present work, a switching frequency of about 500 Hz is used, which is an order above the maximum frequency with which the DC link capacitors in a conventional neutral clamped three-level inverter would have discharged.

The pairs of auxiliary switches are switched with a duty factor of 50% to ensure an equal duty for the auxiliary switch pairs. Also, a dead time of about 10 μs is chosen to avoid the overlapping conduction of the outgoing pair and the incoming pair of the auxiliary switches.

Applying Kirchhoff's voltage law around the loop O-A-A′-O′-O (Fig. 3):

$$v_{AO} - v_{AA'} - v_{A'O'} - v_{O'O} = 0 \tag{5}$$

Therefore

$$v_{AA'} = (v_{AO} - v_{A'O'}) - v_{O'O} \tag{6}$$

Applying Kirchhoff's voltage law around the loop O-B-B′-O′-O (Fig. 3):

$$v_{BB'} = (v_{BO} - v_{B'O'}) - v_{O'O} \tag{7}$$

Applying Kirchhoff's voltage law around the loop O-C-C′-O′-O (Fig. 3):

$$v_{CC'} = (v_{CO} - v_{C'O'}) - v_{O'O} \tag{8}$$

Adding (6), (7) and (8):

$$\begin{aligned} v_{AA'} + v_{BB'} + v_{CC'} &= (v_{AO} - v_{A'O'}) \\ &+ (v_{BO} - v_{B'O'}) + (v_{CO} - v_{C'O'}) - 3v_{O'O} \end{aligned} \tag{9}$$

As mentioned earlier, the triplen harmonic components are denied a path to flow as one of the inverters is disconnected from the DC bus due to the alternating switching of the auxiliary switch pair. Therefore, the auxiliary switches with this switching strategy are constrained to block the triplen harmonic content of the set of the difference of pole voltages $(v_{AO} - v_{A'O})$, $(v_{BO} - v_{B'O})$ and $(v_{CO} - v_{C'O})$ (Fig. 3, (1) and (2)). Consequently, the motor phase voltages $v_{AA'}$, $v_{BB'}$ and $v_{CC'}$ do not contain the triplen harmonic components. This means that:

$$v_{AA'} + v_{BB'} + v_{CC'} = 0 \tag{10}$$

Hence, from (9) and (10), the instantaneous value of the triplen harmonic component $v_{O'O}$ is

$$\begin{aligned} v_{O'O} = \frac{1}{3}[&(v_{AO} - v_{A'O'}) + (v_{BO} - v_{B'O'}) \\ &+ (v_{CO} - v_{C'O'})] \end{aligned} \tag{11}$$

Applying Kirchhoff's voltage law around the loop consisting of the DC power supply Sw_1, C_1 and Sw_3:

$$\frac{V_{dc}}{2} - v_{sw1} - v_{C1} - v_{sw3} = 0 \text{ and } v_{C1} \approx \frac{V_{dc}}{2} \quad (12)$$

Therefore

$$v_{sw1} = -v_{sw3} \quad (13)$$

Hence, when a given pair of auxiliary switches is opened, the instantaneous voltages across the individual switches are equal in magnitude but are of opposite signs (i.e. these voltage waveforms are in anti-phase with respect to each other). Hence the sum of the instantaneous voltages across that pair of auxiliary switches is always zero. This means that, when a given pair of auxiliary switches is opened, the waveform of the voltage across one of these switches during that period is identical to the triplen harmonic content ((11) and Fig. 3).

5 Proposed PWM switching strategy

5.1 PWM generation for inner sectors

From Fig. 2, sectors 1–6 form the inner sectors. The PWM strategy involves the following steps: (*a*) sector identification in which the tip of the reference space phasor $\boldsymbol{v_{sr}}$ lies, and (*b*) finding the switching timings T_1, T_2 and T_0 for the vectors forming the triangular sector [10, 12]. The sector identification is achieved by taking the projection of the reference space phasor $\boldsymbol{v_{sr}}$ along the *jA*, *jB*, *jC* axes, which are orthogonal to the *A*,*B*,*C* axes, respectively (Fig. 4) [10]. The projected values v^*_{ja}, v^*_{jb} and v^*_{jc} are then compared with fixed values for sector identification [10, 11]. For example the comparison levels for sector 1 identification are:

$$v^*_{ja} < (\sqrt{3}/4)V_{dc},\ v^*_{jb} \geq -(\sqrt{3}/4)V_{dc},\ v^*_{jc} < (\sqrt{3}/4)V_{dc} \quad (14)$$

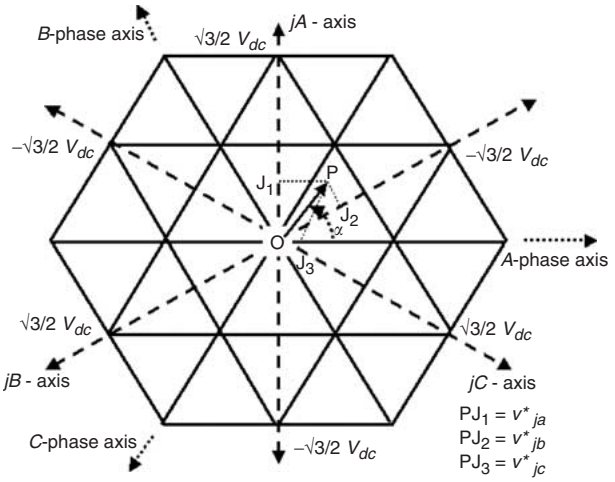

Fig. 4 *Procedure for sector identification*
OP: Reference voltage space phasor

Once the sector is identified, for the inner sectors the switching timings T_1, T_2 and T_0 are obtained directly from the instantaneous sampled reference values [10–12]. The inverter switching vectors and sequences for the inner sectors used for the present work are presented in Table 2.

5.2 PWM switching strategy for the outer sectors

The outer layer consists of the sectors numbered 7 to 24 (Fig. 2). In Fig. 5, the reference voltage vector ***OT*** is shown

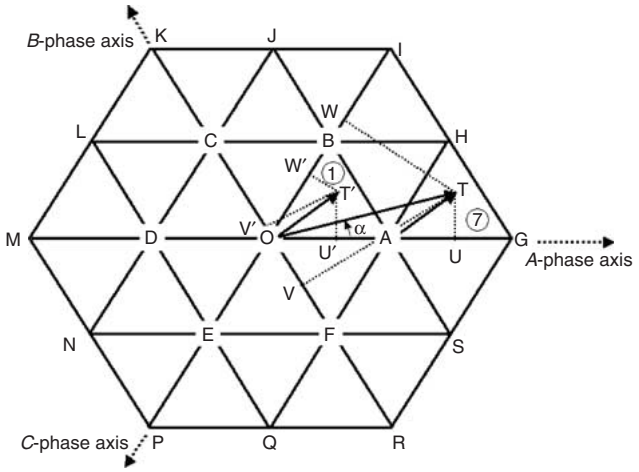

Fig. 5 *Resolution of reference voltage space phasor in middle and outer sectors*

with its tip lying in sector 7. The vector ***OT*** can be conceived to be the summation of two components ***OA*** and ***AT***. The vector ***OA*** can readily be obtained from the appropriate space vector combinations from the individual inverters (Fig. 2). The vector ***AT*** can be produced by switching amongst the space vector combinations situated at the vertices A, G and H, which constitute sector 7 using the volt-second balance. This can be accomplished by mapping the original reference space vector ***OT*** onto the inner sub-hexagon centred on O by shifting the sub-hexagonal centre A to O, using an appropriate co-ordinate transformation. Thus, the original reference voltage vector ***OT*** gets mapped as ***OT′*** into the inner hexagon.

The generalised equations of transformation for shifting the centres A–F to O are given by:

$$\begin{aligned} v_a &= v^*_a - \frac{V_{dc}}{3}\cos\left[\frac{(m-1)\pi}{3}\right] \\ v_b &= v^*_b + \frac{V_{dc}}{3}\cos\left[\frac{m\pi}{3}\right] \\ v_c &= v^*_c + \frac{V_{dc}}{3}\cos\left[\frac{(m-2)\pi}{3}\right] \end{aligned} \quad (15)$$

In these equations, the quantities v^*_a, v^*_b and v^*_c are the instantaneous reference phase values of the actual reference voltage space vector ***OT*** and the quantities v_a, v_b and v_c are the instantaneous reference phase voltages corresponding to the transformed reference voltage space vector ***OT′*** that is situated in the inner hexagon. The index m is an integer variable that assumes values 1 to 6, respectively, for points A to F.

The transformed instantaneous reference phase voltages v_a, v_b and v_c are employed to realise ***OT′*** in the inner hexagon. The algorithm described in [10–12] is used to determine the inverter leg switching timings for the transformed reference voltage space vector ***OT′***, and these timings are then employed to switch between the vertices A, G and H to produce the original reference voltage vector ***OT*** in sector 7. A similar procedure is adopted in all the other sectors belonging to the outer layer.

When the tip of ***OT*** is situated in any of the sectors numbered 8, 11, 14, 17, 20 and 23, the nearest sub-hexagonal center to the tip of ***OT*** is identified and mapped to the inner sector for determining the switching timings [10, 11].

In all the sectors, it is ensured that only one of the two inverters switches while the other inverter is clamped to a given state. This feature is evident from Table 2.

Table 2: Inverter switching vectors and sequences

α (deg)	Possible sectors			Switching sequences		
				inner sectors $T_0/2\ -T_2-T_1-T_0/2$	middle sectors	outer sectors
0.0	1	—	7	88′-85′-84′-87′	—	74′-24′-14′-84′
7.5	1	8	7	77′-27′-17′-87′	84′-34′-24′-74′	84′-14′-24′-74′
15.0	1	8	7	77′-27′-17′-87′	74′-24′-34′-84′	74′-24′-14′-84′
22.5	1	8	7	88′-85′-84′-87′	17′-16′-15′-18′	17′-14′-15′-18′
30.0	1	8	7	88′-18′-28′-78′	85′-15′-65′-75′	15′-15′-15′-15′
37.5	1	8	9	77′-74′-75′-78′	28′-23′-24′-27′	28′-25′-24′-27′
45.0	1	8	9	77′-74′-75′-78′	27′-24′-23′-28′	27′-24′-25′-28′
52.5	1	8	9	88′-18′-28′-78′	75′-65′-15′-85′	75′-25′-15′-85′
60.0	2	—	10	88′-38′-28′-78′	—	85′-35′-25′-75′
67.5	2	11	10	77′-76′-75′-78′	75′-45′-35′-85′	75′-25′-35′-85′
75.0	2	11	10	77′-76′-75′-78′	85′-35′-45′-75′	85′-35′-25′-75′
82.5	2	11	10	88′-38′-28′-78′	28′-21′-26′-27′	28′-25′-26′-27′
90.0	2	11	10	88′-85′-86′-87′	76′-26′-16′-86′	26′-26′-26′-26′
97.5	2	11	12	77′-27′-37′-87′	37′-34′-35′-38′	37′-36′-35′-38′
105.0	2	11	12	77′-27′-37′-87′	38′-35′-34′-37′	38′-35′-36′-37′
112.5	2	11	12	88′-85′-86′-87′	86′-16′-26′-76′	86′-36′-26′-76′
120.0	3	—	13	88′-81′ -86′-87′	—	76′-46′-36′-86′
127.5	3	14	13	77′-47′-37′-87′	86′-56′-46′-76′	86′-36′-46′-76′
135.0	3	14	13	77′-47′-37′-87′	76′-46′-56′-86′	76′-46′-36′-86′
142.5	3	14	13	88′-81′-86′-87′	37′-32′31′-38′	37′-36′-31′-38′
150.0	3	14	13	88′-38′-48′-78′	81′-31′-21′-71′	31′-31′-31′-31′
157.5	3	14	15	77′-76′-71′-78′	48′-45′-46′-47′	48′-41′-46′-47′
165.0	3	14	15	77′-76′-71′-78′	47′-46′-45′-48′	47′-46′-41′-48′
172.5	3	14	15	88′-38′-48′-78′	71′-21′-31′-81′	71′-41′-31′-81′
180.0	4	—	16	88′-58′-48′-78′	—	81′-51′-41′-71′
187.5	4	17	16	77′-72′-71′-78′	71′-61′-51′-81′	71′-41′-51′-81′
195.0	4	17	16	77′-72′-71′-78′	81′-51′-61′-71′	81′-51′-41′-71′
202.5	4	17	16	88′-58′-48′-78′	48′-43′-42′-47′	48′-41′-42′-47′
210.0	4	17	16	88′-81′-82′-87′	72′-42′-32′-82′	42′-42′-42′-42′
217.5	4	17	18	77′-47′-57′-87′	57′-56′-51′-58′	57′-52′-51′-58′
225.0	4	17	18	77′-47′-57′-87′	58′-51′-56′-57′	58′-51′-52′-57′
232.5	4	17	18	88′-81′-82′-87′	82′-32′-42′-72′	82′-52′-42′-72′
240.0	5	—	19	88′-83′-82′-87′	—	72′-62′-52′-82′
247.5	5	20	19	77′-67′-57′-87′	82′-12′-62′-72′	82′-52′-62′-72′
255.0	5	20	19	77′-67′-57′-87′	72′-62′-12′-82′	72′-62′-52′-82′
262.5	5	20	19	88′-83′-82′-87′	57′-54′-53′-58′	57′-52′-53′-58′
270.0	5	20	19	88′-58′-68′-78′	83′-53′-43′-73′	53′-53′-53′-53′
277.5	5	20	21	77′-72′-73′-78′	68′-61′62′-67′	68′-63′-62′-67′
285.0	5	20	21	77′-72′-73′-78′	67′-62′61′-68′	67′-62′-63′-68′
292.5	5	20	21	88′-58′-68′-78′	73′-43′-53′-83′	73′-63′-53′-83′
300.0	6	—	22	88′-18′-68′-78′	—	83′-13′-63′-73′
307.5	6	23	22	77′-74′-73′-78′	73′-23′-13′-83′	73′-63′-13′-83′
315.0	6	23	22	77′-74′-73′-78′	83′13′-23′-73′	83′-13′-63′-73′
322.5	6	23	22	88′-18′-68′-78′	68′-65′-64′-67′	68′-63′-64′-67′
330.0	6	23	22	88′-83′-84′-87′	74′-64′-54′-84′	64′-64′-64′-64′
337.5	6	23	24	77′-67′-17′-87′	17′-12′-13′-18′	17′-14′-13′-18′
345.0	6	23	24	77′-67′-17′-87′	18′-13′-12′-17′	18′-13′-14′-17′
352.5	6	23	24	88′-83′-84′-87′	84′-54′-64′-74′	84′-14′-64′-74′

In the present work each cycle of the reference phase voltage is divided into 48 equal sub-intervals. Each sub-interval duration corresponds to the sampling interval T_s for PWM operation. This is maintained for the entire modulation range, including the over-modulation region [11], with voltage/frequency control.

6 Experimental results and discussion

The proposed scheme has been implemented for a 1 kW, three-phase, open-end induction motor drive in open loop with voltage/frequency control for different reference voltages covering the entire speed range. The gating signals for the dual-inverter drive were generated using a TMS 320F240 DSP. A DC bus voltage of 200 V was employed for experimentation.

The experimental results for $|\boldsymbol{v}_{sr}| = 0.4\ V_{dc}$ are presented in Fig. 6. In this case, the tip of the reference voltage space vector $\boldsymbol{v}_{sr}$ is confined to the inner sub-hexagon, i.e. sectors 1–6 (Fig. 2). The experimentally obtained pole voltage waveforms v_{AO} and $v_{A'O}$ (Fig. 3) are presented in Fig. 6*a* (top and bottom traces, respectively). Figure 6*b* shows the triplen harmonic content in the difference of the pole voltages ($v_{AO} - v_{A'O}$). Figure 6*c* gives the voltage across (top trace) and the current through the auxiliary switch 3 (bottom trace) (Fig. 3). As explained in Section 4, the voltage across the auxiliary switch Sw_3 is identical to the triplen harmonic content in the difference of the pole voltages ($v_{AO} - v_{A'O}$) when the switch pair Sw_3 and Sw_4 is opened. Figure 6*d* shows the motor phase voltage waveform. The motor phase current waveform at no load is presented in Fig. 6*e*.

These experimental results demonstrate the capability of the proposed power circuit topology and the PWM strategy to eliminate the triplen harmonic components, as explained in Section 4.

The experimental results for the case corresponding to $|\boldsymbol{v}_{sr}| = 0.7$ V DC are presented in Figs. 7*a* –*e*. When $|\boldsymbol{v}_{sr}| = 0.7\ V_{dc}$, the tip of the reference voltage space vector lies exclusively in the outer layer (sectors numbered 7 to 24). Figure 7*a* presents the pole voltages in this case. Figure 7*b* presents the triplen harmonic content as the difference of these pole voltages. Figure 7*c* presents the voltage across the auxiliary switch (top trace) and the current through the auxiliary switch. From Fig. 7*b* and the top trace of Fig. 7*c*, it is evident that the voltage across the auxiliary switch is identical to the triplen harmonic content when the switch is

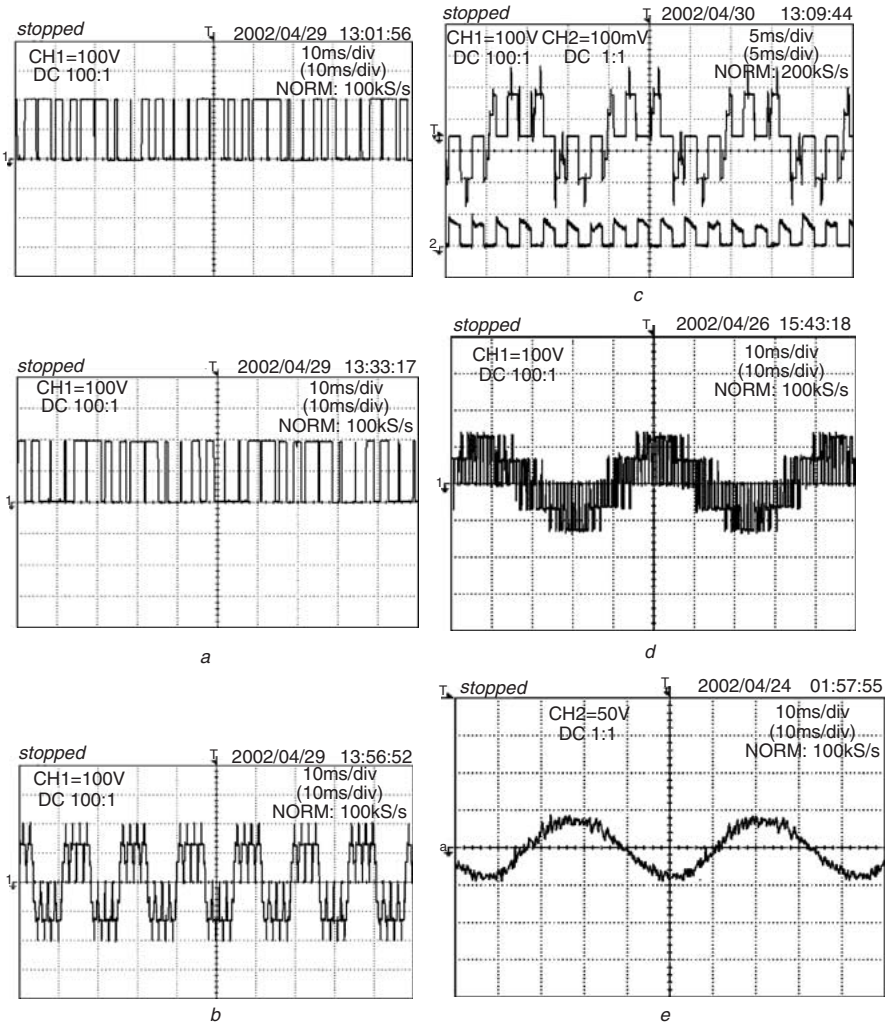

Fig. 6
a Waveforms for pole voltages v_{ao} (top) and $v_{a'o}$ (bottom) for $|V_{sr}| = 0.4\ V_{DC}$
Scale: *x*-axis 10 ms/div; *y*-axis 100 V/div
b Triplen harmonic content in the voltage (v_{ao}–$v_{a'o}$) for $|V_{sr}| = 0.4\ V_{DC}$
Scale: *x*-axis 10 ms/div; *y*-axis 100 V/div
c Voltage across and current through the auxiliary switch for $|V_{sr}| = 0.4\ V_{DC}$
Scale: *x*-axis 5 ms/div; *y*-axis 100 V/div (top) 0.5 A/div (bottom)
d Experimental motor phase voltage for $|V_{sr}| = 0.4\ V_{DC}$
Scale: *x*-axis 10 ms/div; *y*-axis 100 V/div
e Experimental motor phase current at no-load for $|V_{sr}| = 0.4\ V_{DC}$
Scale: *x*-axis 10 ms/div; *y*-axis 1 A/div

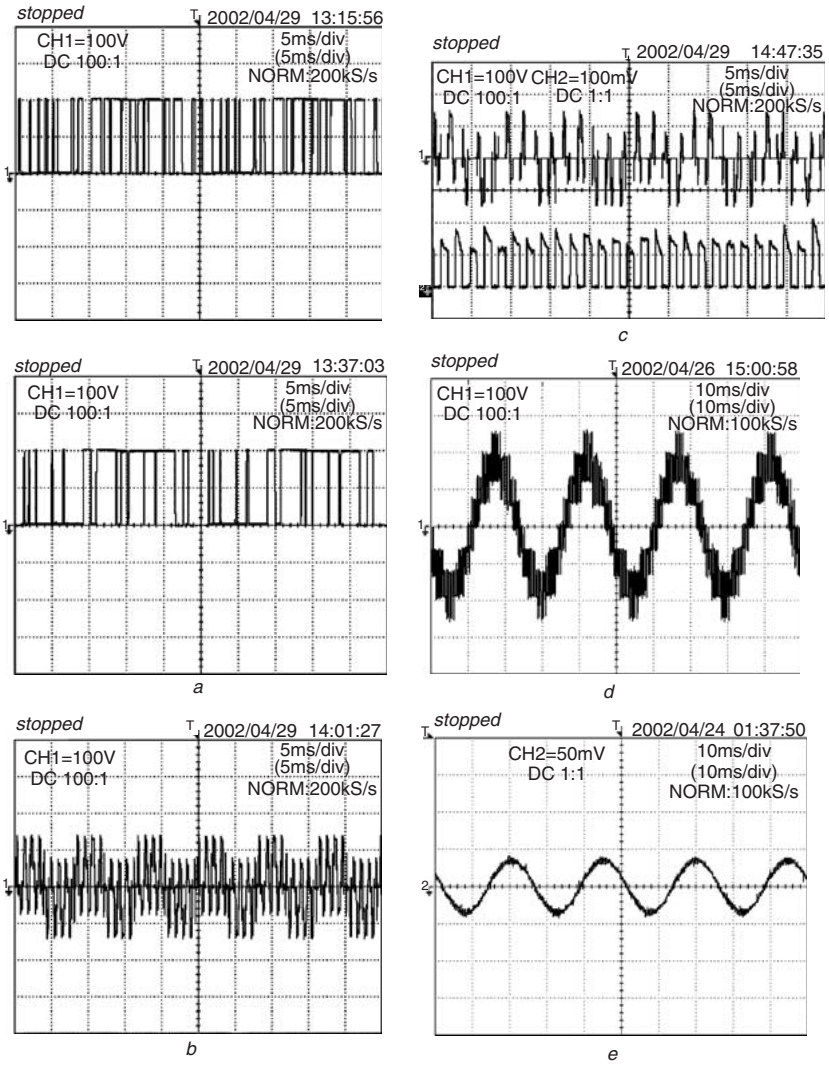

Fig. 7
a Waveforms for pole voltages v_{ao} (top) and $v_{a'o}$ (bottom) for $|V_{sr}| = 0.7\,V_{DC}$
Scale: *x*-axis 5 ms/div; *y*-axis 100 V/div
b Triplen harmonic content in the voltage (v_{ao}–$v_{a'o}$) for $|V_{sr}| = 0.7\,V_{DC}$
Scale: *x*-axis 5 ms/div; *y*-axis 100 V/div
c Voltage across and current through the auxiliary switch for $|V_{sr}| = 0.7\,V_{DC}$
Scale: *x*-axis 5 ms/div; *y*-axis 100 V/div (top); 0.5 A/div (bottom)
d Experimental motor phase voltage for $|V_{sr}| = 0.7\,V_{DC}$
Scale: *x*-axis 10 ms/div; *y*-axis 100 V/div
e Experimental motor phase current at no-load for $|V_{sr}| = 0.7\,V_{DC}$
Scale: *x*-axis 10 ms/div; *y*-axis 1 A/div

turned off. Note that, in this case, all the extreme vertices G, I, K, M, P and R are used in the switching strategy. The experimental phase voltage is presented in Fig. 7*d*, and it is similar to the conventional three-level motor phase voltage waveform. The motor phase current at no-load in this case is presented in Fig. 7*e*.

Similar experimental results corresponding to the case of over-modulation [10] are presented in Figs. 8*a–e*. During over modulation, the tip of $\boldsymbol{v}_{sr}$ is forced to trace the outer hexagon GIKMPR. The motor phase current is slightly distorted in this case due to the presence of the lower order harmonics (5th, 7th etc.) in the phase voltage waveform.

Figures 9*a–e* present the experimental results obtained when the dual inverter system is in the mode of 12-stepped operation. In this mode of operation, the space vector combinations at G, H, I, J, K, L, M, N, P, Q, R and S are sequentially switched for the fundamental cycle of operation. The 12 steps are clearly discernible in the phase voltage waveform presented in Fig. 9*d*. The motor phase current is further distorted in this case due to the enhancement of the lower order harmonics in this operating mode.

Thus, for the dual-inverter fed open-end winding induction motor drive with a single DC power supply, triplen harmonic elimination is achieved, without using either isolation transformers or harmonic filters. With the proposed switching scheme, all 64 space phasor combinations can be employed. Thus, the space phasor locations produced in the current scheme are identical to those produced by a conventional three-level inverter. The switching strategy proposed in this paper is an

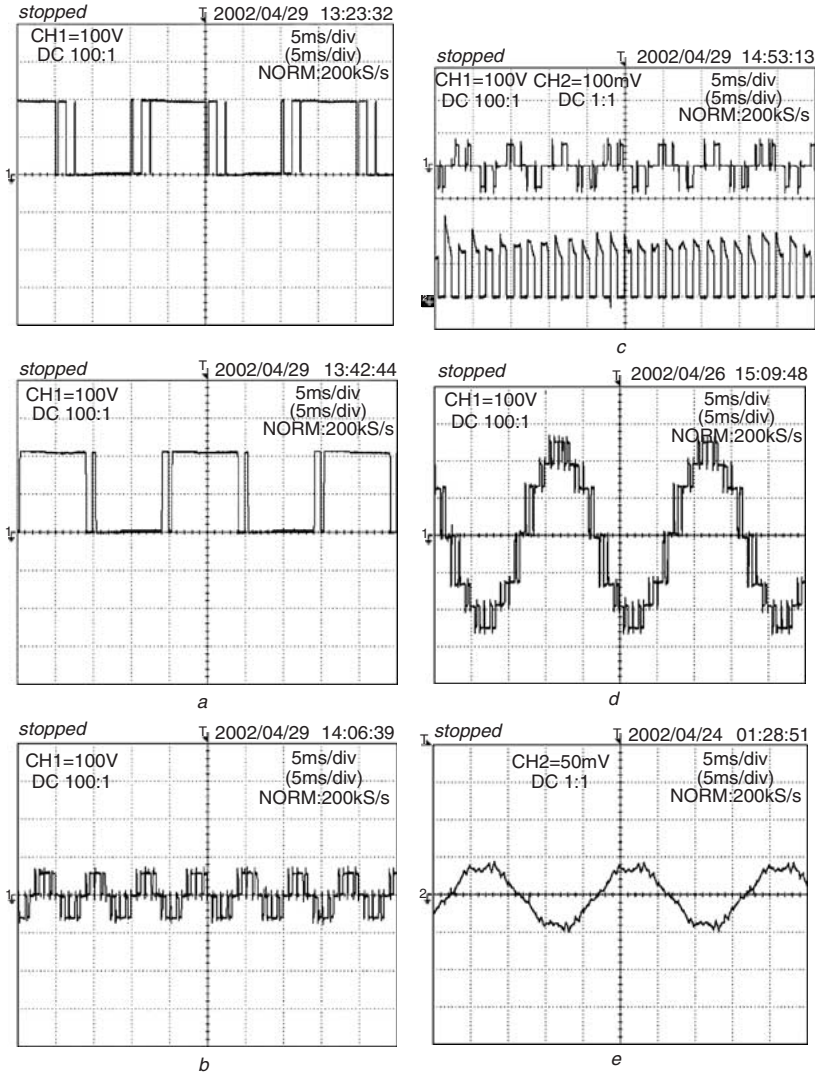

Fig. 8
a Waveforms for pole voltages v_{ao} (top) and $v_{a'o}$ (bottom) for $|V_{sr}| = V_{DC}$ (over-modulation)
Scale: *x*-axis 5 ms/div; *y*-axis 100 V/div
b Triplen harmonic content in the voltage (v_{ao}–$v_{a'o}$) for $|V_{sr}| = V_{DC}$ (over-modulation)
Scale: *x*-axis 5 ms/div; *y*-axis 100 V/div
c Voltage across and current through the auxiliary switch for $|V_{sr}| = V_{DC}$ (over-modulation)
Scale: *x*-axis 5 ms/div; *y*-axis 100 V/div (top) 0.5 A/div (bottom)
d Experimental motor phase voltage for $|V_{sr}| = V_{DC}$ (over-modulation)
Scale: *x*-axis 5 ms/div; *y*-axis 100 V/div
e Experimental motor phase current at no-load for $|V_{sr}| = V_{DC}$ (over-modulation)
Scale: *x*-axis 5 ms/div; *y*-axis 1 A/div

improvisation over the one proposed in [11] and improves the DC bus utilisation by about 15%.

7 Conclusions

A dual two-level inverter fed open-end winding induction motor drive using a single DC link is proposed with voltage space phasor locations similar to that of a conventional three-level inverter. A PWM switching strategy to suppress the triplen harmonic currents is highlighted without the need for bulky harmonic filters or isolation transformers. The triplen harmonic current suppression is achieved by alternately connecting one of the inverters to the DC link by toggling the bidirectional auxiliary switch pairs. The modified switching strategy could enhance the DC bus utilisation by a factor of 15% compared to the earlier scheme reported in [11]. The neutral point fluctuations are expected to be smaller in the proposed scheme, when compared to a three-level inverter.

The frequency of the ripple current of the individual DC link capacitors is determined by the switching frequency of the auxiliary switch pair and not by the frequency of the fundamental component of the load current, as for a conventional neutral clamped three-level inverter.

The switching frequency of each inverter is half of the motor phase switching frequency. The proposed space phasor based PWM scheme requires only the instantaneous sampled values of the reference phase voltages as inputs for gate drive signal generation, in the entire speed range. The switching patterns are implemented in such a way that minimum inverter switch transitions are only needed during a sampling period T_s.

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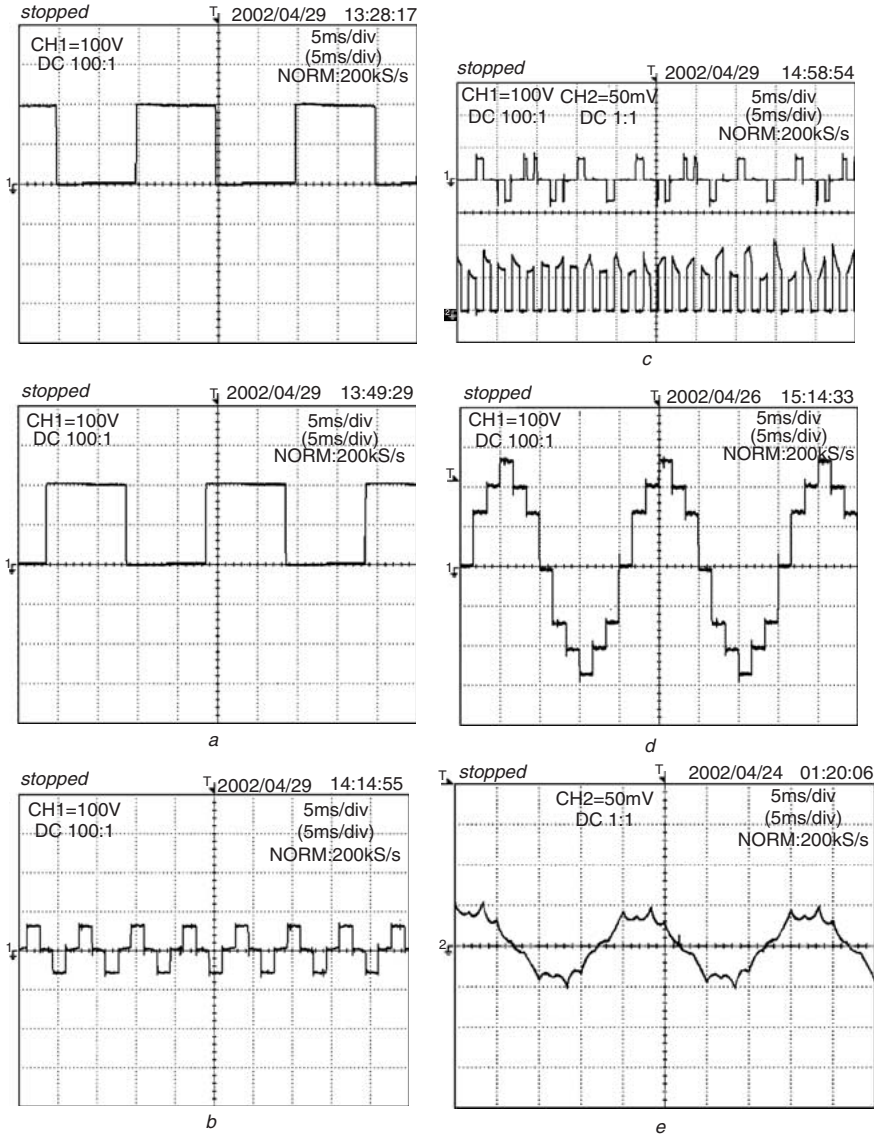

Fig. 9

a Waveforms for pole voltages v_{ao} (top) and $v_{a'o}$ (bottom) for 12-step operation
Scale: *x*-axis 5 ms/div; *y*-axis 100 V/div
b Triplen harmonic content in the voltage (v_{ao}–$v_{a'o}$) for 12-step operation
Scale: *x*-axis 5 ms/div; *y*-axis 100 V/div
c Voltage across and current through the auxiliary switch for 12-step operation
Scale: *x*-axis 5 ms/div; *y*-axis 100 V/div (top) 0.5 A/div (bottom)
d Experimental motor phase voltage for $|V_{sr}| = V_{DC}$ (over-modulation)
Scale: *x*-axis 5 ms/div; *y*-axis 100 V/div
e Experimental motor phase current for 12-step operation at no load
Scale: *x*-axis 5 ms/div; *y*-axis 100 V/div (top) 1 A/div (bottom)

development tools for the implementation of the PWM generation.

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