Design of Low Voltage Low Power CMOS OP-AMPS with Rail-to-Rail Input/Output Swing.

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Abstract—A novel input and output biasing circuit to extend the input common mode (CM) voltage range and the output swing to rail-to-rail in a low voltage op-amp in standard CMOS technology is presented. The input biasing circuit uses a Switched Capacitor Based Attenuator (SCBA) approach to establish rail-to-rail common mode input voltage range. And the output biasing circuit uses an Output Driver (OD), with floating bias to give the rail-to-rail swing at output stage. Three different OD schemes in operational amplifier have been proposed and tested the performance with SCBA. The simulation results justify the theoretical analysis.

I. Introduction

The importance of analogue circuits using low supply voltage is enormously increasing in recent past [1], [2], [3]. The large component densities particularly in VLSI demands lower power consumption. The low power consumption is a key factor in modern portable equipments to increase the battery life and also, the packaging density and circuit reliability. Low power dissipation is attractive and even essential in battery operated systems for longer life. The power consumption can be minimized either by reducing the supply voltage or current. But the transistor noise is dependent on current. Hence, for high performance analogue circuits, reduction in current beyond certain limit is not recommended and the most accepted method of reducing the power consumption is through the reduction in supply voltage. Typical supply voltage used in analogue circuits is around 2.5 V - 3.0 V. But the latest trends suggest that supply voltages can go down to 1.5 V and may less even [4], [5]. But scaling down the supply voltage leads to a formidable challenge in the design of CMOS analogue circuits as threshold voltage of analogue devices is a bottleneck. Since, in near future, threshold voltage in CMOS devices may not decrease much [6], the design of standard CMOS analogue / mixed circuits with a threshold voltage of about 0.7 V opens up a great research interest.

The fundamental building block of any analogue/mixed signal circuit is the Operational Amplifier (op-amp) [7]. The

two critical problems in low voltage op-amp design are providing rail-to-rail Common Mode (CM) input range and output swing. The reduced supply voltage also degrades the circuit performance like bandwidth and input/output swings. With the reduction of supply voltage, the CM input voltage range of conventional CMOS differential amplifier becomes narrower and lies in the region between $V_{SS} + V_T + 2V_{Dsat}$ (i.e., V_A and V_{DD}) as shown in Fig. 1 [7], where V_{SS} , V_{DD} are negative and positive supply voltages respectively, V_T is the threshold voltage of CMOS device and V_{Dsat} is the saturation voltage of the transistor. The decrease in input

Fig. 1. Operation zone of low supply CMOS op-amp.

CM range imposes a serious restriction over which the input signal can be applied. If the applied input signal falls in the forbidden region (i.e., between V_A and V_{SS}), it will not be amplified properly. It is also clear from Fig. 1 that the maximum input signal levels which can be applied at the input of the differential pair for proper amplification must lie in the region around a DC ($\frac{V_{DD} + V_A}{2}$), where V_A is the minimum permissible CM voltage level of the differential amplifier. It is also clear that an input signal with zero DC falls in the forbidden region and therefore is not suitable for amplification. Hence, a circuit which moves the input signal from the forbidden region to the active region of the differential amplifier is required.

The other problem considered in the design of low

voltage op-amp is the maximum swing that is obtainable from the output circuit. When the supply voltage goes below the sum of threshold voltages of NMOS and PMOS transistors in the output stage, neither a traditional source follower nor a class-AB amplifier will give a rail-to-rail output swing due to reduction in the linear range of operation. Hence an output stage with a proper biasing circuit to give improved dynamic range and rail-to-rail output swing is required.

In this paper, the Switched Capacitor Based Attenuator(SCBA) to extend the CM range to rail-to-rail at the input and then, Output Drivers (OD) based on floating bias to give the rail-to-rail swing at the output stage have been described in section II. In section III, three different schemes of op-amp with floating bias are presented. Section IV gives the simulation results and V conclusions.

II. Rail-to-Rail input/output stages

A. The input stage

The differential pair input stage of the low voltage op-amp accepts input signals only over a limited range i.e., from V_A to V_{DD} (Fig. 1). But, the requirement is to extend the CM input range to rail-to-rail, i.e., over the entire range from V_{SS} to V_{DD} . In order to address this, a front end SCBA network is designed at the input of the differential pair. The transfer characteristic of SCBA is shown in Fig. 2 and is described by a straight line equation [8].

$$V_{out} = mV_{in} - (m - 1)V_{DD} \quad (1)$$

where $m = \frac{(V_{DD} - V_A)}{(V_{DD} - V_{SS})}$ (slope of the curve) and $V_A = 0.2$ V, a minimum CM voltage level of the differential amplifier, $V_{SS} = -0.6$ V and $V_{DD} = +0.6$ V are used. The transfer function (Eq. 1)(Fig. 2) of the SCBA to be introduced, becomes,

Fig. 2. Transfer characteristic of SCBA.

$$V_{out} = \frac{V_{in}}{3} + \frac{2V_{DD}}{3} \quad (2)$$

Hence, SCBA circuit is proposed to realize the level shifting to cover the entire CM range.

B. Front-End SCBA circuit

It comprises of two SCBA's which are connected to the inputs of the differential pair of op-amp (V_{in}^+ and V_{in}^-). The inputs to SCBA's are v_i^+ and v_i^- . The SCBA accepts rail-to-rail input signal and moves it to the active region of the basic op-amp (Fig.1). The schematic of a typical front-end SCBA used is shown in Fig. 3. A common switch driver is used to drive the switches used in SCBA. The front-end SCBA circuit shown in Fig. 3 drives the in-

Fig. 3. Schematic circuit of SCBA.

put differential stage which is made up of source coupled pair M1-M2 and the folded current mirror M6-M7. Transistors M3-M5 are bias current sources and the diode connected transistors M8 and M9 provide the necessary bias to these transistors. The SCBA consists of two identical parallel paths (P and Q) to supply signal continuously during alternate clock phases to the input of the differential pair. The ϕ_1 and ϕ_2 are two complementary clock phases. The circuit comprises of capacitors C1 to C4 where $C_2 = 2C_1$ and $C_4 = 2C_3$ and switches S1-S8. The switches S1 to S4 are driven by the clock ϕ_1 and S5 to S8 by the clock ϕ_2 . During ϕ_1 , switches S1 to S4 are closed, the capacitors C1 and C2 perform the voltage division operation while C3 and C4 get discharged through S3 and S4. During ϕ_2 , the switches S5 to S8 are closed, the capacitors C3 and C4 share the charges to perform voltage division operation while C1 and C2 get discharged through S5 and S6. Hence, it is clear that SCBA attenuates the signal by 3 and introduces a DC component equal to $\frac{2V_{DD}}{3}$. Thus, the proposed circuit implements Eq.(2).

C. The Rail-To-Rail output stage

It is pointed out in the introduction that as the supply voltage to a class - AB CMOS amplifier is reduced below the sum of two threshold voltages of NMOS and PMOS, both the transistors go to the cut off state under quiescent condition. This reduces the dynamic range and increases output distortion. In order to overcome this problem and to achieve rail-to-rail output swing, the output stage

is driven by two floating biases (Fig. 4) which prevent the output transistors going to cut off state at the quiescent operating condition, ensuring class-AB operation. The prac-

Fig. 4. Class-AB output with floating biases .

tical implementation of the output stage shown in Fig. 4 is used in proposed op-amp schemes constitutes an Output Driver(OD) and the working principle is explained below.

In the scheme 1 (Fig. 5), two floating biases are implemented by using two current sources M14, M15 and two resistors R1, R2 [9] . The current sources together with resistors R1 and R2 set the bias voltages V_M and V_N which in turn control quiescent current I_Q in the output branch. Two common source transistors M16, M17 are used to provide rail-to-rail output swing. A positive signal excursion at node V_k increases VGS16 by V_M and decreases VGS17 by V_N (Eq. 3 and 4).

$$V_x = V_k + V_M \quad (3)$$

$$V_y = V_k - V_N \quad (4)$$

In the scheme 2 (Fig. 6), two floating biases are implemented by using two MOS inverters M12, M13 and M14, M15 and the main advantage of this scheme over the scheme 1 is elimination of resistors R1, R2. The inverters M12, M13 and M14, M15 sets the bias voltages V_y and V_x for controlling quiescent current. According to MOS transistor quadratic law, these variations in gate-to-source voltages produce the necessary changes in the output current such that a true class - AB operation is established. The OD establishes proper biasing at the output stage to drive the output transistors in a class-AB mode. The accurate control of output bias current which is the key issue for high drive capability, large dynamic range and low quiescent power consumption, depends on the magnitudes of the floating biases.

In scheme 3, two floating biases are implemented by using Switched Capacitor (SC) network. Two output transistors M12, M13 are connected in source follower configuration (Class-A). The limitation of this scheme is that it

needs slightly more supply voltage compared with the two previous schemes. The SC network composed of capacitors C1 to C4 ($C1=C2$ and $C3=C4$) and MOS switches S1 to S6 for performing dynamic biasing[10]. The switches are controlled by complementary clock phase ϕ_1 and ϕ_2 . During ϕ_1 the switches S1, S3, S5 are ON , C1 and C3 get charged. During clock phase ϕ_2 switches S2, S4, S6 are ON resulting in charge sharing between C1, C2 and C3, C4.

III. The complete op-amp

The complete op-amps are shown in Figs. 5-7 consists of three main stages viz., input, intermediate and the output stages. The input stage is a folded mirror type differential amplifier with an SCBA circuit whereas the output stages are class-AB and class-A types with floating bias architectures. As the output nodes of the input and intermediate stage are high impedance nodes, they introduce two low frequency poles. The load resistance R_L at the output node introduces a high frequency pole which is well beyond the unity-gain-bandwidth (UGB) of the op-amp. The R-C Miller compensation R_{C1} and C_{C1} is used to provide frequency stability to the op-amp. As the poles and zeros of the front-end SCBA are well beyond the unity-gain-bandwidth (UGB) of the op-amps, it does not introduce any additional poles and zeros within the UGB of the op-amp. The bandwidth of the op-amp is determined by the pole of the input differential stage which is the dominant pole of the op-amp. The compensating capacitor C_{c2} is connected between the output of the intermediate stage and output of the differential stage in order to achieve a single low-frequency pole at the output of the input stage and to move the other pole to a frequency higher than the gain-bandwidth product. Resistor R_{c2} is included to transform the right half-plane zero that arises from the feed forward signal path through the compensating capacitor into high frequency left half-plane zero.

Fig. 5. An operational amplifier:Scheme 1

Fig. 6. An operational amplifier: Scheme 2

Fig. 7. An operational amplifier: Scheme 3

IV. Simulated results

Simulation study has been carried out by using SPICE. A standard $0.5\mu\text{m}$ CMOS process with a threshold voltage of around 0.7 V for both N and P channel transistors is considered. The supply voltages are set to $\pm 0.6\text{ V}$ as indicated. The Table I gives the simulated performances. The clock is set to a frequency of 100 kHz [3]. The DC transfer characteristic of SCBA obtained (Fig. 8), shows that the input CM range of $\pm 0.6\text{ V}$ is converted at the output to a range of 200 mV (V_A) to 600 mV (V_{DD}) as designed. The transfer curve for the complete op-amps under unit follower configuration is shown in Fig. 9. From the figures, it may be noted that addition of SCBA at the input of the differential stage extends the input CM range to 0.6 V . Figs. 10 shows the frequency response of the complete op-amps. The frequency response of SCBA alone is shown in Fig. 11 and it is clear that the total gain has reduced by 9.54 dB ($1/3$) of the total gain. (Eq.2). The frequency responses of the op-amps also shows that there is only one dominant pole within the GBW (Gain Band Width) and this ensures that the circuits are stable [11].

Fig. 8. DC transfer characteristic of SCBA.

Fig. 9. DC transfer characteristics of op-amps under unity follower.

V. Conclusion

In this paper, a SCBA, and OD which extend the input CM voltage range and the output swing to rail-to-rail supply respectively are described. A detailed study on the working of op-amp with the proposed input/output circuit is carried out using CMOS devices with a dual supply of $\pm 0.6\text{ V}$. The simulation study shows that the proposed circuit extends the CM range and output swing to rail-to-rail supply voltage. The pole-zero configuration are also studied to ensure the stability of the circuit. Further, the distortion, output swing and CMMR are evaluated and found to be in close agreement with other op-amps reported in the literature.

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TABLE I
MEASURED MAIN PERFORMANCES

(At $R_L=1k$, $C_L=10pf$)

Parameters	Scheme 1	Scheme 2	Scheme 3
Open loop gain	77.38 dB	81 dB	71 dB
GBW	1.2MHz	1.2MHz	1.67MHz
Phase margin	82 deg	81.5 deg	81 deg
CMRR	130dB	133dB	123dB
THD	-79.5 dB	-76 dB	-96 dB
Supply voltage	$\pm 0.6V$	$\pm 0.6V$	$\pm 0.75V$
Output swing	$\pm 5.4V$	$\pm 5.4V$	$\pm 0.6V$
Power dissipation	$158.4 \mu w$	$157.2 \mu w$	$196.8 \mu w$

Fig. 10. Frequency response of op-amps.

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Fig. 11. Frequency response of SCBA.

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