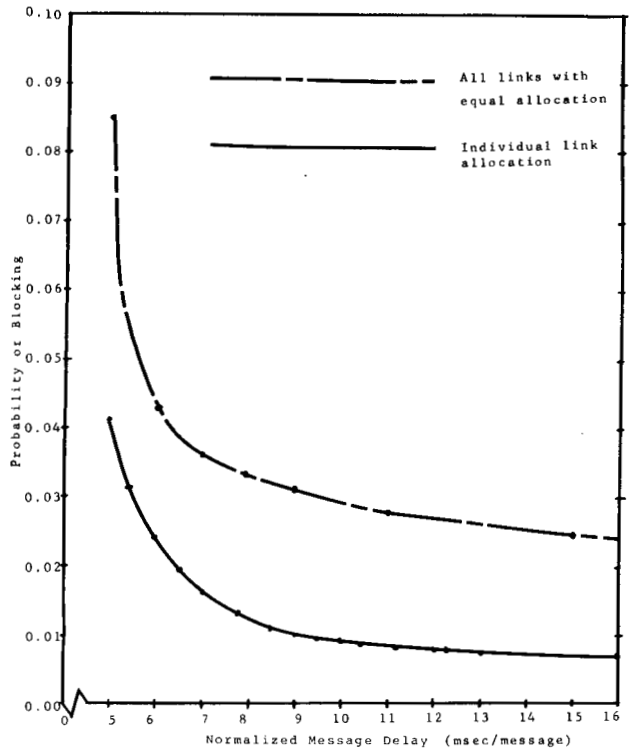

Fig. 6. Probability of blocking with a constraint on message delay—uniform traffic.

delay were presented. These formulas were used in a network capacity allocation problem. The primary tool for solving the problem was linear programming. The results show considerable improvement in performance when capacity is allocated on a link-by-link basis.

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A Class of Companded Unity Bit Coders

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Abstract—**Speech encoding using unity bit coders in the form of delta modulators (DM) has become very popular. Many different designs have been proposed [1]–[3] and implemented in monolithic form [4], [5]. The strategy used in all of these coders is to adapt the "step size" of the coder to suit the input signal power. In the present paper we examine a class of unity bit coders where a basic linear coder is used while the input to this coder is constrained or compressed to be within suitable limits, so as to have the linear coder operating in its optimal range. Results are presented for delta modulators, delta–sigma modulators, and a modified unity bit coder, and it is found that some of the coders perform as well as the "conventional" adaptive delta modulators.**

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INTRODUCTION

Adaptive delta modulators, as analog/digital converters for speech, are becoming serious competitors to the conventional pulse code modulators (PCM). A wide variety of such coders are available [1]-[3] and a few designs have been successfully implemented on monolithic chips [4], [5]. All of these ADM coders have a wide dynamic range brought about by the adaptation of the step size of the coder to match the signal variations. Adaptation of the step size is done either on a sample to sample basis (instantaneous adaptation) [6] or over the envelope duration (syllabic adaptation) [8]-[10].

Alternatively, we could use a linear coder with the input constrained to be within suitable limits. At the decoder the signal will have to be appropriately expanded. This idea was first proposed by Stephanne and Villert [11] and some improved versions have been reported [12]. The same principle has also been successfully applied for PCM/DPCM coding as well [13], [14].

In this paper we present the realization of a class of such coders and discuss the results obtained with these coders. The important difference from the technique of Stephanne and Villert [11] is in the fact that the companding signal is obtained from the coder output rather than from the input signal, which ensures that the coder and decoder have the same signal for compression and expansion.

Different alternatives are suggested for extracting the control signal, and the designs of the different schemes are outlined.

CODING ALTERNATIVES

The basic coding scheme is shown in Fig. 1. The input to the linear coder is obtained through a compressor while the signal that is used for companding is derived from the output of the coder. At the receiving end, an expansion operation has to be performed. The linear coder can be a delta modulator, a delta-sigma modulator, or any other form of unity bit coder. It should further be noted that at all times the predictor is inside the companding loop.

The extraction of the control signal itself can be achieved in different ways. The well-known technique of the continuously variable slope delta modulator (CVSD) yields a signal that varies in accordance with the input envelope. This will therefore involve the use of a divider at the encoder [Fig. 2(a)] and a multiplier at the decoder. Since the use of a divider is not always convenient, one can just utilize a multiplier by forming the reciprocal of the control signal. This is rather simply achieved by filtering the complement of the coincidence detector output rather than the normal output, while the decoder utilizes the coincidence detector output directly [12].

The other way of extracting the control signal is to use the method outlined in [10] [Fig. 2(b)]. We obtain a signal that is inversely proportional to the input amplitude and the use of a multiplier will produce the compression at the input. The decoder must therefore employ a divider to restore the proper signal level.

We will refer to these two methods as the digitally controlled and the analog controlled coders, respectively, consistent with the terminology used in [8].

An alternative method of realizing the compressor/expander would be to use a gain-controlled operational amplifier with an FET as the control element. The resistance of the

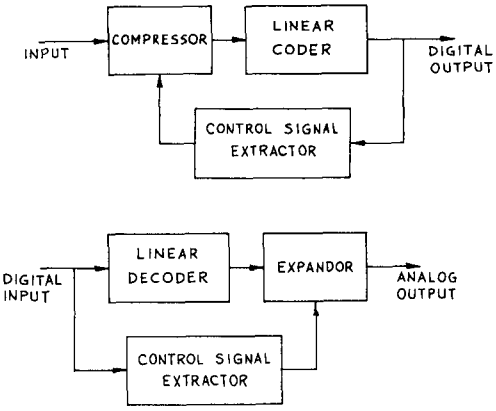

Fig. 1. General form of the companded coder.

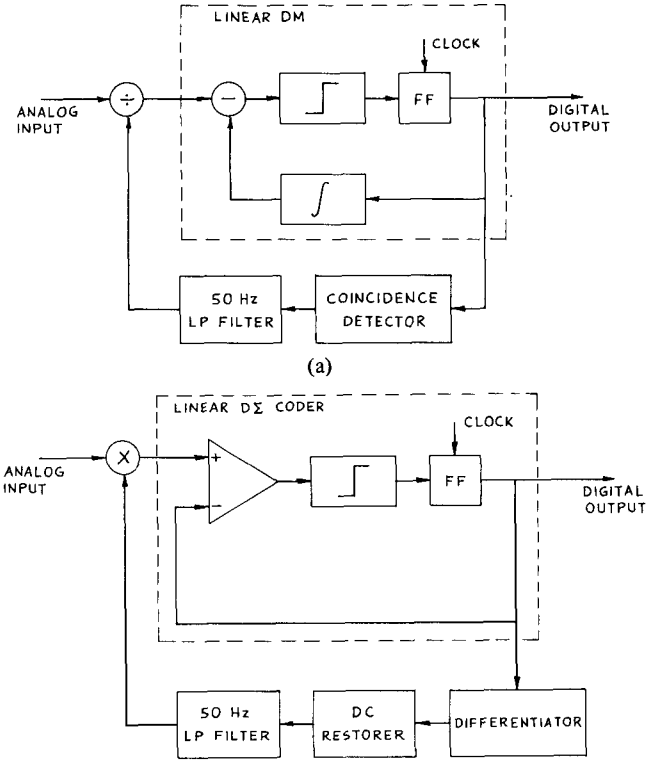

Fig. 2. (a) Block diagram of the companded DM (digitally controlled). (b) Companded DΣM (analog controlled).

FET is changed by the control signal. The position of the FET decides whether compression or expansion is performed.

We have suggested a few alternatives for realizing the companded codes. Apart from these we have one more method[1] of realizing our goal.

The system described in [13] uses an antilog amplifier for the division. A signal proportional to the logarithm of the divisor is generated and used to control the gain of an antilog amplifier. The result is the division of the input by the required value. A simple change of sign in the control signal ensures the multiplication at the decoder for expansion.

If an identical approach is to be adopted here, the generated control signal must be processed in a log amplifier, the

1 The author thanks one of the reviewers for suggesting this comparison.

output of which controls the antilog amplifier. Suitable sign changes must be made to take into account the two different methods used in extracting the control signal.

The above-mentioned strategy is very well suited for the systems studied in [13] where the divisors take on discrete, nonzero values whose magnitude is not very small. However, in the present case, the control signal in either of the methods can become zero or have very small values. This will cause the log amplifier to malfunction and degrade the performance.

This can be avoided by using only an antilog amplifier and settling for some form of compression. The difficulties encountered when the control signal becomes zero may be overcome by the addition of a small bias. The bias, however, will be a critical value since it has to be provided at the decoder also. This method is expected to offer better linearity as compared to schemes reported.

When we consider the inner coder, the use of a DM will be advantageous since it provides a higher SNR. The delta-sigma modulator, on the other hand, has a constant SNR at all input frequencies, although the magnitude of the SNR is lower. The integrator break point can be varied to obtain the best compromise.

Apart from the above-mentioned coders we can use a modified coder [15] and obtain the advantages of the delta-sigma coder without much sacrifice in the SNR. The coder for this purpose is illustrated in Fig. 3. We call this the two loop coder because of the additional feedback loop around the basic coder.

This coder employs an additional feedback loop around a DM to improve the SNR at higher input frequencies. Without the inner loop, this coder is basically a delta-sigma modulator. The addition is the filter to cut off the out-of-band noise in the feedback path. The inner loop aids in keeping the system operating at low or zero input conditions when the filter output will be zero. An adaptive version of this is described in [8]. The designer has the choice of other techniques also, namely, the noise feedback coder described by Tewkesbury and Hallock [16].

Thus, we have a family of coders with companding performed on the input. The technique of compression and the form of the inner coder are the differentiating factors. The coders have been compared using the following criteria. First, the degree of compression produced has been compared by plotting the compression characteristics and then the dynamic range, with the SNR as the figure of merit. The different coders studied have also been compared with a commercially available CVSD Coder (Motorola's MC 3418).

RESULTS

Figs. 4 and 5 show the results of the various measurements carried out on the different coders implemented in hardware. Fig. 4 compares the compression characteristics of the two methods of extracting the control signal for companding. The plot shows the input to the linear coder as a function of the input signal. The compression achieved is good and the first scheme of using a coincidence detector appears to be the better strategy. Unlike in a conventional adaptive DM codec, the linearity of the coder/decoder pair is important, since the decoder differs from the feedback path of the coder. The linearity of the coders has been measured and found to be good. The most common figure of merit for digital coders is the SNR, and the SNR for a delta-sigma modulator (DΣM), DM, and the two-loop coder appear in Fig. 5. The

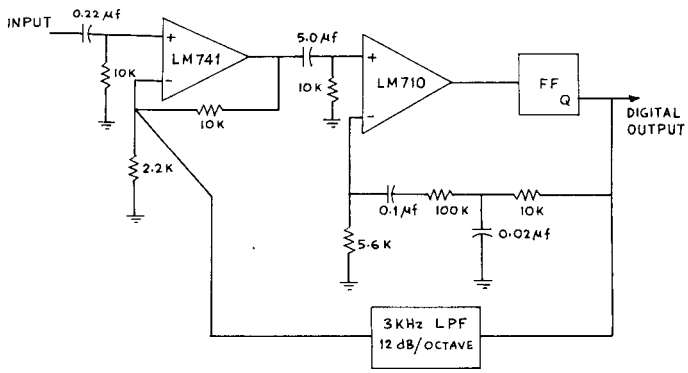

Fig. 3. Circuit diagram of the two-loop coder.

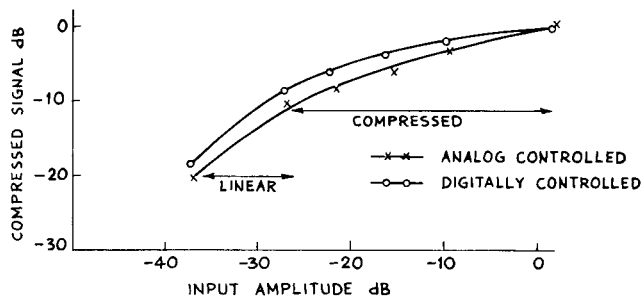

Fig. 4. Compression characteristics.

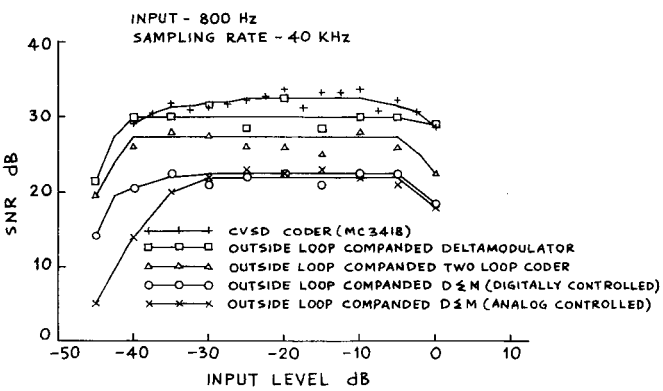

Fig. 5. SNR versus input characteristics.

DΣM case comprises both the compression schemes while the other coders have been implemented using only the CVSD strategy, since this is found to be the better of the two. As to be expected from Fig. 5, the dynamic range for the digitally controlled coder is greater than that for the analog controlled coder. The SNR for the modified unity bit coder is better than that of the DΣM by about 4 dB. Also shown in Fig. 5 is the SNR for a CVSD coder for which Motorola's MC3418 integrated coder has been used. The CVSD and the companded DM perform almost alike. In fact, subjectively the difference is not noticed at all. All measurements have been made at a bit rate of 40 kbits/s, the input signal used being an 800 Hz sinusoid. The improvement in the SNR with increase in the bit rate is of the order of 9 dB/octave, which is to be expected.

The companded two-loop coder is better than the flat spectrum coder described in [8]. This is because the latter has the adaptation gain in the same path as the low-pass filter used and the phase shift of the filter tends to make the system unstable.

The most vital test for a coder is, however, the subjective assessment. Although no detailed comparison of the different coders has been made, the DΣM has been found to offer an acceptable quality of speech while the DM and the modified coder offer toll quality speech at 40 kbits/s.

CONCLUSIONS

We have presented an overview of some of the different methods of realizing a companded unity bit coder where the companding is carried out on the input signal while a linear coder is used to code this compressed signal. Two different methods of extracting the control signal have been presented. One method involves the detection of the presence of digital output bits of the same polarity while the other involves the differentiation of the coder output and filtering, so as to end up with a signal that is inversely proportional to the input envelope. Whatever the companding scheme, the DΣM performs the poorest. A tradeoff between SNR and frequency response (SNR versus frequency) is possible by the use of a two-loop companded coder, which is attractive at lower bit rates, because of its better high frequency reproduction. The quality of speech in the companded DM is the same as that in the CVSD coder.

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Comparison of Adaptive Linear Prediction Algorithms in ADPCM

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Abstract—**A comparison of adaptive differential pulse code modulation (ADPCM) speech compression systems is made using different recursive adaptive linear prediction algorithms. The particular algorithms considered are 1) a fixed predictor, 2) the adaptive least mean square (LMS) transversal predictor, 3) the LMS (gradient) lattice predictor, 4) the least squares (LS) lattice predictor, and 5) an LS lattice predictor combined with a third-order pitch inverse filter. The last configuration uses the pitch detection scheme described in [21] to recursively estimate the pitch period in the context of an adaptive predictive coder (APC). The results indicate that for the conditions simulated, the difference in system performance using the different adaptive algorithms is negligible, suggesting that the predictor having the simplest implementation is the best.**

I. INTRODUCTION

This paper reports results obtained from a series of simulations of adaptive differential pulse code modulation (ADPCM) speech compression systems using different recursive adaptive linear prediction algorithms. A block diagram of an ADPCM system is shown in Fig. 1(a). The adaptive (or fixed) linear predictor forms an estimate $\hat{y}_i$ of the current speech sample y_i, and the causal prediction residual e_i is quantized ($\tilde{e}_i$) and sent to the receiver. The received (quantized) data sample is denoted as $\tilde{y}_i$. Also shown in Fig. 1 is an adaptive quantizer, which adjusts the quantizer step size relative to the short-term prediction error power.[1]

Any fixed or adaptive linear predictor may be used in ADPCM. Because prediction alogrithms vary greatly in com-

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[1] To avoid confusion we state here that throughout this paper "ADPCM" refers to a DPCM coder with an adaptive quantizer and either a fixed or adaptive predictor. Furthermore, the configuration in Fig. 1(b) will be referred to as an "adaptive predictive coder (APC)."

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