A simple and inexpensive two channel boxcar integrator

R K SHENOY, J RAMAKRISHNA and K R JEFFREY*
Physics Department, Indian Institute of Science, Bangalore 560 012
*Physics Department, University of Guelph, Guelph, Ontario, Canada

Abstract. A two-channel boxcar integrator with an analog to digital converter was constructed using integrated circuits wherever convenient. The digital output can be instantaneously displayed or displayed after accumulating many samplings in the totaliser. The totaliser mode provides averaging at the digitiser level and hence the integrator has an infinite holding time. When used in the double boxcar mode the instrument overcomes the problem of any base line instability.

Keywords. Boxcar integrator; gated integrator; analog-digital converter; totaliser.

1. Introduction

Boxcar integrators are widely used in pulsed NMR measurements to improve the signal-to-noise ratio. Most of the circuits described in the literature (Allen *et al* 1970; Blume 1961; Clark and Kerlin 1967; Hodby 1970; Niemela 1972; Packer and Strike 1970; Reichert and Townsend 1964; Samuelson and Ailion 1969; Sandhu 1974; Stejskal 1963; Ware and Mansfield 1966; Woessner *et al* 1969) do not incorporate a digital display and the few that contain systems for digital conversion are based on commercial units and are therefore generally expensive. In this paper we describe a simple and inexpensive two channel boxcar integrator with digital output, built from readily available components. This unit has been in use with our home-made pulsed NMR spectrometer and its performance is very satisfactory.

A boxcar integrator, in general, has basically two modes of operation—the single point mode and the scan mode. In the single point mode a certain segment of the transient repetitive signal is sampled and stored. Successive samplings are added to the previous ones, building up the signal-to-noise ratio. On the other hand, in the scan mode, the sampling point is moved to cover the entire signal, thus retrieving the complete signal point by point with an improved signal-to-noise (S/N) ratio. The boxcar integrator described in this paper operates in the single point mode. It can be used as a single channel boxcar or as a double boxcar wherein the difference between two signals is measured. In the double boxcar mode the signal is sampled in one channel and the base line is sampled for an equivalent time in the other channel. This mode has the advantage of reducing the background and also reducing the effect of any base line instability that may be present.

2. Description of the circuit

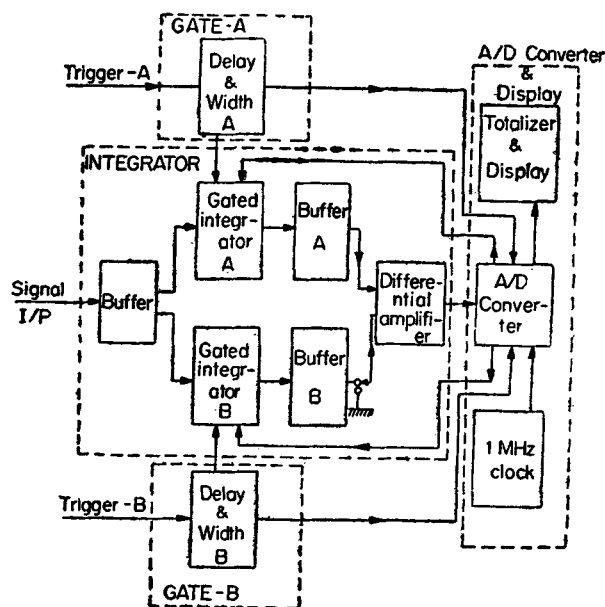The block-diagram of the circuit is shown in figure 1. The timing and duration of the

Figure 1. Block diagram of the boxcar integrator.

gating pulses are controlled by the delay and width units.   The signal at the input of the gated integrator is integrated during the sampling pulse, amplified and converted to digital form and displayed.   The circuit is divided into three sections: (1) the gating time circuit, (2) the gated integrator, (3) A/D converter and display.   Extensive use has been made of integrated circuits in the fabrication of this instrument.

2.1. *The gating time circuit*

Figure 2 shows the circuit used for controlling the delay and the duration of the sampling pulses. It consists of four SN74121 IC monostable multivibrators $(M_1 – M_4)$. A reference pulse synchronous with the trailing edge of the transmitter gating pulse (of the pulsed NMR spectrometer) is derived from the pulse programmer (Shenoy *et al* 1976) and is used to trigger M_1 or M_2 to generate the delay. The delay could be adjusted from 40 nsec to 10 sec.   The trailing edges of the delay pulses trigger the monostable multivibrators M_3 or M_4, thus generating the sampling pulses. The width of the sampling pulse may be varied between 40 nsec to 100 msec. The sampling pulse is also used in the digitiser for other time functions. When used as a single channel boxcar only trigger *A* is required; as a two channel boxcar two separate triggers (*A* and *B*) are required for triggering these monostables. However in the two channel mode the same trigger can generate both sampling pulses, but with different delays for the two channels.

2.2. *The gated integrator*

The transistor-transistor-logic (TTL) compatible, high speed MOS analog switches AH0019CD (National Semiconductor) are used as the gates (*G1* and *G2*) in the gated
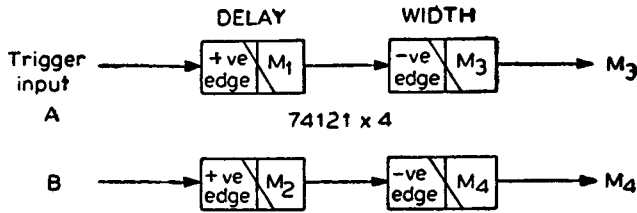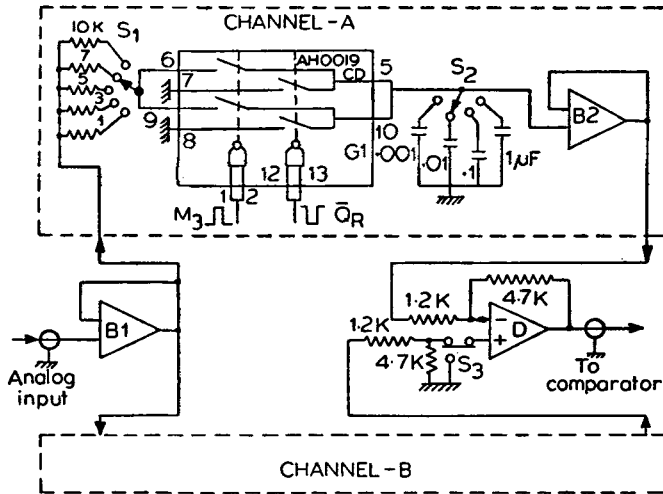
Figure 2. Gating time circuit.

Figure 3. Gated integrators (Channel *A* and *B* are identical) with common input buffer (*B*1) and output diff. amp. (*D*).

integrators (figure 3). This switch has a low resistance when ' on ', and a high resistance when ' off ', typically 200 ohms and 10^{11} ohms respectively. It can also handle large analog voltage inputs (± 10 V). The AH0019CD is a dual DPST switch, in which the output pins 5 and 10 (figure 3) are both connected to the integrating capacitor (S_2). The input pins 6 and 9 are both connected to the analog signal through the integrating resistor (S_1). These two inputs are connected to the output when the sampling pulse is applied at pins 1 and 2. The other pair of input pins 7 and 8 are grounded. The integrator condenser is charged to the signal value through the resistor with a characteristic learning time ($\sim$RC), when the sampling pulse is ' on '; and the charge is held on the capacitor till the end of the reset pulse. When the reset pulse, which is obtained from the $\bar{Q}$ output of the A/D converter flipflop (*R* or *S*), is applied at pins 12 and 13, the integrating condenser is discharged. Between the end of sampling pulse and the reset, the analog signal is converted into digital form by the A/D converter and stored and displayed by the totaliser. The integrator capacitor must hold the charge until the information is processed by the digitiser. This condition is satisfied if the ' off ' resistance of the switch is very high and the capacitor has low leakage. The gate used satisfies the first condition and low leakage mylar capacitors are used as storage elements to satisfy the second condition. It is also necessary to minimise the leakage into the input of the following circuit. NE536 FET input op. amps,

(National Semiconductor) are used in the voltage follower configuration to buffer both the input ($B1$, common to both the channels) and the output ($B2$ and $B3$; the latter is not shown in figure 3) of the gated integrator. The high input impedance of the FET op. amps, which is of the order of the gate ' off ' resistance, minimises the drift due to input leakage currents. (Actually the drift in the charge on the integrator capacitor is determined by the leakages currents of the gate and the buffer, which are typically of the order of 40 pA and 30 pA respectively). The outputs from the buffers ($B2$ and $B3$) are fed to the two inputs of a differential amplifier (D). Channel A buffer is fed to the inverting input and that of channel B is connected to the non-inverting input. In the single channel mode the non-inverting input is grounded (Switch $S3$). Again the FET input operational amplifier is used as differential amplifier with a closed loop again of 8 db.

2.3. *A/D converter and display*

The A/D converter (Wittlinger 1974) is a closed circuit type consisting of a 1 MHz crystal clock, a staircase generator, a level shifter, a comparator and a pair of set-reset flip-flops R and S, for the two channels (figure 4).

2.3a. *Linear staircase generator:* A CA3033 op. amp. (RCA) is used as a linear stair-case generator (P) with a capacitor C_1 and diodes D_1 and D_2 at the input and a capcitor C_2, with a BFW 10 (Mullard) switch across it, in the feed back loop. When the switch is opened and the pulses from the 1 MHz clock are applied to the input, the output is a negative going staircase voltage. The switch is activated by the output Q of the flipflop R (or S). A pulse of amplitude e at the junction of the 10K resistor and capacitor C_1 couples a charge Q to the amplifier input. The charge Q is equal to
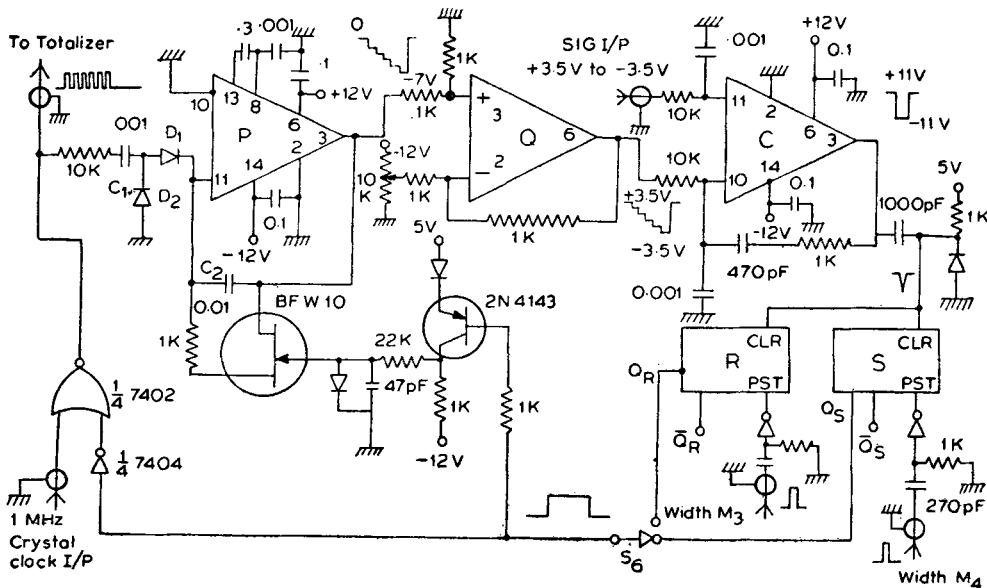

Figure 4. A/D converter (*P*-CA3033 staircase generator, *Q*-NE536 level shifter, *C*-CA3033 comparator, *R* & *S*-7474 flip-flops. All diodes are IN914).

$C_1(e-2V_{ak})$, where $2V_{ak}$ is the forward voltage drop across the two diodes. The capacitor is incrementally charged in steps of $(e-2V_{ak})C_1/C_2$. Thus when the switch is open the staircase output runs down until it compares with the analog signal input at the comparator. After this the switch is closed and the charge on the capacitor C_2 is grounded. The step height of staircase has been adjusted to 5 mV.

2.3b. *Level shifter:* A NE536 is used as a level shifter (Q) before the comparator as shown in figure 4. In the absence of this, the analog signal must lie between 0 and —7V. But we find that in some experiments e.g. T_1 measurement by inversion recovery method, the signal takes both negative and positive values. To take this change in polarity of the signal into account, the limits of the output voltage of the staircase are level shifted from 0– —7V to +3·5– —3·5 V.

2.3c. *Comparator:* The output of the staircase generator, after being level shifted, is connected to the non-inverting input of a CA3033 used as a comparator (C), where it is compared with the analog voltage appearing at the inverting input. The comparator output changes from 11 V to —11 V when the inputs are equal. The 470 pf capacitor and the 100 ohm resistor between output and non-inverting input provide the necessary regeneration to accelerate the transition when the input voltages are equal. Two 0·001 μfd capacitors on each input filter any externally generated noise.

2.3d. *7474 flip flops:* The two flip flops R and S (SN 7474) initiate and reset the A/D convertor circuit as well as operate the switches controlled by pins 12 and 13 of AH0019CD in the gated integrator ($G1$ and $G2$). The charge on the integrating capacitor (S_2) in figure 3 has to be held till it is digitised. Digitisation is complete when the comparator changes state, and this change of state triggers the flip flop R (or S). The output Q of R (or S) disables the NOR gate and clock pulses are prevented from reaching the staircase generator. At the same time, the $\overline{Q}$ output of the flip flop R (or S) grounds the integrating capacitor (S_2) and holds it at ground potential until the next sampling pulse occurs. The leading edge of this sampling pulse triggers flip flop R (or S) so that output Q initiates the A/D converter, while output $\overline{Q}$ opens the switch which grounded the capacitor (S_2) thus enabling it to be charged again.

Switches S_3 at the input of the differential amplifier (D) and S_6 of the digitiser are the parts of a DPDT switch, which select either the single channel or two channel mode as required.

2.3e. *Totaliser:* The totaliser (figure 5) counts the number of pulses in each burst at the output of the NOR gate in the A/D converter circuit. In the display and erase (DAE) mode, the number of pulses in one burst is counted and displayed till the next burst begins. Just before the beginning of the next burst, the display of the previous burst is erased—hence the name. In the totaliser mode, the number of pulses in n bursts are added together and displayed. n can take the values 1, 10, 100 or 1000. Switch S_8 selects the mode of operation.

The number of pulses in a burst is counted by a series of decade counters (SN7490) and displayed on HP5082-7300 numeric displays (Hewlett Packard). In the DAE mode, the counters are cleared by trigger A. In the totaliser mode, the counters are
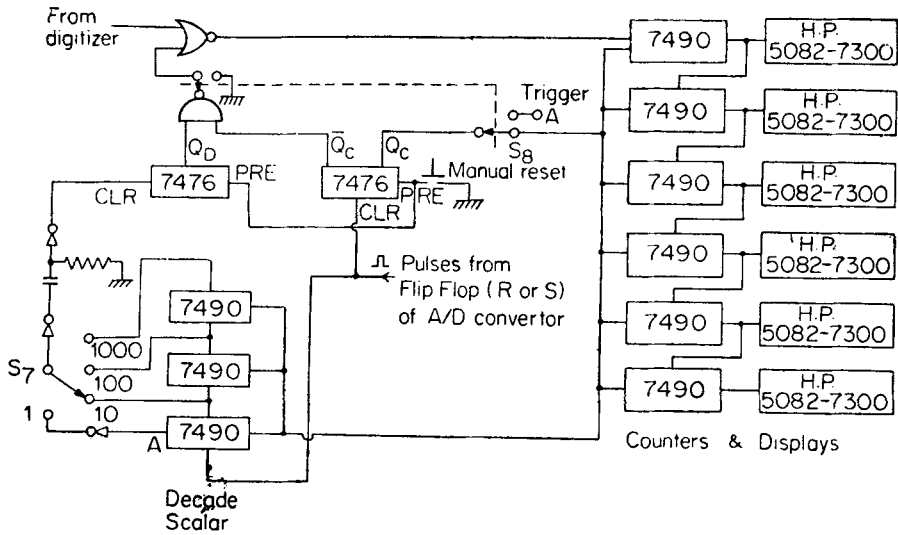
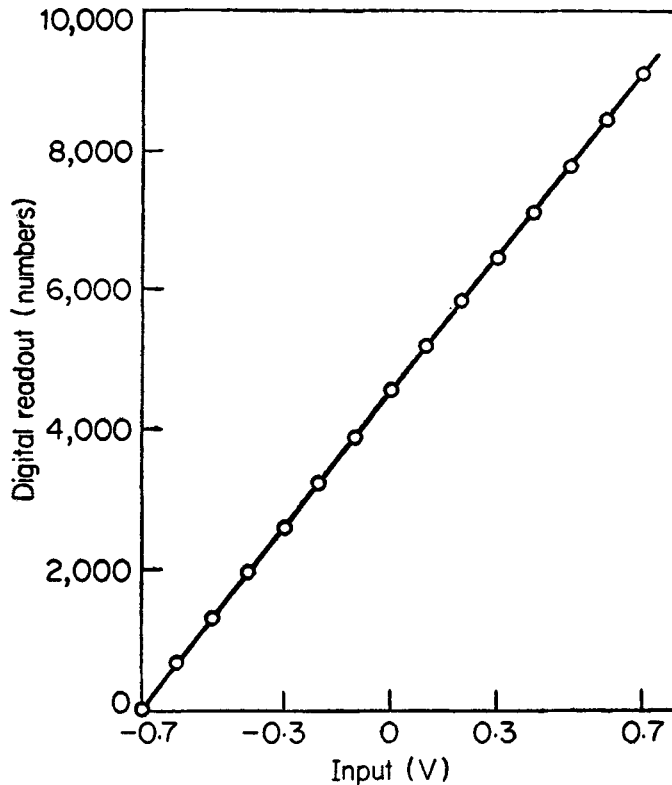**Figure 5.** Totaliser.

Figure 6. Boxcar integrator digital read-out vs input-voltage in the totaliser mode.

not cleared until n bursts pass through. A decade scalar is preset to the value n and then counts down using the pulses from output Q of flip flop R (or S) of figure 4. For accurate counting, it is essential that all the pulses in a burst are counted. The

decade counters, the flip flops, Q_C and Q_D and the NAND gate are used in such a way as to open the NOR gate at the input of the totaliser well in advance of the burst of pulses and close it well after the burst. This ensures complete counting of the pulses. The totaliser has to be manually reset after the decade scalar counters have finished counting the preset number of bursts of pulses.

3. Conclusions

The step height in the A/D converter is 5 mV and the input to this circuit can be ± 3.5 V. The resolution, therefore, is better than 0.1 %. Because of amplification in the differential amplifier the analog input voltage is limited to ± 1.5 V.

A check of the linearity of the instrument was carried out and the results are shown in figure 6. An anlysis of these results shows that the linearity is about 0.1 % in the DAE or totaliser mode.

Acknowledgement

References

Allen P S, Harding W and Jocelyn M 1970 *J. Phys.* E 3 749
Blume R J 1961 *Rev. Sci. Instrum.* 32 1016
Clark W G and Kerlin A L 1967 *Rev. Sci. Instrum.* 38 1593
Hodby J 1970 *J. Phys.* E 3 221
Niemela L 1972 *J. Phys.* E 5 526
Packer K J and Strike A J 1970 *J. Magn. Resonance* 3 503
Reichert J and Townsend J 1964 *Rev. Sci. Instrum.* 35 1692
Samuelson G L and Ailion D C 1969 *Rev. Sci. Instrum.* 40 676
Sandhu H S 1974 *J. Magn. Resonance* 13 379
Shenoy R K, Ramakrishna J and Srinivasan R 1976 *J. Phys.* E 9 779
Stejskal E O 1963 *Rev. Sci. Instrum.* 34 971
Ware D and Mansfield P 1966 *Rev. Sci. Instrum.* 37 1167
Wittlinger H A 1974 RCA Solid State Data books—*Linear integrated circuits and MOS Devices* (Application notes only)
Woessner D E, Snowden Jr. B S, McKay R A and Strom E T J 1969 *J. Magn. Resonance* 1 105