Input Voltage Sensorless Average Current Control Technique for High-Power-Factor Boost Rectifiers Operated in Discontinuous Conduction Mode

Rajesh Ghosh **G. Narayanan**
Power Electronics Group, Department of Electrical Engineering,
Indian Institute of Science, Bangalore-560012
rajesh@ee.iisc.ernet.in gnar@ee.iisc.ernet.in

Abstract – **A simple, low-cost analog controller is proposed for average current mode control of high-power-factor boost rectifiers operated in the discontinuous conduction mode (DCM). The current shaping is based on comparison of the input current with a suitably generated periodic nonlinear carrier. The controller does not need input voltage sensing, error amplifier in the current-shaping loop and/or any multiplication / division operation. The performance of the proposed controller is comparable to those of existing schemes. The controller may be fabricated into a single integrated circuit. A 600W rectifier is simulated in MATLAB/SIMULINK. The control concept is experimentally validated on a 600W laboratory prototype.**

I. INTRODUCTION

Single-phase ac-dc PWM converters are widely used for rectification at high input power factors. The converter may be designed to operate either in the continuous conduction mode (CCM) or in the discontinuous conduction mode (DCM). A converter operated in the DCM has higher device currents. It requires an additional low pass filter at the input to filter the switching harmonics in the source current. However, it also offers a number of advantages over its CCM counterpart such as simpler transfer function, ease of control, zero current turn on, minimum diode reverse recovery and reduced inductor size. Hence DCM converters are increasingly used in applications such as UPS and battery charger, and in applications where size, weight and cost are major concerns.

A number of control techniques are reported in the literature for boost rectifiers operated in the DCM. Among them voltage follower approach is the simplest [1]. The converter operates at a constant switching frequency and a fixed duty ratio with a single output voltage sensor. It has drawback of having low frequency harmonics (3_{rd}, 5_{th} etc) present in input current along with fundamental. Bulk input filter is required to remove these lower order harmonics. Other techniques like second harmonic injection [2], varying duty cycle (divider approach) [3], multiplier approach [4] and operation at CCM-DCM boundary (variable switching frequency) [5] use input voltage sensing. These can give high quality input current at the cost of either complicating the control circuitry and/or using mathematical operations such as division, multiplication and square root. These make the analog implementation complicated. As these types of converters are mostly used in low power applications, a low-cost and simple controller solution is preferred.

Nonlinear Carrier Controllers (NLC) have proved their simplicity and efficiency over conventional controllers in the field of active current shaping [6-7]. The current mode control is implemented in a simpler way without sensing the input voltage and using any multiplication/division/square-root operation. The absence of error amplifier in the current loop makes the current controller much faster compared to conventional controllers.

So far these controllers find their applications only in converters operated in CCM. Their performance deteriorates when operated under DCM [6].

The purpose of this paper is to propose a simple, low-cost, analog controller for single-phase, single-switch DCM boost rectifier, which has the simplicity like voltage follower technique [1] or the NLC controllers, and the performance like converters with control reported in [2 -5]. The proposed controller is suitable for being fabricated into a single integrated circuit.

II. CONTROL SCHEME

A single-switch, single-phase boost rectifier operated in the discontinuous conduction mode is shown in Fig. 1. The current through the inductor L_b over a switching interval T_s is as shown. An input low pass filter is used for filtering the high frequency harmonics in the source current.

A. Expression of Switch Duty Ratio D.

Referring to Fig. 1, in each switching interval T_s, the converter switch S is turned on for duration DT_s. The boost inductor current i_g increases linearly to its peak value I_P. At the end of this interval, the switch S is turned off. The inductor current i_g falls linearly to zero at the end of the

0-7803-8975-1/05/$20.00 ©2005 IEEE.

second interval D_1T_s. It remains zero for rest of the switching interval D_2T_s. The peak current and the average current through the inductor can be expressed as shown in (1) and (2) respectively. Solving (1) and (2) yields the expression for switch duty ratio D as shown in (3) [8].

$$I_P = \frac{V_g D T_s}{L_b} = \frac{(V_O - V_g) D_1 T_s}{L_b} \quad (1)$$

$$I_g = \frac{1}{2}(D + D_1) I_P \quad (2)$$

$$D^2 = \frac{2 I_g (V_o - V_g) L_b}{V_o V_g T_s} \quad (3)$$

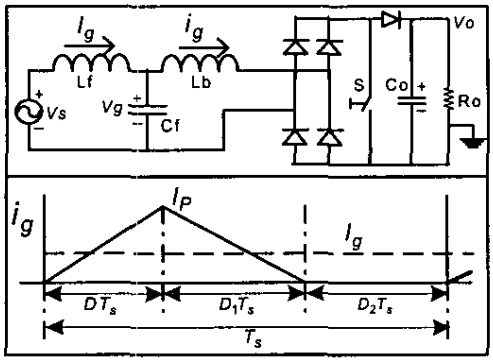

Fig. 1 Single-phase DCM boost rectifier (Top), Inductor (L_b) current in a switching cycle (bottom)

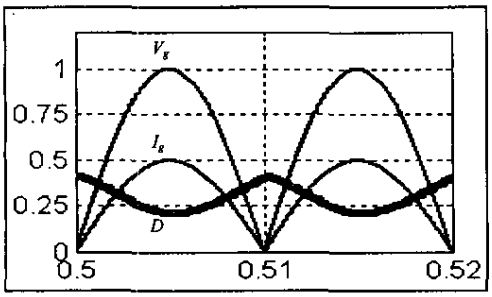

Fig. 2 Variation of duty ratio D over a fundamental

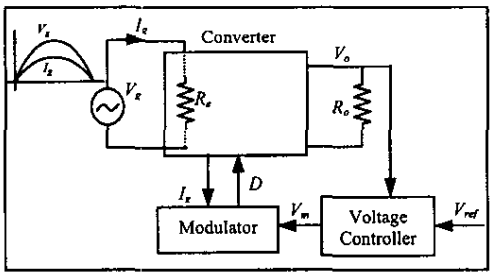

Fig. 3 Resistor emulator

B. *Control Objective*

The control objective is to maintain the average inductor current I_g proportional to the average input voltage V_g in each switching cycle, in addition to maintaining the output voltage V_o constant at the desired reference level (see Fig. 2). The converter is seen as a resistance R_e by the source as shown in Fig. 3. It can be said to emulate a resistance R_e as defined in (4). The converter output voltage V_o can be controlled by regulating the input power to the converter. This is achieved by controlling R_e. R_e can be controlled by the voltage controller output signal V_m as shown in (5), where R_s is the gain in current sensing path [9-10].

$$I_g = \frac{V_g}{R_e} \quad (4)$$

$$V_m = \frac{V_o R_s}{R_e} \quad (5)$$

A typical variation of the duty cycle required to achieve (3) is shown Fig. 2.

C. *Simplification of the Duty Ratio Expression*

The switch duty ratio D can be calculated by solving (3) analytically [8]. This involves complex operations like multiplication, division and square root operation along with input voltage sensing. These make the analog implementation difficult.

In the present work, (3) has been simplified using (4) and (5) to make the analog implementation easier. The simplified control equation of the proposed controller is shown in (6). As the converter has a single switch, the absolute value of I_g is considered in (6). The control equation does not depend on the load resistor R_o.

$$V_m - D^2 \left(\frac{R_s T_s}{2L_b}\right) V_o = |I_g| R_s \quad (6)$$

D. *Nonlinear Carrier*

In each switching interval T_s, let us consider a parabolic carrier $v_c(t)$ as defined in (7). At the beginning of each switching interval it starts with a zero value. At time ($t=DT_s$) it equals the second term in the LHS of (6). Hence this carrier may be used to determine the switching instant. The shape of the carrier is shown in Fig. 4. The carrier can be generated by double integration as shown in (8).

$$v_c(t) = \left(\frac{R_s V_o}{2L_b T_s}\right) t^2 \quad (7)$$

$$v_c(t) = \left(\frac{R_s V_o}{2L_b T_s}\right) t^2 = \left(\frac{R_s V_o}{L_b T_s}\right) \int_0^t \left(\int_0^t 1 * dt \right) dt \quad (8)$$

E. *Generation of Gating Pulses*

Referring to Figs. 4 and 5, a clock pulse generator with narrow pulse width and time period T_s is used in the controller. Two cascaded integrators are used to generate the required carrier as defined in (8). In the beginning of each switching cycle, the rising edge of the clock resets both the integrators. The turn on and turn off instants of the converter switch is obtained by comparing the absolute value of the source current with the signal $(V_m - V_c(t))$ in a comparator. The comparator output directly drives the converter switch S through a gate driver (not shown). In each switching cycle the switch S is turned on for duration DT_s.

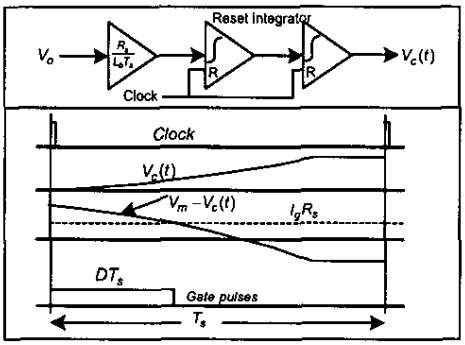

Fig. 4. Gate pulse generation

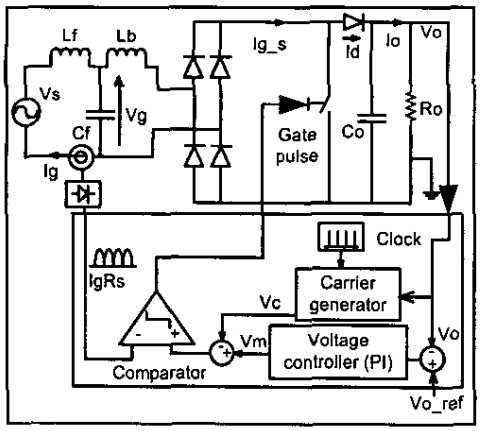

Fig. 5. Proposed controller

In Fig. 4 the clamped portion of $v_c(t)$ is due to integrator saturation. This does not affect the operation, as the clamped portion of $(V_m - v_c(t))$ is always below zero level, where as $|I_g R_s|$ is always positive.

III. Different Methods of Current Sensing

Referring to the control equation (6), the controller requires the absolute value of the average input current I_g to determine the duty ratio D. There are a number of ways to obtain this.

A. *Source Current Sensing*

A low pass filter is used at the input of the DCM converter as mentioned earlier. The current through the inductor in this low pass filter can be regarded as the average source current. This current is sensed and fed to the controller. Since the controller requires the rectified / absolute value of the input current, an active rectifier (op-amp based) may be used as shown in Fig. 5.

B. *Boost Inductor Current Sensing*

The current through the boost inductor (L_b) is filtered using an op-amp based low-pass filter, and rectified using an active rectifier. This is then used for computation of duty ratio.

C. *DC Bus Current Sensing*

In the first two methods of current sensing, an electrically isolated current sensor is required if the control ground is connected to the negative rail of the dc bus. DC bus current sensing does not require such an electrical isolation.

In this method a low valued resistor is inserted in the negative rail of the dc bus as shown in Fig. 6. The output current is rectified, but is pulsating. The discontinuous dc bus current may be integrated over each switching cycle to get the required average input current. An additional integrator with reset may be used. Two approaches may be followed.

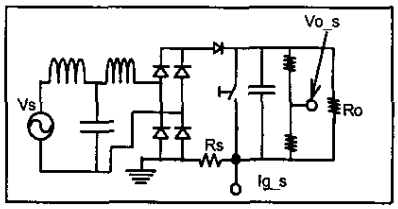

Fig. 6 DC bus current sensing

(i) *With Sample and Hold*

In this approach the reset integrator starts integrating the dc bus current at the beginning of each switching interval. At the end of each switching interval, its output is sampled and held by a sample and hold circuit before the output being reset. The output of the sample and hold circuit is used as the average input current to compute the duty ratio for the next switching cycle. There is a delay of one sampling period T_s in current sensing. However, the delay has negligible effect on the performance of the converter since the switching frequency is high.

(ii) *Without Sample and Hold*

In this method the integrator starts integrating the dc bus current at the end of first interval DT_s as shown in Fig. 7. Because of high switching frequency it may be assumed that the duration $Ts\_1 \approx Ts$, the switching interval. Hence the integral of the inductor current over the interval Ts_1 can be taken as a measure of the average inductor current Ig_i. The integrator is reset by the falling edge of the gate pulse. In this method the sample and hold is not required and the reset integrator output can be directly used for the duty ratio computation.

DC bus current sensing also gives information about the instantaneous device current. This may be used for peak current protection of the converter switch.

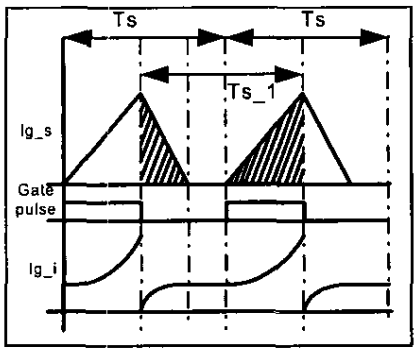

Fig.7 Average current computation

IV. CCM-DCM BOUNDARY

The proposed controller has been designed for operation in the discontinuous conduction mode. This section determines the boundary between CCM and DCM operation.

Let us define two-voltage ratios m_g and M_g as shown in (9) and (10), respectively, where ω is the supply angular frequency, and V_{gm} is the peak input voltage.

$$m_g = \frac{|V_g|}{V_o} = \frac{|V_{gm}\sin(\omega t)|}{V_o} \tag{9}$$

$$M_g = \frac{V_{gm}}{V_o} \tag{10}$$

Under CCM the duty ratio D may be expressed as shown in (11) [6]. The duty ratio under DCM, given in (3), is rewritten in (12a), where K is the conduction parameter of the converter and R_o is the load resistance.

$$D = 1 - \frac{V_g(t)}{V_o} \tag{11}$$

$$D = \sqrt{\frac{2I_g(V_o - V_g)L_b}{V_o V_g T_s}} = \sqrt{\frac{(1-m_g)KR_o}{R_e}} \tag{12a}$$

$$K = 2L_b / R_o T_s \tag{12b}$$

The CCM-DCM boundary can be determined by equating the RHS of (11) and that of (12a). In a given switching interval, the operation is in CCM if (13a) is satisfied and in DCM if (13b) is satisfied.

$$K \geq (1 - m_g)\frac{R_e}{R_o} \tag{13a}$$

$$K < (1 - m_g)\frac{R_e}{R_o} \tag{13b}$$

The above inequalities may be rewritten using input output power balance as shown in (14) and (15).

$$\frac{R_e}{R_o} = \frac{V_{gm}^2}{2V_o^2} = \frac{M_g^2}{2} \tag{14}$$

$$K \geq \frac{M_g^2}{2}(1 - m_g) \tag{15a}$$

$$K < \frac{M_g^2}{2}(1 - m_g) \tag{15b}$$

For high values of the conduction parameter K as shown in (16), the converter operates in CCM throughout the mains cycle. For low values of the conduction parameter as shown in (17), the converter operates in DCM throughout the cycle.

$$K \geq M_g^2 / 2 \tag{16}$$

$$K < (1 - M_g)M_g^2 / 2 \tag{17}$$

In the intermediate range of K, not covered by (16) and (17), the operation is in CCM in certain switching cycles and in DCM in the other switching intervals over a each half cycle as per (13).

Since the controller has been designed for DCM operation, whenever the operation of the converter enters into the continuous conduction mode, the quality of the mains current deteriorates. This may be compared with [6], where the design is for CCM operation and the input current gets distorted in the discontinuous conduction mode.

V. LOW FREQUENCY MODELS

An averaged large signal model of the converter with the proposed control is shown in Fig. 8 (top) [9]. High frequency switching harmonics have been neglected, retaining the dc and the second harmonic components. The

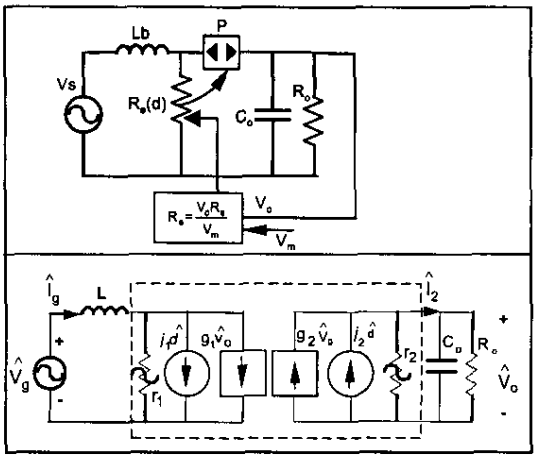

Fig. 8 Large signal model (top),
Small signal ac model (bottom) [9]

power absorbed in the emulated resistor R_e is transferred to the dependent power source P and finally to the load without any internal loss. The inductor and the capacitor in this model behave like a short circuit and an open circuit, respectively. This model may be used to evaluate the low frequency ripple in the output voltage and to select suitable value of capacitor C_o. The dc characteristic of the converter is given in (18). This is obtained by input-output power balance over a fundamental cycle.

$$V_o^3 = V_m \frac{R_o}{R_s} V^2_{g,rms} \tag{18}$$

The large signal ac equivalent model is nonlinear. In order to design the voltage controller a low frequency ac model is essential. Assuming high switching frequency, in each switching interval the converter may be realized by a dc-dc boost converter. The corresponding small signal ac model is shown in Fig. 8 (bottom). This is derived by perturbing and linearizing the network shown in Fig. 8 (top) around an operating point [9]. The parameters of the model are given in [9].

The control-to-output transfer function of the converter is required to design the voltage controller. This is given in (19) [9]. All the parameters in (19) are constant except m_g, which is a function of ωt as shown in (9).

$$\left[\frac{\hat{v}_o(s)}{\hat{d}(s)}\right]_{\hat{V}_g=0} = \frac{G}{1+\frac{s}{\omega_p}} \tag{19}$$

$$G = \frac{V_{gm}\sqrt{(1-m_g)\frac{R_o T_s}{L_b}}}{(2-m_g)}; \quad \omega_p = \frac{2-m_g}{(1-m_g)R_o C_o}$$

Considering a 600W rectifier and parameters as given in Table I, the bode plot of (19) for different values of ωt is shown in Fig. 9. It can be concluded that the above transfer function has little dependence on ωt.

TABLE I
SYSTEM PARAMETERS

C_o	R_o	V_o	V_{gm}	$1/T_s$
1100μF	77Ω	215V	156V	5000Hz

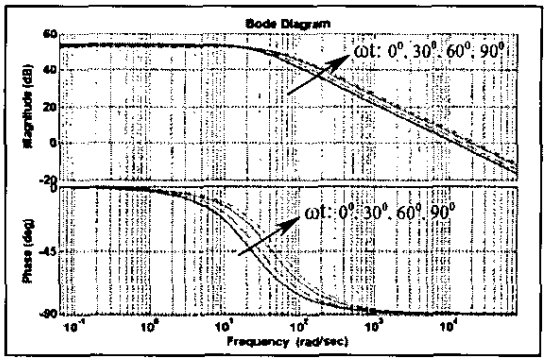

Fig. 9 Bode plot of DCM boost rectifier.

The proposed controller does not have any error amplifier in the current loop. However the mathematical small signal model of an equivalent current loop is given in (20). This is obtained by perturbation and linearization of (6) around the steady state operating point. It relates the converter duty ratio D with V_m, V_o and i_g and may be used along with low frequency ac model (19) to design the parameters of the voltage controller.

$$\hat{d} = \left(\frac{L_b}{R_s T_s D V_o}\right)\hat{V}_m - \left(\frac{D}{2V_o}\right)\hat{V}_o - \left(\frac{L_b}{T_s D V_o}\right)\hat{I}_g \tag{20}$$

VI. Experimental Verification

For validating the control concept, a 600W prototype is built. The experimental set up is shown in Fig. 10. The device used is IRF840 (MOSFET). The passive components are L_f: 2.5mH, C_f: 4uF (input LC filter), boost inductor L_b: 375μH, C_o: 1100μF. A 200Ω, 10A rheostat is used for loading. A current sensor, LA-55P, is used to sense the source current. The output of the current sensor is passed through an active rectifier before the controller uses it. The switching frequency is 5kHz. The gating pulse generated by the circuit is shown in Fig. 11.

The converter is simulated in MATLAB/SIMULINK and experimentally tested with the following specifications,

(a) Output voltage (V_o): 215V, Input voltage (V_s): 75V (rms) at 50Hz, output power (P_o): 300W

(b) V_o: 215V, V_s: 110V (Rms), P_o: 600W.

The simulation results are given in Figs. 12(a)-12(d). The corresponding experimental results are given in Fig. 12(e)-12(h). The current transducer gain is set at 100mV/A. The FFT of the input currents in Figs. 12(f) and 12(h) are presented in Figs. 13(a) and 13(b), respectively.

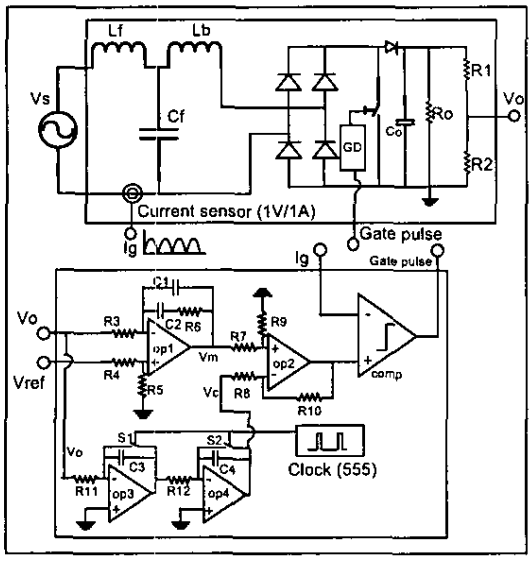

Fig. 10 Experimental setup

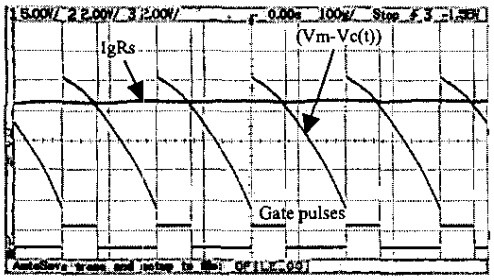

Fig. 11 Experimental Gate pulse generation

VII. Conclusion

An analog controller suitable for a single-phase, single-switch DCM boost rectifier is proposed. The switch duty ratio D is determined by comparing the source current with a suitably generated periodic nonlinear carrier. A simple scheme is proposed to generate the required carrier. The proposed controller works under DCM. Averaged large and small signal ac models are presented to design the passive components and the voltage controller. A number of methods for average input current sensing are discussed. The proposed controller does not need input voltage sensing. It does not have any error amplifier in the inner current loop. The required gating pulses may be generated without using any multiplication, division or square root operation. The proposed controller offers comparable performance over the existing controllers. The control concept is validated through simulation and experiments. The experimental results agree well with the simulation results.

REFERENCES

[1] *Liu, K.H. and Lin, Y.L* , "Current waveform distortion in power factor correction circuits employing discontinuous-mode boost converters," in Proc. PESC '89, Vol.2, pp. 825 – 829

[2] D. Weng and S. Yuvarajan, "Constant-Switching-Frequency AC-DC Converter Using Second Harmonic Injected PWM," IEEE Trans. On Power Electronics, Vol. 11, No. 1, pp. 115-121, January, 1996.

[3] Yu-Kang Lo, Sheng-Yuan Ou and T. Song, "Varying Duty Cycle Control For Discontinuous Conduction Mode Boost Rectifiers," in Proc. IEEE, PEDS, Vol. 1, , pp. 149-151, Oct 2001.

[4] M. Ferdowsi, and A. Emadi, "Estimative Current Mode Control Technique for DC–DC Converters Operating in Discontinuous Conduction Mode," IEEE Power Electronics Letters, Vol. 2, No. 1, pp. 20-23, March 2004.

[5] Chen, D.-S. and Lai, J.-S., " A study of power correction boost converter operating at CCM-DCM mode," in Proc. IEEE, Southeastcon '93, April 1993.

[6] Maksimovic. D, Jang. Y, R. Erickson, " Nonlinear-Carrier Control for High-Power-Factor Boost Rectifiers," IEEE Trans. on power Electronics, Vol. 11, No. 4, July 1996.

[7] Regan Zane, Maksimovic. D, "Modeling of High Power-factor Rectifiers Based on Switching Converters With Nonlinear-Carrier control, PESC '96, IEEE, Vol.2, pp-1105 – 1111, June 1996.

[8] J. Lazar and S. Cuk, "Feedback loop analysis for AC/DC rectifiers operating in discontinuous conduction mode," Proc. APEC '96. Vol. 2, March 1996, pp. 797 – 806.

[9] Robert W. Erickson, "Fundamentals of Power Electronics", first edition, Chapman and Hall, New York, May 1997.

[10] S. Chattopadhyay, V. Ramanarayanan and V. Jayashankar, " Predictive switching modulator for current mode control of high power factor boost rectifier," IEEE Trans. On Power Electron. Vol. 18. No. 1, pp. 114-123, January 2003.

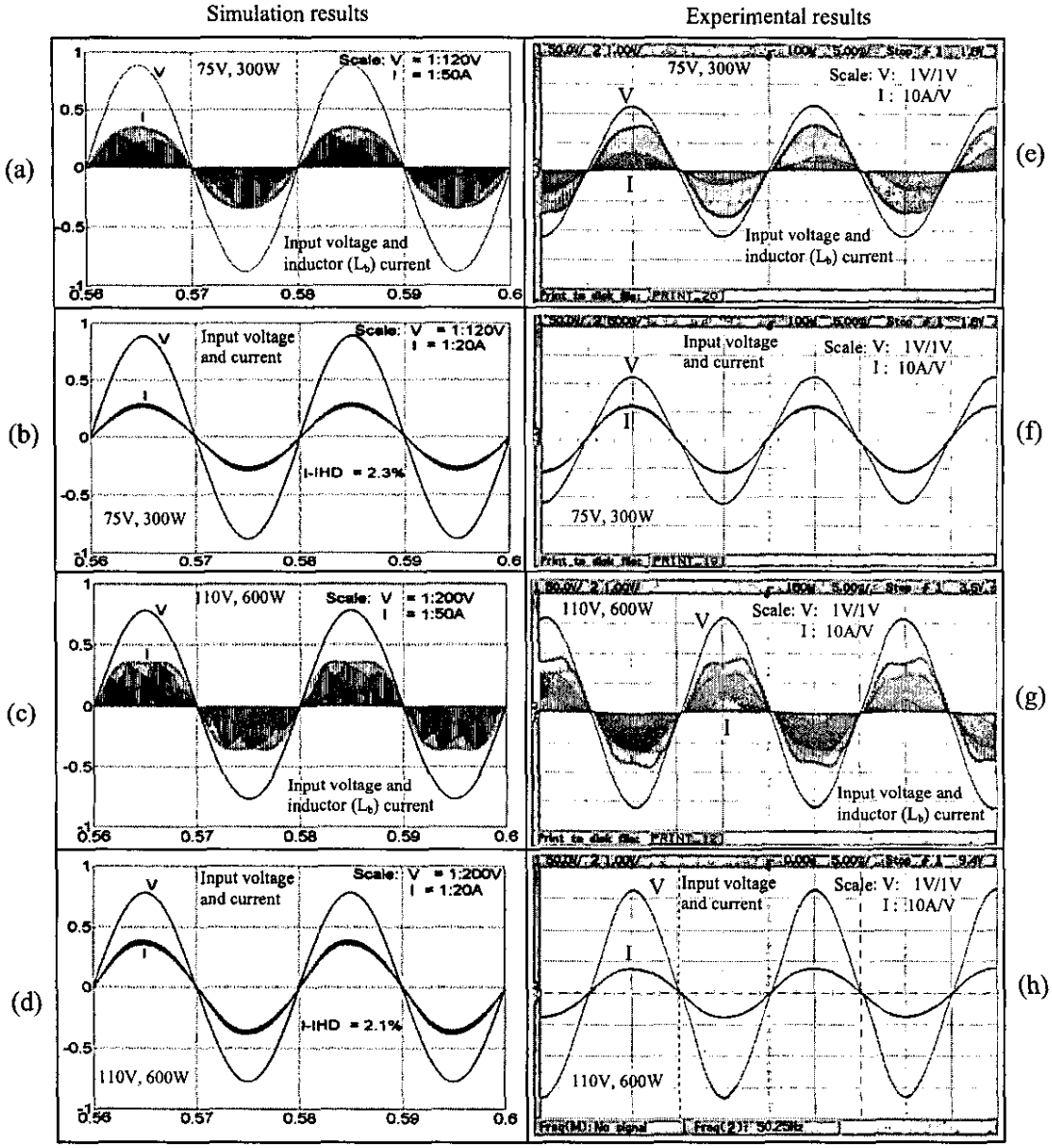

Fig. 12. Simulation results (a-d), and experimental results (e-h).

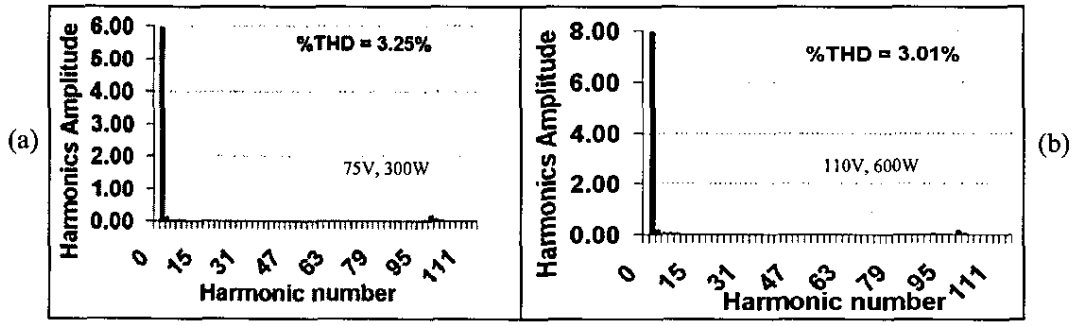

Fig. 13. FFT of input currents.