A Hybrid Multilevel Inverter Topology for an Open-End Winding Induction-Motor Drive Using Two-Level Inverters in Series With a Capacitor-Fed H-Bridge Cell

K. Sivakumar, *Student Member, IEEE*, Anandarup Das, *Student Member, IEEE*, Rijil Ramchand, *Student Member, IEEE*, Chintan Patel, *Student Member, IEEE*, and K. Gopakumar, *Senior Member, IEEE*

***Abstract*—In this paper, a new five-level inverter topology for open-end winding induction-motor (IM) drive is proposed. The open-end winding IM is fed from one end with a two-level inverter in series with a capacitor-fed H-bridge cell, while the other end is connected to a conventional two-level inverter. The combined inverter system produces voltage space-vector locations identical to that of a conventional five-level inverter. A total of 2744 space-vector combinations are distributed over 61 space-vector locations in the proposed scheme. With such a high number of switching state redundancies, it is possible to balance the H-bridge capacitor voltages under all operating conditions including overmodulation region. In addition to that, the proposed topology eliminates 18 clamping diodes having different voltage ratings compared with the neutral point clamped inverter. On the other hand, it requires only one capacitor bank per phase, whereas the flying-capacitor scheme for a five-level topology requires more than one capacitor bank per phase. The proposed inverter topology can be operated as a three-level inverter for full modulation range, in case of any switch failure in the capacitor-fed H-bridge cell. This will increase the reliability of the system. The proposed scheme is experimentally verified on a four-pole 5-hp IM drive.**

***Index Terms*—H-bridge, multilevel inverter, open-end winding induction motor (IM) drive.**

I. Introduction

MULTILEVEL voltage-source inverters have been receiving more and more attention in the past few years for high- and medium-power induction-motor (IM) drive applications. Many multilevel inverter configurations and pulsewidth modulation (PWM) techniques are presented to improve the output voltage harmonic spectrum [1], [3]–[5]. Some of the popular multilevel configurations are the neutral point clamped (NPC), series-connected H-bridge, flying capacitor, etc. Although they can be configured for more than two levels, as the number of levels increase, the power circuit and control complexity due to a large number of devices, increases. An optimum topology for multilevel inverters for more than three levels has not been achieved until now, and research is going on to improve the drive efficiency at reduced circuit complexity and control. In NPC multilevel inverters [1]–[7], the load current drawn from the neutral point will cause an unequal voltage sharing between the series-connected capacitors. This will introduce unwanted harmonics in the inverter output voltage and also results in an unequal voltage stress on the switching devices. To avoid this problem, special voltage-balancing techniques must be implemented [2], [5]–[7], or isolated voltage sources have to supply each series-connected capacitors. Although a scheme is proposed in [8] that allows the NPC three-level inverter to operate with unbalanced capacitor voltages, it increases the control-circuit complexity due to the 3-D space-vector arrangement. In cascaded H-bridge (CHB) multilevel inverter structure [9]–[11], the H-bridge cells are supplied from individual dc source and are series connected to generate multilevel voltage profile. As the number of levels increases, the CHB requires a huge number of isolated voltage sources. In a flying-capacitor topology [12], more number of levels in the phase voltage is generated by adding or subtracting the capacitor voltages. It requires additional control and increased switching for maintaining the capacitor voltages constant. The power circuit and control complexity increases when the number of levels increases in the output voltage. The generalized multilevel inverter topology is presented in [13]. This topology is a combination of NPC and flying-capacitor inverter topologies. However, it requires additional capacitor banks and many active switches to generate a multilevel output voltage. A hybrid asymmetric multilevel inverter topology is proposed [14], by connecting a flying capacitor in series with the NPC inverter. However, this scheme is not valid for the entire operating range of the drive (with respect to the power factor and modulation index). A dc-voltage-ratio control strategy for single-phase two-cell CHB converter with a single dc source is presented in [15]. However, this scheme is based on the elimination of switching states which tend to make the floating capacitor voltage unbalanced. Therefore, this scheme cannot be operated for the full modulation range using any arbitrary dc-voltage ratios (i.e., the ratio between the dc-source voltage and floating-capacitor voltage). Moreover, if this scheme is extended to a three-phase system, then it requires three isolated voltage sources.

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The authors are with the Center for Electronics Design and Technology, Indian Institute of Science, Bangalore 560 012, India (e-mail: kgopa@cedt.iisc.ernet.in).

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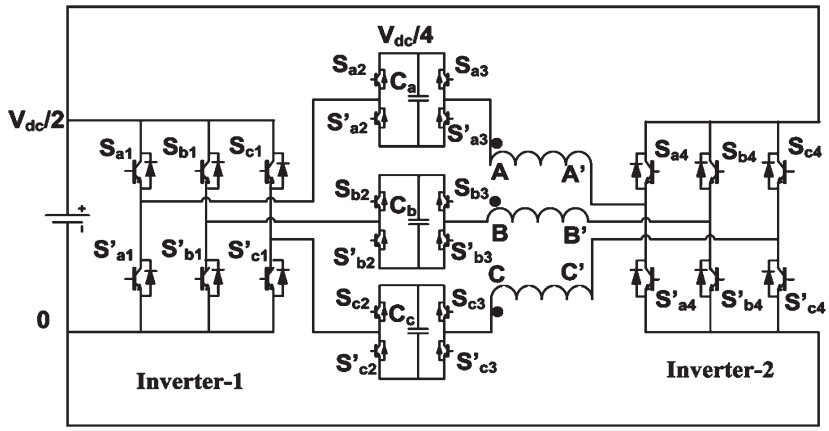

Fig. 1. Proposed five-level inverter power circuit.

An interesting addition in this paper is the open-end winding IM scheme [16]–[19]. Here, the number of levels in the phase voltage can be increased by lower magnitude dc sources. In the open-end winding scheme, the IM windings are fed from both sides with two two-level inverter (with half the dc-link voltage compared with conventional NPC inverter) to get a three-level inverter topology [16]. Further, the number of levels on the phase winding can be extended by cascading conventional two- and three-level inverters [20]–[23]. However, this cannot eliminate the series connection of the capacitors or voltage sources. Thereby, it will introduce capacitor voltage unbalance problems.

As mentioned earlier, it is possible to generate a three-level voltage profile on the phase winding of an open-end IM by feeding with two two-level inverters from both sides. In this paper, this is further improved by connecting a capacitor fed H-bridge cell in series with the motor phase winding. By balancing the H-bridge capacitor voltage, it is possible to generate five voltage levels on a motor phase winding. Thereby, the dc-bus voltage requirement is reduced to one-half compared with a conventional NPC inverter. The inverter scheme proposed in this paper produces 61 voltage space-vector locations as in conventional (NPC or flying capacitor) five-level inverter topology. A total of 2744 voltage space-vector combinations are possible in this scheme, whereas the NPC five-level inverter can produce only 125. In this work, with the advantage of additional space-vector combinations, the H-bridge capacitor voltages are balanced for the full modulation range. Thereby, the voltage-balancing problems and complexity in the power circuit are also minimized. In the case of any switch failure in the capacitor fed H-bridge cell circuit, the proposed topology can still operate, for the full modulation range, as a three level inverter (like open-end winding structure [17]). Thereby, the reliability of the system increases. This proposed topology is experimentally verified on a 5-hp IM drive.

II. Proposed Five-Level Inverter Scheme

The proposed five-level inverter power circuit is shown in Fig. 1. In this circuit, only one voltage source is used with a magnitude of $V_{\rm dc}/2$ where $V_{\rm dc}$ is the dc-link voltage requirement for the conventional NPC inverter. This topology is an extension of the open-end winding multilevel inverter structure. An open end IM drive will have a three-level voltage space-vector structure across the phase winding when fed from two-level inverters from both sides [17]. In this work, the number of levels on the phase voltage can be further increased by introducing an additional capacitor-fed H-bridge cell in series with motor phase windings. For this study, it is assumed that the H-bridge capacitors (C_a, C_b, and C_c) are charged to a voltage $V_{\rm dc}/4$. If the two-level inverters are now clamped to zero voltage, then the H-bridge cell can produce voltage levels of $V_{\rm dc}/4$, 0, and $-V_{\rm dc}/4$ on the motor phase winding. On the other hand, by clamping the H-bridge cell to zero voltage, the two two-level inverters can generate voltage levels of $V_{\rm dc}/2$, 0, and $-V_{\rm dc}/2$ on the phase winding. When both of them are operated together, it is possible to have five voltage levels on the motor phase windings with a magnitude of $V_{\rm dc}/2$, $V_{\rm dc}/4$, 0, $-V_{\rm dc}/4$, and $-V_{\rm dc}/2$. For easy understanding, these voltage magnitudes are defined as 2, 1, 0, -1, -2 levels, respectively. The H-bridge capacitor voltages can always be maintained at $V_{\rm dc}/4$, using the switching state redundancy, as explained in the next paragraph. The switches $S_{\rm a1}$ to $S'_{\rm c1}$ and $S_{\rm a4}$ to $S'_{\rm c4}$ in Fig. 1 are part of the two-level inverters which are fed from the voltage source magnitude of $V_{\rm dc}/2$. Therefore, the maximum voltage-blocking capacity of these switches is $V_{\rm dc}/2$. The remaining switches in the proposed circuit (i.e., $S_{\rm a2}$ to $S'_{\rm c3}$) are connected in parallel to the capacitor; therefore, the maximum voltage-blocking capacity of these switches is $V_{\rm dc}/4$ (since the H-bridge capacitor voltage is balanced at $V_{\rm dc}/4$).

The possible switching combinations for the five voltage levels on the A-phase winding are shown in Table I. In Table I, due to the complementary nature of the two-level inverter switches, switch $S_{\rm a1}$ is "ON" automatically implies that switch $S'_{\rm a1}$ is "OFF." The current from points A to A' (Fig. 1) is assumed to be the positive direction of the current and is shown as $i_a > 0$ in Table I. The H-bridge capacitors can be charged or discharged independently of the phase-current direction for the voltage levels $V_{\rm dc}/4$ and $-V_{\rm dc}/4$. For example, if $i_a > 0$, C_a can be charged for the voltage level $V_{\rm dc}/4$ by turning on the switches $S_{\rm a1}$ and $S_{\rm a2}$ and by turning off the switches $S_{\rm a3}$ and $S_{\rm a4}$. It can be discharged by turning off the switches $S_{\rm a1}$, $S_{\rm a2}$, and $S_{\rm a4}$ and by turning on the switch $S_{\rm a3}$. The other voltage levels (i.e., $V_{\rm dc}/2$, 0, and $-V_{\rm dc}/2$) on the phase winding is achieved

TABLE I
ALL POSSIBLE SWITCHING COMBINATIONS FOR THE FIVE VOLTAGE LEVELS FOR PHASE A

Phase voltage (level)	$V_{dc}/2$ (2)		$V_{dc}/4$ (1)			0 (0)				$-V_{dc}/4$ (-1)			$-V_{dc}/2$ (-2)	
Status of S_{a1}	ON	ON	ON	ON	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	OFF
Status of S_{a2}	ON	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	ON	ON	OFF
Status of S_{a3}	ON	OFF	OFF	ON	ON	ON	OFF	ON	OFF	ON	OFF	OFF	ON	OFF
Status of S_{a4}	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	ON	ON
Capacitor C_a status	No change		$i_a>0$: charging $i_a<0$: discharging	$i_a<0$: discharging $i_a<0$: charging		No change				$i_a<0$: charging $i_a<0$: discharging	$i_a<0$: discharging $i_a<0$: charging		No change	

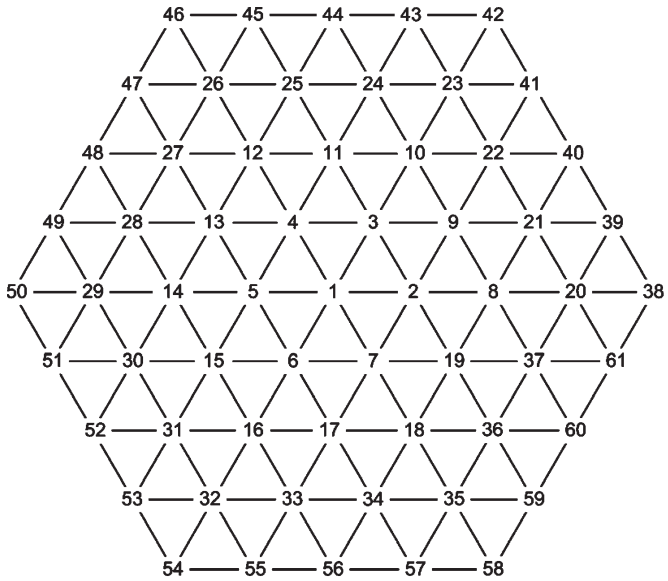

Fig. 2. Voltage space-vector locations for a five-level inverter.

by bypassing the H-bridge capacitors; therefore it will not affect the capacitor voltages. The switching states for the bypass (H-bridge capacitor) operation are listed in Table I. The proposed power circuit can generate two more voltage levels with a voltage magnitude of $3 * V_{\rm dc}/4$ and $-3 * V_{\rm dc}/4$. These additional voltage levels can be generated by placing the capacitor in series with the dc-link voltage. However, at this voltage level, the power circuit does not have any complementary state to balance the H-bridge capacitor voltage. Therefore, the capacitor voltage balancing is not possible with redundant switching states when all the seven levels are used for PWM control. Therefore, only five voltage levels are used for PWM control in this study. If the capacitor in the H-bridge cell is replaced with a dc-voltage source, then all seven levels can be used for PWM control. However, the power circuit needs additional three dc-link voltage sources which will increase the power circuit complexity. From Table I, it can be noted that there are 14 possible switching combinations for one phase to realize the five voltage levels. Therefore, a total of 2744 $(14 \times 14 \times 14)$ switching combinations are possible for this work. The space-vector structure for the five-level inverter is shown in Fig. 2. The possible switching combinations for the each space-vector point (which is a vector addition of all three-phase voltages), shown in Fig. 2, are listed in Table II, with the help of the voltage levels. Note that each voltage level can be realized in a number of ways, as shown in Table I.

TABLE II
SPACE-VECTOR LOCATIONS AND THE CORRESPONDING SWITCHING STATES

Points (P)	SWITCHING STATE	P	SWITCHING STATE	P	SWITCHING STATE
1	(2,2,2), (1,1,1), (0,0,0), (-1,-1,-1), (-2,-2,-2)	21	(2,0,-1), (1,-1,-2)	41	(2,1,-2)
2	(1,0,0), (2,1,1), (0,-1,-1), (-1,-2,-2)	22	(1,0,-2), (2,1,-1)	42	(2,2,-2)
3	(1,1,0), (2,2,1), (0,0,-1), (-1,-1,-2)	23	(2,2,-1), (1,1,-2)	43	(1,2,-2)
4	(0,1,0), (-1,0,-1), (-2,-1,-2), (1,2,1)	24	(1,2,-1), (0,1,-2)	44	(0,2,-2)
5	(0,1,1), (-1,0,0), (-2,-1,-1), (1,2,2)	25	(0,2,-1), (-1,1,-2)	45	(-1,2,-2)
6	(0,0,1), (-1,-1,0), (-2,-2,-1), (1,1,2)	26	(-1,2,-1), (-2,1,-2)	46	(-2,2,-2)
7	(1,0,1), (2,1,2), (0,-1,0), (-1,-2,-1)	27	(-1,2,0), (-2,1,-1)	47	(-2,2,-1)
8	(2,0,0), (1,-1,-1), (0,-2,-2)	28	(-2,1,0), (-1,2,1)	48	(-2,2,0)
9	(2,1,0), (1,0,-1), (0,-1,-2)	29	(-1,2,2), (-2,1,1)	49	(-2,2,1)
10	(2,2,0), (1,1,-1), (0,0,-2)	30	(-1,1,2), (-2,0,1)	50	(-2,2,2)
11	(1,2,0), (0,1,-1), (-1,0,-2)	31	(-2,-1,1), (-1,0,2)	51	(-2,1,2)
12	(0,2,0), (-1,1,-1), (-2,0,-2)	32	(-1,-1,2), (-2,-2,1)	52	(-2,0,2)
13	(0,2,1), (-1,1,0), (-2,0,-1)	33	(0,-1,2), (-1,-2,1)	53	(-2,-1,2)
14	(-1,1,1), (-2,0,0), (0,2,2)	34	(0,-2,1), (1,-1,2)	54	(-2,-2,2)
15	(0,1,2), (-1,0,1), (-2,-1,0)	35	(1,-2,1), (2,-1,2)	55	(-1,-2,2)
16	(0,0,2), (-1,-1,1), (-2,-2,0)	36	(1,-2,0), (2,-1,1)	56	(0,-2,2)
17	(1,0,2), (0,-1,1), (-1,-2,0)	37	(1,-2,-1), (2,-1,0)	57	(1,-2,2)
18	(2,0,2), (1,-1,1), (0,-2,0)	38	(2,-2,-2)	58	(2,-2,2)
19	(2,0,1), (1,-1,0), (0,-2,-1)	39	(2,-1,-2)	59	(2,-2,1)
20	(2,-1,-1), (1,-2,-2)	40	(2,0,-2)	60	(2,-2,0)
				61	(2,-2,-1)

It is known that inverters controlled by conventional 2-D space-vector PWM (SVPWM) will produce a common-mode (triplen) voltage along with the fundamental voltage on the motor phase windings [16], [24] (i.e., the sum of all three phase voltages is not equal to zero). The triplen harmonic content in the phase voltage would cause a high triplen harmonic current

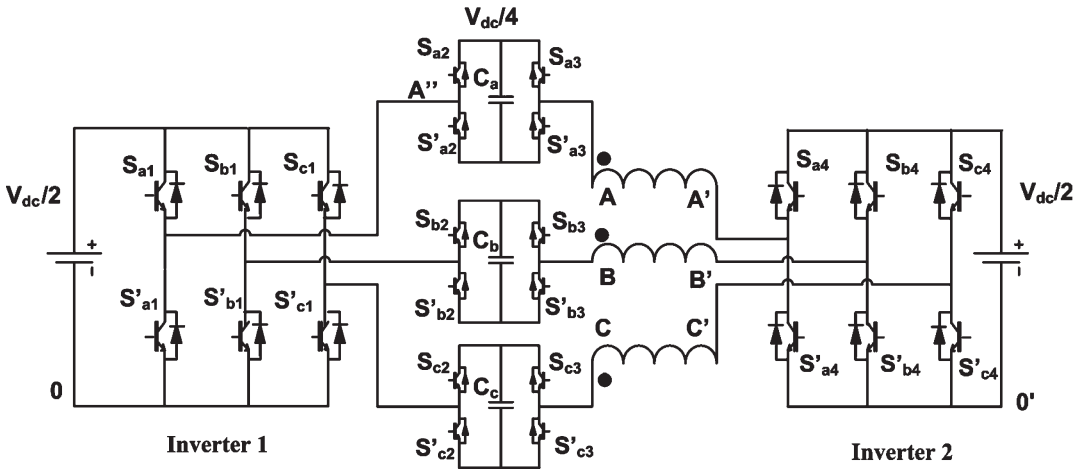

Fig. 3. Modified five-level inverter topology.

to flow through the motor phases and power semiconductor devices in Fig. 1. To suppress the triplen harmonic current, either harmonic filter or isolated power supplies should be used. In this proposed topology, two isolated voltage sources are used to deny the path for triplen current (circulating currents). The modified inverter topology is shown in Fig. 3.

The proposed topology can be operated as a dual-inverter-fed open-end winding IM drive (i.e., three-level operation) [17] for full modulation range, by properly clamping the H-bridge cells. In case of any switch failure in inverter 1 or inverter 2, the proposed scheme can be operated as a three-level inverter by properly clamping the faulty inverter. This will increase the reliability of the system in fault conditions.

III. Switching Strategy and H-Bridge Capacitor Design

In this work, the inverter-gating pulses are generated similar to an SVPWM technique, using the sampled reference phase voltage magnitudes [25]. The reference voltage space-vector magnitude (V_r^*) ($V_r^* = v_a^* + v_b^* e^{j120^\circ} + v_c^* e^{j240^\circ}$, where v_a^*, v_b^*, and v_c^* are the reference voltages magnitudes of three phases) can be calculated from the motor speed requirement using a constant V/f control [1], [16]. The individual phase voltage references (v_a^*, v_b^*, and v_c^*) can be derived from a voltage space vector. To have maximum utilization of the dc-bus voltage, in linear modulation, an offset voltage is added to the three reference voltages [25], [26] given as

$$V_{\text{offset}} = -\left[\max\left(v_a^*, v_b^*, \text{ and } v_c^*\right) + \min\left(v_a^*, v_b^*, \text{ and } v_c^*\right)\right]/2 \tag{1}$$

$$v_{an}^* = v_a^* + V_{\text{offset}}. \tag{2}$$

The new A-phase reference voltage V_{an}^* is shown in Fig. 4 for modulation index (the modulation index M is defined as the ratio of the magnitude of the equivalent voltage space vector (V_r), generated by the three phase voltages, to the dc-link voltage) that is equal to 0.8. The voltage magnitude required by the load is realized by comparing the reference voltage waveform with the carrier wave. The switching state can be selected from Table I, by observing the current direction and H-bridge capacitor voltage.

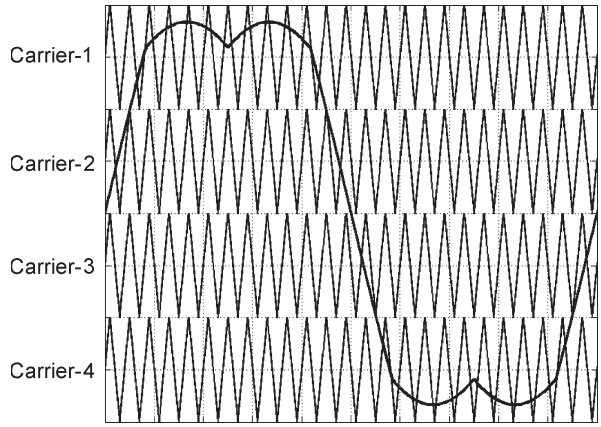

Fig. 4. Reference voltage and four-level shifted triangle carriers.

The performance of the proposed topology is dependent on the H-bridge capacitor ripple voltage. The capacitors can be designed properly to restrict the ripple voltage within acceptable limits. The capacitance required by the H-bridge capacitor can be calculated by using the formula given in

$$C = I_p * \frac{\Delta T}{\Delta V} = I_p * \frac{T_s}{\Delta V} \tag{3}$$

where

C H-bridge capacitor (C_a, C_b, or C_c);
I_p peak phase current;
T_s switching time period;
ΔV peak-to-peak voltage ripple allowed in the H-bridge capacitor.

According to (3), if the peak-to-peak H-bridge capacitor ripple voltage is allowed to vary up to 10 V, then for a load current magnitude of 10 A at a switching frequency of 1 kHz, the capacitor value is designed as 1000 μF.

The proposed topology is compared with the conventional topologies (with respect to the switching devices, capacitor banks, and isolated voltage sources) and is presented in Table III. It can be observed that the number of active switches is same for all the topologies, but the proposed topology

TABLE III
COMPARISON BETWEEN THE PROPOSED TOPOLOGY AND CONVENTIONAL FIVE-LEVEL INVERTER TOPOLOGIES

		NPC Topology	Flying capacitor topology	H-bridge topology	Proposed topology
Switches	voltage rating of $V_{dc}/4$	24	24	24	12
	$V_{dc}/2$	0	0	0	12
Clamping diodes	Voltage rating of $3*V_{dc}/4$	6	0	0	0
	$V_{dc}/2$	6	0	0	0
	$V_{dc}/4$	6	0	0	0
Isolated voltage sources (voltage magnitude)		1* (V_{dc})	1* (V_{dc})	6 ($V_{dc}/4$)	2 ($V_{dc}/2$)
Number of capacitor banks (with a voltage rating of $V_{dc}/4$)		4	18	0	3

* - Capacitor voltage balancing techniques are required

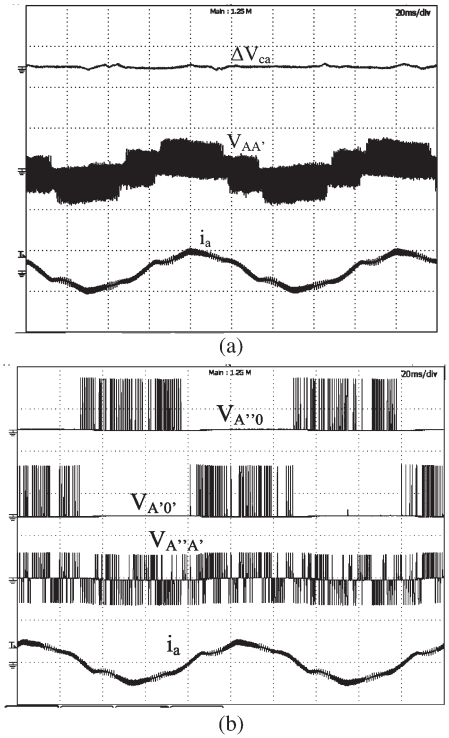

Fig. 5. (a) Top trace is H-bridge capacitor ripple voltage [Y-axis: 2 V/div], second trace is motor phase voltage [Y-axis: 50 V/div], and third trace is phase current [Y-axis: 1 A/div]. (b) Top trace is inverter 1 pole voltage, second trace is inverter 2 pole voltage, third trace is H-bridge cell output voltage, and fourth trace is phase current at $M = 0.2$ [Y-axis: 100 V/div and 1 A/div, and X-axis: 20 ms/div].

does not require additional clamping diodes as in the case of NPC inverter. However, the proposed topology requires 12 switches with a maximum voltage rating of $V_{\rm dc}/4$, and the other 12 switches have a maximum voltage rating of $V_{\rm dc}/2$. The proposed topology requires two isolated voltage sources $(V_{\rm dc}/2)$ only, whereas the H-bridge topology requires six

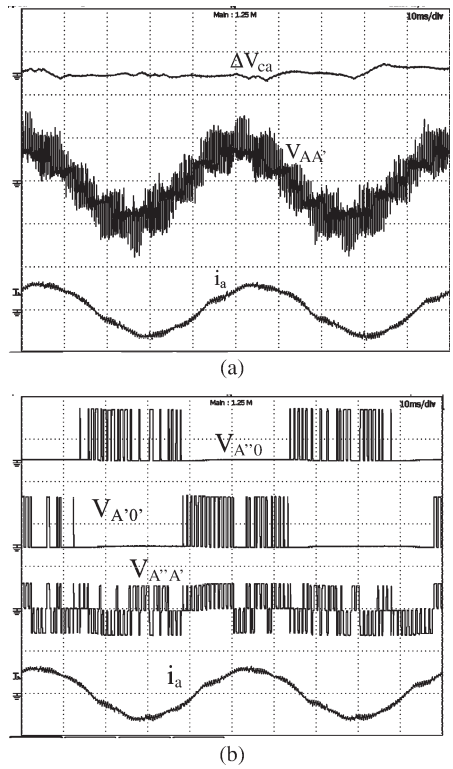

Fig. 6. (a) Top trace is H-bridge capacitor ripple voltage [Y-axis: 2 V/div], second trace is motor phase voltage [Y-axis: 50 V/div], and third trace is phase current [Y-axis: 1 A/div]. (b) Top trace is inverter 1 pole voltage, second trace is inverter 2 pole voltage, third trace is H-bridge cell output voltage, and fourth trace is phase current at $M = 0.4$ [Y-axis: 100 V/div and 1 A/div, and X-axis: 10 ms/div].

isolated voltage sources with a voltage magnitude of $V_{\rm dc}/4$. For five-level operation, the number of capacitor banks (with voltage rating of $V_{\rm dc}/4$) required in NPC and flying-capacitor topologies are, respectively, 4 and 18. On the other hand, the proposed topology requires only three capacitor banks (with voltage rating of $V_{\rm dc}/4$).

IV. EXPERIMENTAL RESULTS

The proposed five-level inverter topology is experimentally verified on a 5-hp open-end winding IM. The motor is run at no-load condition to show the effect of changing PWM patterns on the motor current. Open loop V/f control is used to test the drive for the full modulation range. Throughout the speed range, the switching frequency is kept at 1 kHz, and the H-bridge capacitor value is chosen as 1100 μF. The controller is implemented in TMS320F2812 DSP platform with the gating signals generated from SPARTAN XC3S200 field-programmable gate array.

Experimental results for modulation index of 0.2 (i.e., inverter output fundamental voltage frequency is 10 Hz) are shown in Fig. 5. The H-bridge capacitor ripple voltage, phase voltage, and phase current are shown in Fig. 5(a). As seen from the phase voltage waveform, the proposed topology is operating in a two-level mode. Because of no-load operation, the H-bridge capacitor peak-to-peak voltage ripple is less than 1 V, which is about 10% of the full-load voltage ripple allowed

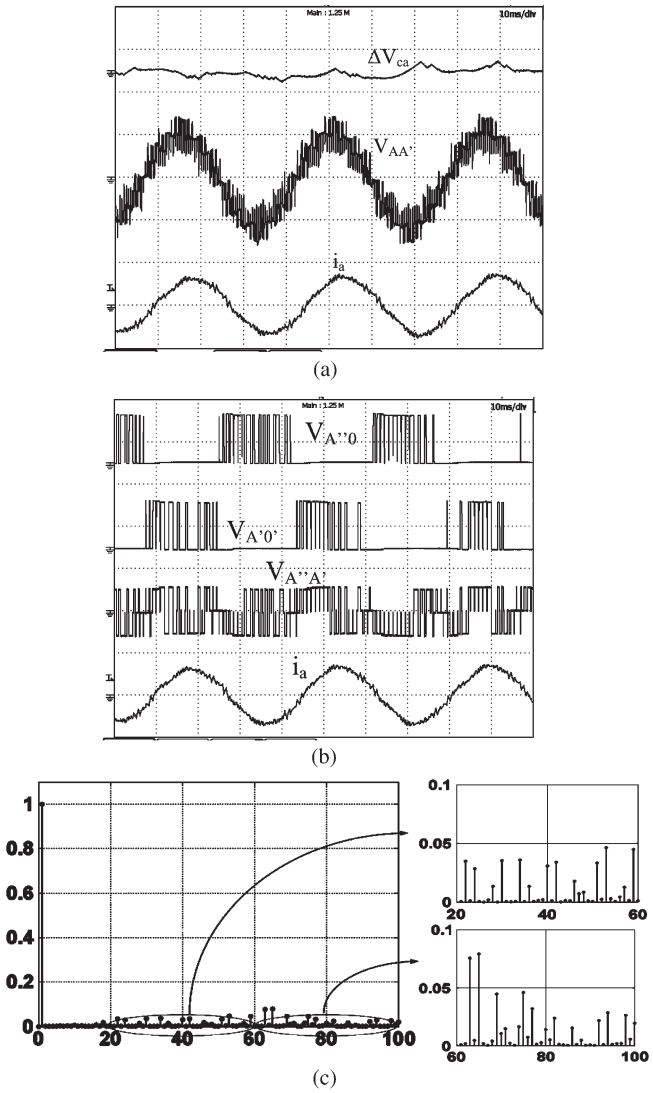

Fig. 7. (a) Top trace is H-bridge capacitor ripple voltage [Y-axis: 2 V/div], second trace is motor phase voltage [Y-axis: 50 V/div], and third trace is phase current [Y-axis: 1 A/div]. (b) Top trace is inverter 1 pole voltage, second trace is inverter 2 pole voltage, third trace is H-bridge cell output voltage, and fourth trace is phase current at $M = 0.6$ [Y-axis: 100 V/div and 1 A/div and X-axis: 10 ms/div]. (c) Normalized harmonics spectrum of phase voltage, X-axis: Harmonic order, Y-axis: normalized harmonic magnitude (linear scale).

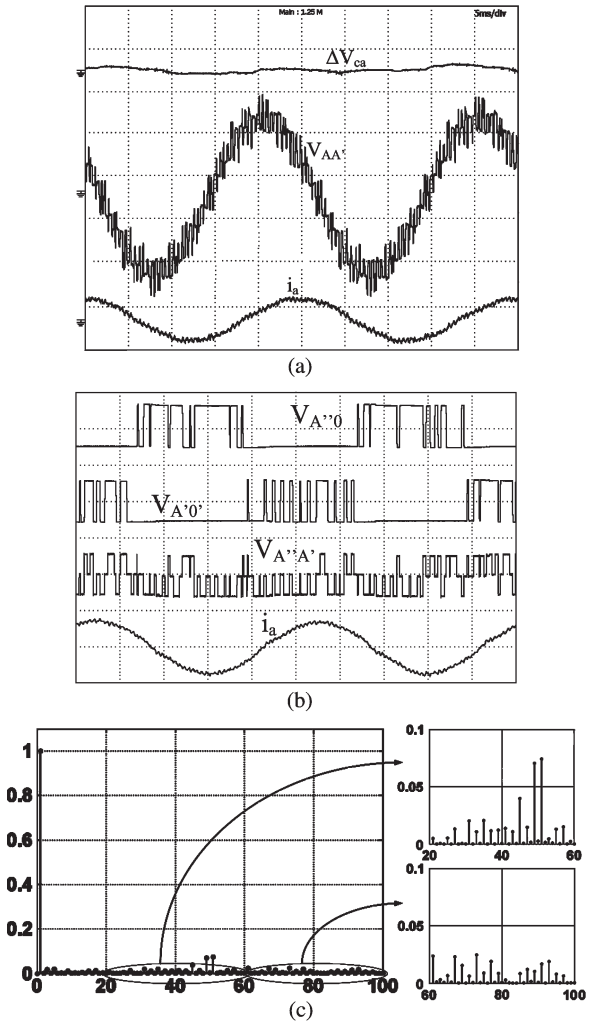

Fig. 8. (a) Top trace is H-bridge capacitor ripple voltage [Y-axis: 2 V/div], second trace is motor phase voltage [Y-axis: 50 V/div], and third trace is phase current [Y-axis: 1 A/div]. (b) Top trace is inverter 1 pole voltage, second trace is inverter 2 pole voltage, third trace is H-bridge cell output voltage, and fourth trace is phase current at $M = 0.8$ [Y-axis: 100 V/div and 1 A/div, and X-axis: 5 ms/div]. (c) Normalized harmonics spectrum of phase voltage, X-axis: Harmonic order, Y-axis: normalized harmonic magnitude (linear scale).

by the capacitors. Fig. 5(b) shows the pole voltages of inverter 1 and inverter 2 and the H-bridge cell output voltage (i.e., difference of the two pole voltage in H-bridge cell) and phase current at no load. From this, it can be observed that high-voltage-fed inverters (i.e., inverter 1 and inverter 2 in Fig. 3) are switching half of the period in fundamental cycle. Therefore, this will reduce the switching losses of the drive.

Another set of experimental results, for modulation index of 0.4, are shown in Fig. 6. The waveforms are in the same order, similar to the previous set of experimental results. From Fig. 6(a) it can be noted that the inverter is operating in a three-level mode, and the H-bridge capacitor voltage is well balanced and the peak to peak ripple is less than 1 V. From Fig. 6(b), it can be seen that at this modulation index also, the high-voltage-fed inverters, inverter 1 and inverter 2 (Fig. 3), are switching for half a period in a fundamental cycle. Similar kind of experimental results are shown for modulation indexes of 0.6 (i.e., inverter output fundamental voltage frequency is 30 Hz) and 0.8 (i.e., inverter output fundamental voltage frequency is 40 Hz) in Figs. 7 and 8, respectively. From the aforementioned experimental results, it can be observed that the inverter is operating in a four-level mode at modulation index of 0.6 and in a five-level mode of operation at modulation index of 0.8. The H-bridge capacitor voltage is well balanced (since the ripple voltage magnitude is less) when the inverter is operating at four-level and five-level modes. Fig. 7(c) shows the normalized harmonic spectrum of the phase voltage $(V_{\mathrm{AA}'})$ for fundamental voltage frequency of 30 Hz (i.e., $M = 0.6$). Therefore, the first center-band harmonics appear at 33 (1000 Hz/30 Hz) times the fundamental frequency. However, as seen from Fig. 7(c), the magnitudes of the harmonics are highly suppressed because of the four-level operation of the inverter. A normalized harmonic spectrum of phase voltage at $M = 0.8$ (i.e., 40 Hz operation) is shown in Fig. 8(c). At this operating condition, the first center-band harmonics is present at 25 (1000 Hz/40 Hz) times the

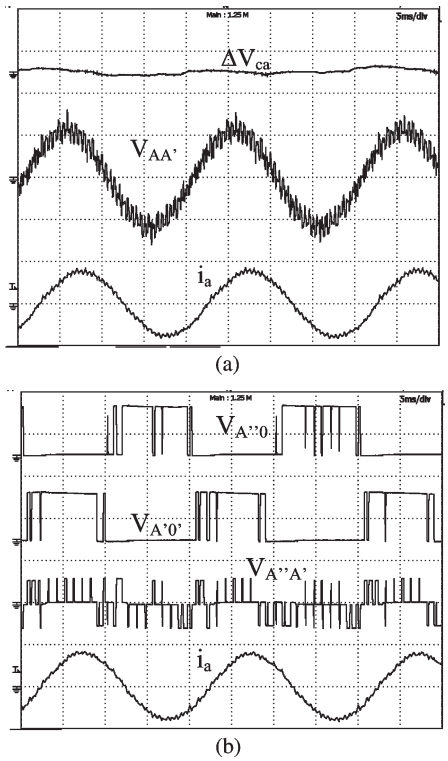

Fig. 9. (a) Top trace is H-bridge capacitor ripple voltage [Y-axis: 2 V/div], second trace is motor phase voltage [Y-axis: 50 V/div], and third trace is phase current [Y-axis: 1 A/div]. (b) Top trace is inverter 1 pole voltage, second trace is inverter 2 pole voltage, third trace is H-bridge cell output voltage, and fourth trace is phase current for overmodulation [Y-axis: 100 V/div and 1 A/div, and X-axis: 5 ms/div].

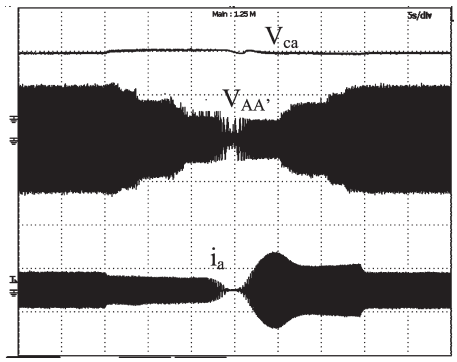

Fig. 10. Top trace is H-bridge capacitor voltage [Y-axis: 50 V/div], second trace is motor phase voltage [Y-axis: 100 V/div], and third trace is phase current during the acceleration from two level mode of operation to a five-level mode of operation. [Y-axis: 2 A/div, X-axis: 5 s/div].

fundamental frequency. However, here also, the harmonics are highly suppressed because of a five-level operation.

Similar set of experimental results are shown in Fig. 9 for overmodulation. From this experimental results, it can be seen that the H-bridge capacitor voltage is well balanced (since the ripple voltage magnitude is less) when the inverter is operating at overmodulation. Inverter 1 and inverter 2 are switching for half the period in a fundamental cycle. It indicates that for the entire modulation range, the high-voltage-fed inverters (inverter 1 and inverter 2 in Fig. 3) are switching half the period in a fundamental cycle, which will reduce the switching losses, and thereby, the efficiency of the drive system increases.

Fig. 10 shows the transient performance of the proposed scheme during speed-reversal operation of the drive. In Fig. 10, the waveforms show the H-bridge capacitor voltage, IM phase voltage, and phase current. From the aforementioned waveforms can be observed the smooth transitions of operating levels of the inverter when speed-reversal command is given in a five-level mode of operation. Even though accelerating and decelerating the motor draw current much more than the steady-state operation, yet the capacitor voltage is balanced for the full modulation range. Thereby, the traces conform that the present scheme is capable of balancing the H-bridge capacitor voltage throughout the modulation range.

V. Conclusion

In this paper, the concept of open-end winding structure has been extended by adding a capacitor-fed H-bridge cell in series with the motor phase winding. This results in a five-level inverter topology. It does not require any clamping diodes as in a conventional five-level NPC inverter. It requires only one capacitor bank for each phase, whereas the five-level flying-capacitor topology requires six additional capacitor banks with a voltage rating of $V_{\rm dc}/4$ for each phase. Therefore, the proposed topology reduces the power circuit complexity compared with NPC or flying-capacitor topologies. In case of any switch failure in the H-bridge cell, the proposed inverter topology can be operated as a three-level inverter for full modulation range (by appropriately clamping the H-bridge cell). Inherent H-bridge capacitor voltage balancing eliminates the need for additional dc-power supplies and hence, increases the reliability of the power circuit and also reduces the power circuit complexity. In case of any failure in inverter 1 and inverter 2 (Fig. 3), this topology can be operated as a three-level inverter in lower modulation index. The proposed five-level inverter topology has been experimentally verified for the full modulation range, on a 5-hp IM drive, for steady-state as well as transient conditions using V/f control.

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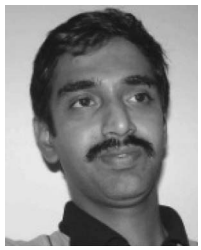
K. Sivakumar (S'08) received the B.Tech. degree in electrical engineering from Sri Venkateswara University, Tirupati, India, in 2004 and the M.Tech. degree in power electronics from the National Institute of Technology, Warangal, India, in 2006. He is currently working toward the Ph.D. degree in the Centre for Electronics Design and Technology, Indian Institute of Science, Bangalore, India.

His fields of interest are multilevel inverters, pulsewidth modulation techniques, and ac drives.

Anandarup Das (S'08) received the B.E. degree in electrical engineering from Bengal Engineering College, Kolkata, India, in 2002 and the M.Tech. degree in power electronics from the Indian Institute of Technology, New Delhi, India, in 2006. He is currently working toward the Ph.D. degree in the Centre for Electronics Design and Technology, Indian institute of Science, Bangalore, India.

His fields of interest are in multilevel inverter-fed drives, power quality, and control.



Rijil Ramchand (S'09) received the B.Tech. degree in electrical engineering from Calicut University, Thenhipalam, India, in 1996 and the M.E. degree from the Indian Institute of Science, Bangalore, India, in 2003, where he is currently working toward the Ph.D. degree in the Centre for Electronics Design and Technology.

He is a Member of the faculty with the Department of Electrical Engineering, National Institute of Technology, Calicut, India. His fields of interest are power converters, pulsewidth modulation techniques, and ac drives.

Chintan Patel (S'08) received the B.E. degree in electrical engineering from South Gujarat University, Surat, India, in 2000 and the M.Tech. degree in electrical engineering from the Institute of Technology–Banaras Hindu University, Varanasi, India, in 2003. He is currently working toward the Ph.D. degree in the Centre for Electronics Design and Technology, Indian Institute of Science, Bangalore, India.

He was a Lecturer with Nirma University, Ahmedabad, India, from 2003 to 2007. His research interests include sensorless control of induction motors and hysteresis current controller.

K. Gopakumar (M'94–SM'96) received the B.E., M.Sc. (Eng.), and Ph.D. degrees from the Indian Institute of Science, Bangalore, India, in 1980, 1984, and 1994, respectively.

He was with the Indian Space Research Organization from 1984 to 1987. He is currently with the Indian Institute of Science as a Professor and the Chairman of Centre for Electronics Design and Technology. His fields of interest are power converters, pulsewidth modulation techniques, and ac drives.

Dr. Gopakumar is a fellow of the Institution of Electrical and Telecommunication Engineers, India, and the Indian National Academy of Engineers. He currently serves as an Associate Editor for IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS.