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(54) Title: YIELD AND SPEED ENHANCEMENT OF SEMICONDUCTOR INTEGRATED CIRCUITS USING POST-FABRICATION TRANSISTOR MISMATCH COMPENSATION CIRCUITRY

(57) Abstract: A novel technique for the enhancement of yield and speed of semiconductor integrated circuits using post fabrication transistor mismatch compensation circuitry is proposed. The system is novel because it recognizes that no matter what, the transistor mismatch is statistical in nature and hence it is prudent to exploit the nature of the distribution to get fast and slow circuits rather than make all circuits slow to meet 6σ design index. The system comprises of sense amplifier, multiplexer, delay elements, and provision for hardwiring fast and slow circuits during packaging. The sense amplifier firing path is split into slow and fast path and the multiplexer can select one of these. The memory circuits are tested after fabrication to assess whether they could be partitioned as slow or fast circuits and accordingly an appropriate path is selected by the multiplexer. This path is then hardwired during packaging by connecting the select input of multiplexer to VDD or GND.

YIELD AND SPEED ENHANCEMENT OF SEMICONDUCTOR INTEGRATED CIRCUITS USING POST-FABRICATION TRANSISTOR MISMATCH COMPENSATION CIRCUITRY

FIELD OF TECHNOLOGY

This invention in general relates to manufacturing of semiconductor. Further this invention is related to manufacturing of VLSI circuits. Further this invention pertains to Semiconductor memory technology such as DRAM, SRAM etc. More particularly this invention encompasses a ***Yield and Speed Enhancement of Semiconductor Integrated Circuits using Post-Fabrication Transistor Mismatch Compensation Circuitry in Semiconductor memory technology.***

DESCRIPTION OF PRIOR ART

In semiconductor integrated circuit (IC) manufacturing, there is a typical trade-off between speed and yield. This is even more so when the IC includes analog blocks. For the semiconductor memories such as SRAM and DRAM, the READ access time determines the speed of the memory. The sense amplifier is the most critical analog block in the READ access path. The response speed of the sense amplifier determines the over all speed of the memory. The typical structure of SRAM memory cell with associated bit line capacitance and sense amplifier is shown in Fig. 1. When the cell is accessed, depending on the data stored in the cell, either BL or BL' starts discharging from the pre charged value of Vdd. Since BL and BL' lines have very large capacitance, the sense amplifier is used to amplify the small differential signals on these lines and get the rail to rail swing. The high gain sense amplifier needs to be fired at a precise time when the correct differential voltage is developed at its inputs. Otherwise incorrect data could be latched at the output of the memory.

There are two important factors that impact the sense amplifier firing delay. The first one is related to the tracking of the word line and bit line delays across the process corners

and the supply voltage fluctuations. The problem becomes worse with the scaling of CMOS technology into the deep sub-micron regime and the associated lower supply voltages. This problem is typically solved by generating the sense control signal by techniques such as replica memory cell.

The second problem relates to the transistor mismatch in the sense amplifier itself. Since the sense amplifier is essentially a differential amplifier, any mismatch in the threshold voltage and the gain factor of the transistors in the two arms of the amplifier shows up as an input offset voltage. In presence of such input offset voltage, the sense amplifier firing signal will have to be further delayed so that the differential voltage developed at the BL and BL' lines can compensate the offset voltage. Since this problem arises *AT THE LOCATION* of the signal amplification, it is not possible to predict the offset a-priori, or even track the offset as in the case of bit line delay tracking. So the sense amplifier design is typically done for the worst case offset condition, by delaying the firing signal in order to compensate the offset voltage. This approach will slow down the sense amplifier significantly depending on the magnitude of the mismatch.

As the CMOS technology is scaled to the deep sub micron regime, the random dopant fluctuation effects will increase, thereby making the transistor mismatch worse. If a fab needs a design index of 6σ for yield consideration, the sense amplifier firing will be delayed to cancel the 6σ transistor mismatch. Assuming a normal distribution of transistor mismatch across the wafer lots, the Fig. 2 gives the percentage of sense amplifiers within certain σ value. It should be noted that a 1σ value corresponds to 84% of the devices. In other words, the design index of 6σ implies that for the sake of 16% more devices, 84% of the devices are penalized with respect to the speed. Had it not been for the delayed sense amplifier firing, these 84% of the devices would be in a different higher speed bin, which in turn translates to higher revenue for the fab! At the same time delaying the sense amplifier firing by 1σ value to get high speed IC's means 16% lower yield. When a fab is shipping millions of IC's, 16% lower yield implies a big hit on revenue. Hence in order to get the best of speed and yield, one would require a programmable sense amplifier firing design technique.

Some techniques have been proposed to do offset cancellation of the sense amplifier. However, these suffer from the drawback of slowing down the intrinsic speed of the sense amplifier due to the loading of the output nodes by extra circuitry required for mismatch compensation. Furthermore the mismatch compensation is not to the tune of 100%.

LIMITATIONS

Typical 60 design index for the fab results in slowing down majority of the chips, which are inherently fast due to lower transistor mismatch. In the Deep Dub-Micron technologies, the speed difference will be more than a factor 2 for the 6σ design index versus 1σ design index. i.e. the memory chip which could potentially run at 2GHz, will have to be marketed with a 1GHz label

A manufacturer who likes to be the first to introduce the fastest chips into the market and thereby capture the market can potentially run the fab with 1σ design index. However, the associated loss of yield is enormous which again impacts the bottom line of the fab.

Some of the techniques proposed such as cancellation of sense amplifier offset suffers from the disadvantage of slowing down the inherent response speed of the sense amplifier.

OBJECTS OF THE INVENTION

It is the primary object of the invention to design a novel circuitry to fire the sense-amplifier in a memory circuit wherein, the firing delay introduced is a function of transistor mismatch in the sense amplifier resulting after the fabrication.

It is another object of the invention to invent a circuitry to extend to have 2 or more speed bins by introducing different delay paths controlled by multiplexer.

It is another object of this invention that to apply this circuitry to any VLSI circuit wherein the transistor mismatch happens to be a speed and yield critical path.

It is another object of the invention to split the firing delay path into two such as *fast* path and *slow* path, which would correspond to lower transistor mismatch and higher transistor mismatch.

It is another object of the invention to adjust the timing for the two paths by a pass gates, buffers, passive interconnect resistor or any other delay element.

It is another object of the invention to use a 2 to 1 multiplexer to select either *fast* or *slow* path using the control signal SPEED to select all the signals of such multiplexers in a single chip to connect together and to bring out the signal to correspond with the SPEED pad.

It is another object of the invention to sort the functional chips as *slow* chips and *fast* chips by testing the functionality with the SPEED pad connected to logic "1" and logic "0".

PROPOSED SOLUTION

Now this invention will be described in detail. The description of the invention will refer to the accompanying drawings of the complete specification. The descriptions will extensively deal with the nature of the invention and the manner in which it is to be performed.

The statements of the drawings, which accompany this complete specification, are as follows:

Fig. 1: Shows the Circuit Diagram of Conventional sense amplifier firing for SRAM circuit;

Fig. 2: Shows the graphical representation in respect of the Percentage of devices within certain mismatch value for Gaussian distribution;

Fig. 3 (a): Split sense amplifier firing path with multiplexer according to the invention;

Fig. 3 (b): Shows the Circuitry indicating possible delay element and multiplexer

Implementation;

Fig. 4: Shows the details of Hardwiring for fast and slow chips during packaging.

Fig. No. 1 shows the conventional memory design with respect to sense amplifier firing signal (prior art). A Latch type sense amplifier is shown in Fig. No. 1 here for illustration, the proposed invention could be applied to any sense-amplifier configuration. The three transistor pairs MN1-MN2, Mpass1-Mpass2 and MP1-MP2 constitute the sense amplifier. The process variations result in device mismatch in these matched pairs, which manifests itself as the offset of the sense amplifier. The conventional design (prior art) attempts to accommodate the worst case offset, resulting in pessimistic design by building in slackness to achieve 6σ design index. The design slackness is reflected in the delayed sense amplifier firing signal. The 6σ design index achieves the high yield (Fig. 2) but at the expense of speed.

The proposed invention is illustrated in Fig. 3 (a) and (b). In this proposed invention the sense amplifier firing path is split into two labeled as 1σ path and 6σ path. One of them is corresponding to "fast chips" and the other one to "slow chips". The delays in the fast and slow paths are appropriately adjusted depending on the required design index. For the example shown in the Fig. 3 (a), the fast path corresponds to 1σ and the slow path corresponds to 6σ design index (transistor mismatch). These numbers could be different depending on the requirement of a particular implementation. The delays in these two paths can be tuned by using delay elements such as pass gates, buffers, passive interconnect resistors etc as shown in Fig. 3(b). The delay in pass gate and buffer can be adjusted by varying the length and width of the transistors whereas the delay in the interconnect can be adjusted by varying length and width of metal line. The implementation of 2-1 multiplexer is shown in Fig. 3(b). The 2-1 multiplexer selects one of the two paths (In-1 and In2) to fire the sense amplifier (Out) as shown in Fig. 3(a). The status of select input (GND or VDD) of the multiplexer determines whether In-1 or In-2 is transmitted to the output. The select inputs of all such multiplexers in a single chip are connected together and brought out as the "SPEED" pad as shown in Fig. 4. . When "SPEED"=0, the fast path is used to control sense amplifier

and when "SPEED"=1, the slow path is used. (The logic could also be reversed, by changing the multiplexer connections appropriately). After the fabrication is completed, the IC's are tested at wafer level to assess the functionality. If a particular chip works with SPEED=0, then it is marked as fast chip. Otherwise, the chip is re-tested with SPEED=1, and the functional chip is marked as slow chip. Then after dicing, the chips are hardwired into fast or slow bins during the packaging step. For all the fast chips, the SPEED pad is shorted to GND pad and for the slow chips the SPEED pad is shorted to VDD pad as shown in Fig. 4. The VDD and GND pads are adjacent to SPEED pad. Note that the SPEED pad need not be connected to an external package pin and hence the hardwiring process does not impact the connectivity of the chip in the system design.

This results in 84% of the chips in high speed bin and 16% of the chips in low speed bin without compromising on memory speed and yield. This in turn translates into a very significant enhancement in the revenue of the fab.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention.

CLAIMS

1. **A** system for high yield and speed enhancement of semiconductor integrated circuits such as SRAM and DRAM using post fabrication transistor mismatch compensation circuitry consisting of sense amplifier, multiplexer, delay elements and hardwiring arrangement during packaging, comprising a novel sense amplifier instrument for providing high memory yield and speed enhancement using post fabrication, transistor mismatch compensation circuit, wherein sense amplifier firing path being split into two paths, one path corresponding to fast chips and the other to the slow chips, means for effecting delay in the fast and slow paths and multiplexer which selects one of the two parts to fire the sense amplifier such that more than 80% of the memory integrated circuits (fast path) are very fast and the rest of the memory integrated circuits (slow path) are still functional without compromising the yield.

2. A system for high yield and speed enhancement of semiconductor integrated circuits using post fabrication transistor mismatch compensation technique as claimed in Claim lwherein a split firing path one corresponding to "*fast* ***chips"*** and the other one to "*slow* ***chips"*** wherein the delay in the *fast* and *slow* paths are adjusted depending on the required design index.

3. **A** system for high yield and speed enhancement of semiconductor integrated circuits using post fabrication transistor mismatch compensation technique as claimed in Claim 1 wherein the *fast* path corresponds to No and the *slow* path corresponds to Mσ design index (transistor mismatch) wherein these numbers could be different depending on the requirement of a particular implementation thus wherein M > N.

4. **A** system for high yield and speed enhancement of semiconductor integrated circuits using post fabrication transistor mismatch compensation technique as claimed in Claim 1 wherein the delay in the two paths can be tuned by using delay elements such as pass gates, buffers, passive interconnect resistors.

5. A system for high yield and speed enhancement of semiconductor integrated circuits using post fabrication transistor mismatch coinpensation technique as claimed in Claim 1 wherein the 2-1 multiplexer selects one either *fast* or *slow* path using the control signal SPEED thus all control inputs of such multiplexers in a single chip are connected together and brought out which corresponds to the "SPEED" pad.

6. A system for high yield and speed enhancement of semiconductor integrated circuits using post fabrication transistor mismatch compensation technique as claimed in Claim 1 wherein the *fast* path is used when "SPEED" =0 and the *slow* path is used when "SPEED" = 1 thus the logic could also be reversed, by changing the multiplexers connections appropriately.

7. A system for high yield and speed enhancement of semiconductor integrated circuits using post fabrication transistor mismatch compensation technique as claimed in Claim 1 wherein after the fabrication is completed, the chips are tested at wafer level to assess the functionality and marking a particular chip as *fast* if the SPEED =0 and *slow* if the SPEED=1 thus dicing and *hardwiving* into *fast* or *slow* bins during the packaging step.

8. A system for high yield and speed enhancement of semiconductor integrated circuits using post fabrication transistor mismatch compensation technique as claimed in Claim lwherein for all the *fast* chips, the SPEED pad is shorted to GND pad and for the *slow* chips the SPEED pad is shorted to VDD pad wherein the VDD and GND pads are adjacent to SPEED pad.

9. A system for high yield and speed enhancement of semiconductor integrated circuits using post fabrication transistor mismatch compensation technique as described in the Complete specification and as illustrated by way of drawings.

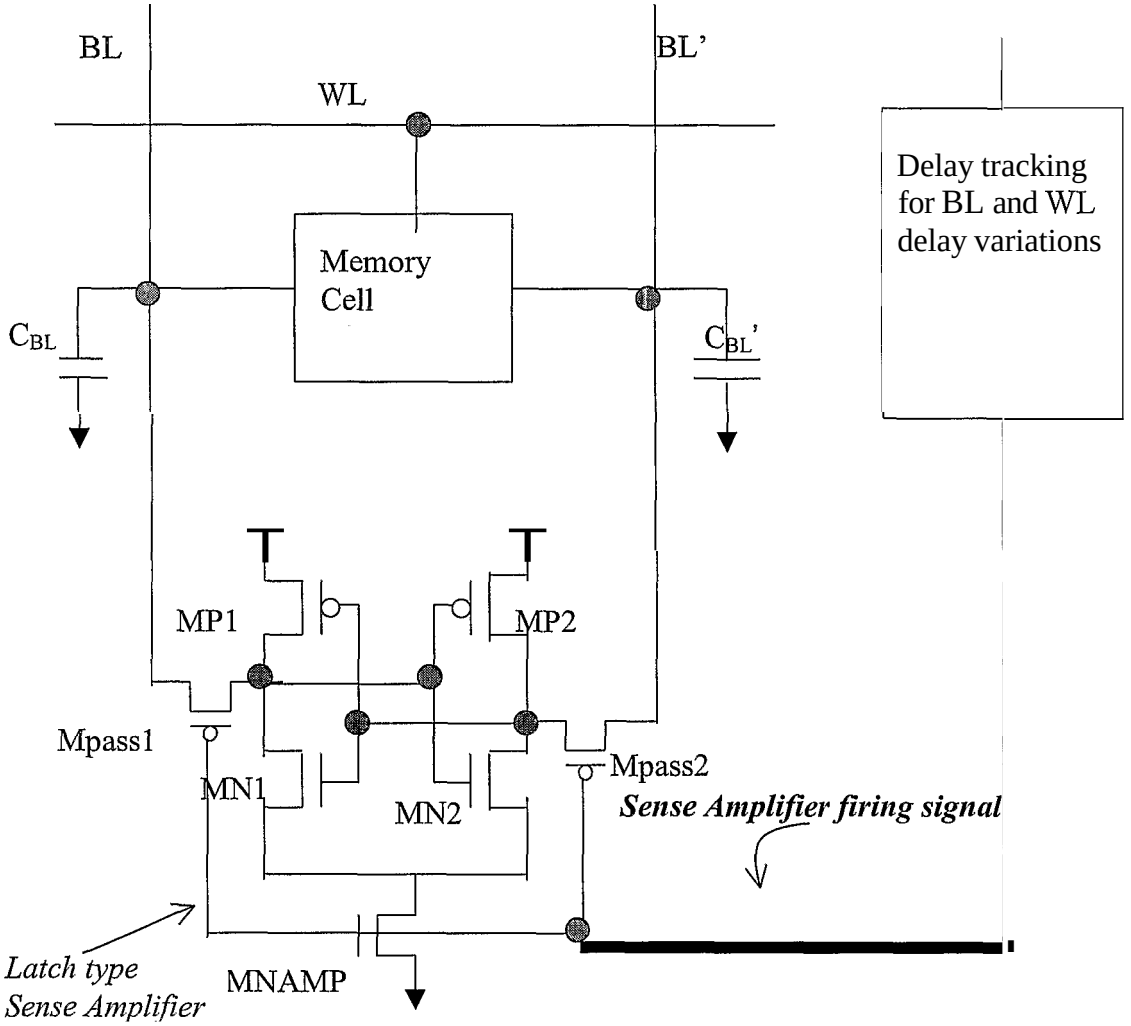
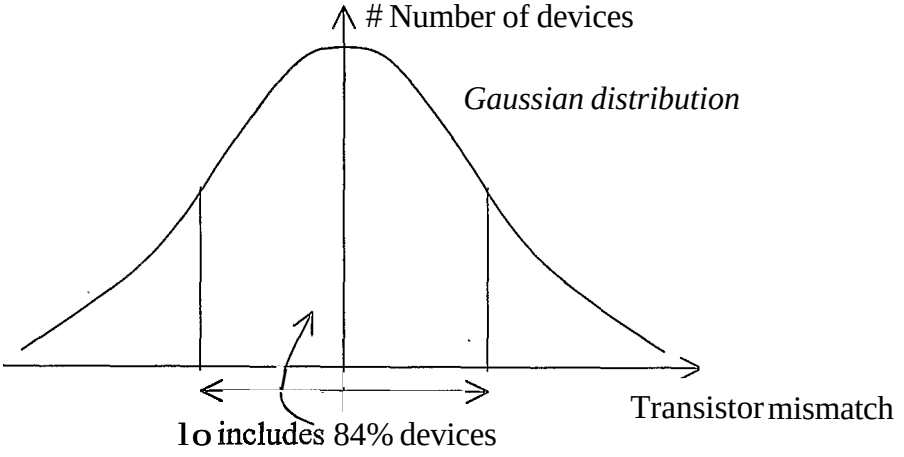

BL
BL'
WL
Memory Cell
C_{BL}
C_{BL}'
Delay tracking for BL and WL delay variations
MP1
MP2
Mpass1
Mpass2
MN1
MN2
Sense Amplifier firing signal
Latch type Sense Amplifier
MNAMP

FIG. 1



Design Index (o)	Percentage of Devices
1	84.1344740
2	97.7249938
3	99.8650033
4	99.9968314
5	99.9999713
6	99.9999999

FIG. 2

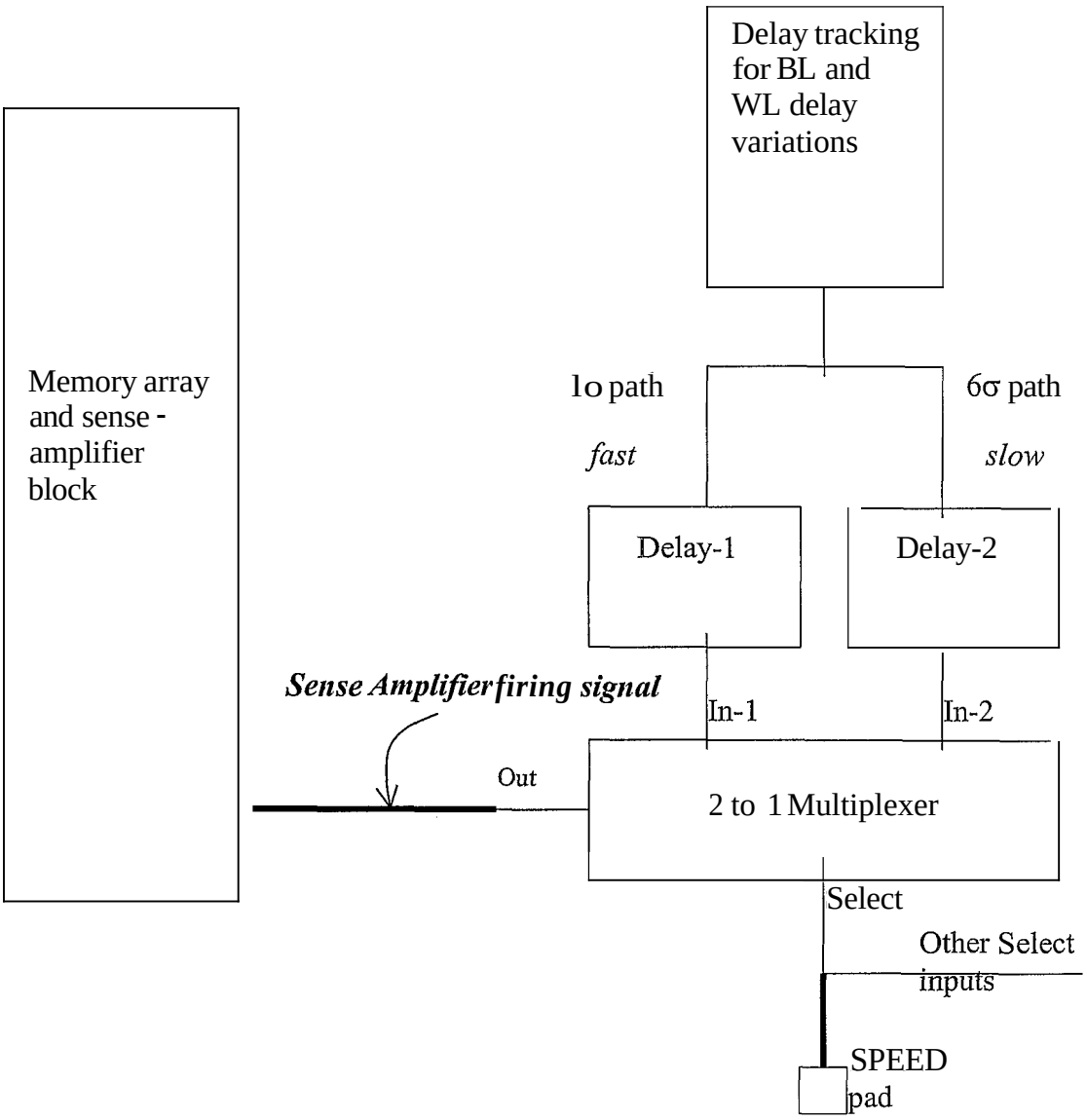
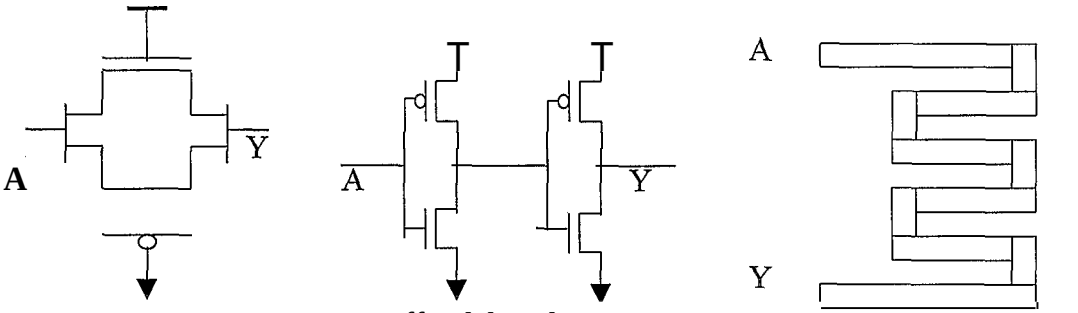

Delay tracking for BL and WL delay variations
Memory array and sense - amplifier block
1σ path
fast
6σ path
slow
Delay-1
Delay-2
Sense Amplifier firing signal
In-1
In-2
Out
2 to 1 Multiplexer
Select
Other Select inputs
SPEED pad

Fig. 3 (a)



Pass gate delay element

Buffer delay element

Interconnect delay element

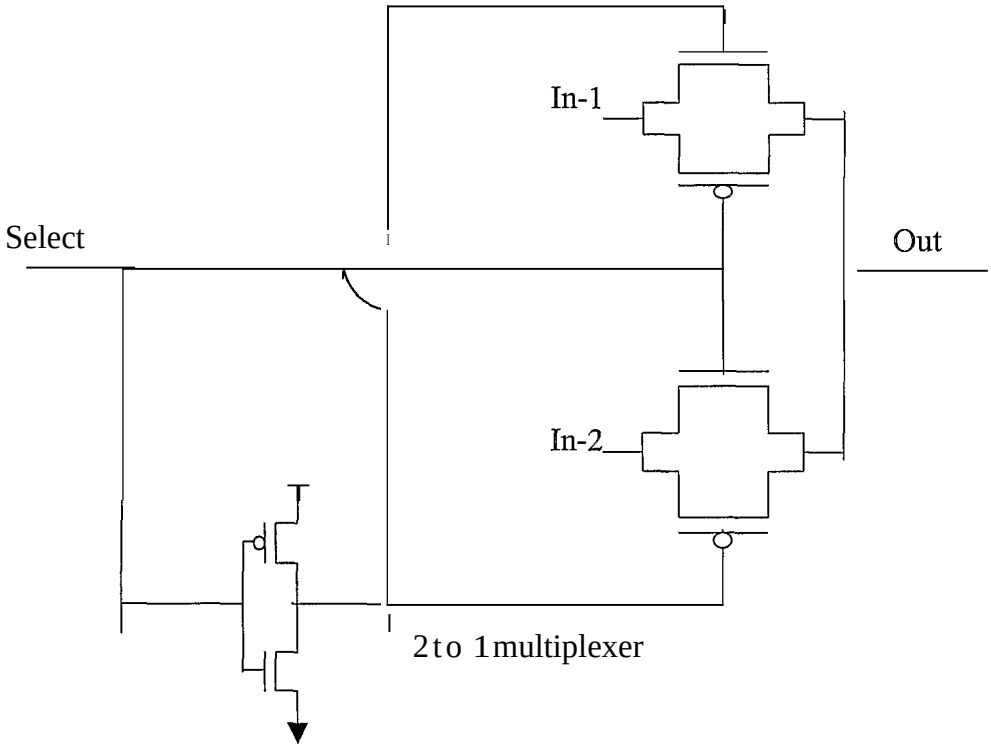
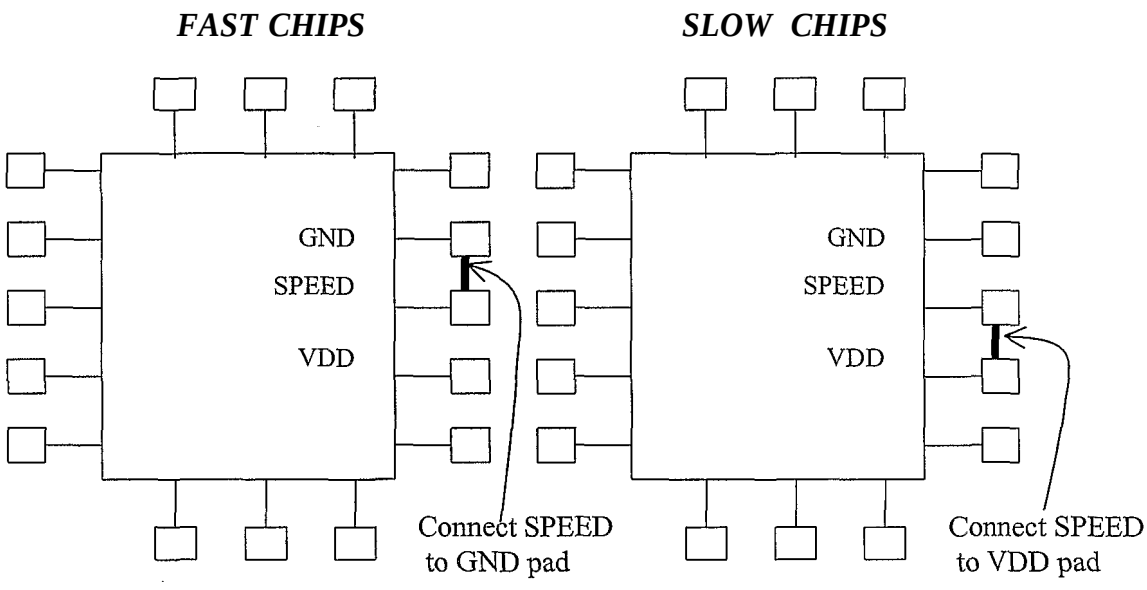


Fig. 3 (b)



NOTE: The pads have been shown at the periphery of the chips in this implementation. However, the pads could also be in the core as in the case of flip-chip packaging. This technique could be applied irrespective of the type of packaging

Fig. 4