A HYBRID COMPUTER FOR X-RAY CRYSTALLOGRAPHY

By S. Harigovindan

(Department of Physics, Indian Institute of Science, Bangalore-12)

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Abstract

A hybrid computer for structure factor calculations in X-ray crystallography is described. The computer can calculate three-dimensional structure factors of up to 24 atoms in a single run and can generate the scatter functions of well over 100 atoms using Vand *et al.*, or Forsyth and Wells approximations. The computer is essentially a digital computer with analog function generators, thus combining to advantage the economic data storage of digital systems and simple computing circuitry of analog systems. The digital part serially selects the data, computes and feeds the arguments into specially developed high precision digital-analog function generators, the outputs of which being d.c. voltages, are further processed by analog circuits and finally the sequential adder, which employs a novel digital voltmeter circuit, converts them back into digital form and accumulates them in a dekatron counter which displays the final result. The computer is also capable of carrying out 1-, 2-, or 3-dimensional Fourier summation, although in this case, the lack of sufficient storage space for the large number of coefficients involved, is a serious limitation at present.

Introduction

In X-ray crystal structure determination, two types of computations, namely those of electron density and structure factor, are repeatedly required, and small-scale special purpose computers for these computations are extremely useful in speeding up the structure determination. A hybrid computer, developed and constructed by the author (1964), mainly for the second type of computations, is described in this paper. The quantities to be computed are

$$F_{hkl} = \sum_{j}^{N} f_j \exp. 2\pi i (hx_j + ky_j + lz_j) \qquad (1)$$

where h, k, l are integers, x_j, y_j, z_j are the normalised co-ordinates and the atomic scatter factors f_j are functions of (hkl). The major requirements to be met for these computations are provisions for storage of the co-ordinates for a sufficiently large number of atoms ($N > 20$), the generation of the scatter functions of various atoms and finally economy and ease of operation.

A large number of special purpose computers for these computations are described in literature. Most of them are simple hand calculators or computing aids (Lipson and Cochran, 1953; Van der Waalt, 1956; Schaeffer, 1959; Linék and Novak, 1960; Harigovindan, 1965). Optical analog techniques (Bragg, 1944; Taylor *et al.*, 1952) though fast and economical are not very accurate and are afflicted by the "Phase Problem". Among full-scale computers, Vand's mechanical computer (1950) and Pepinsky's electronic analog computer S-FAC (1952), are worthy of note. However the former is incapable of generating f_j, while the latter is confined to two-dimensional calculations. In these respects the present computer is superior and is probably the only special purpose computer which can fully meet the requirements for conventional structure factor calculations. It should be mentioned that the popularity of the special purpose computers is some what diminished with the advent of the modern electronic digital general purpose computers, the speed, accuracy and flexibility of which cannot be matched by the former. Nevertheless, due to the low costs and ease of operation of the former, they still remain useful.

BASIC PRINCIPLES

With the development of a Fourier synthesiser (Krishnan, 1959) for electron density calculations in this laboratory, interest was taken in developing a structure factor computer. One of the earliest designs involved the use of AC resolvers positioned by rotary switches (Venkatakrishnan, 1958). This was later discarded for a d.c. serial machine employing analytical approximations for generating f_j (Suryan and Krishnan, 1959; Venkatakrishnan, 1959, 1960, 1961). Some of these basic principles are retained in the present computer though it exploits digital techniques better. The machine actually calculates

$$\frac{\text{Real}}{\text{Imag.}} F_{hkl} = \sum_{j=1}^{N} f_j \frac{\cos}{\sin} (HX_j + KY_j + LZ_j) \tag{2}$$

where

$$f_j = P_j e^{-A_j S} + Q_j e^{-B_j S + K_j} \tag{3}$$

The above form for f_j permits the use of either Vand *et al.* (1957) ($R_j \equiv 0$, $S = \sin^2\theta$) or Forsyth and Wells (1959) ($R_j \neq 0$, $S = \sin^2\theta/\lambda^2$) approximations. The former is particularly convenient since the isotropic temperature correction can be included by suitable additions to A_j and B_j. The actual ranges and accuracy of the machine variables in equation (2) available in the computer are given in Table I and are adequate for all practical purposes (except in the case of A_j and B_j for certain light atoms when using Forsyth and Wells approximations).

Although the max. value of N is only 24 for a single run, it is possible to calculate F_{hkl} for any $N > 24$ by block-wise summation of 24 atoms each, in repeated runs. The application of the computer for Fourier summation is evident.

Consider the triple Fourier series

$$\rho = \sum_h \sum_k \sum_l F_{hkl} \cos(hx + ky + lz). \tag{4}$$

Here for each point (xyz) the integers (hkl) vary from term to term whereas in F_{hkl} calculation, (hkl) are constant and (xyz) vary. Thus by substituting (*see* Table I) $H = 100x$, $K = 100y$, $L = 100z$ and $X_j = h_j/100$, $Y_j = k_j/100$,

TABLE I

	Data	Range	Precision (in steps of)	Mode of data representation
..	XYZ	0– 0·999	0·001	Matrix Switches
..	A	0– 9·99	0·01	do.
..	B	0–99·9	00·1	do.
..	HKL	±99	1·0	Decade Switches Signs set on SPDT Switches.
..	S	0– 0·999	0·001	do.
..	PQR	1–10	Continuous	Potentiometers.
Rl	..	..	..	Dekatron Counter.
..	F_{hkl}	999·9	0·1	Sign displayed by neon lamps.
Im	..	99·99	0·01	Real/Imag. Selected by switch.

Max. Value of N = 24.

No. of Scatter functions available = 9.

$Z_j = l_j/100$ and $P_j = F_{hjkjlj}$, $S = Q_j = R_j = O$ in equation (2), ρ can be calculated directly by the computer. However only 9 different values of P_j are available for a single run (Table I) so that a large number of repeated runs will be required to cover the large number of terms (about 200 for typical 2-dimensional summation) and the process is somewhat laborious though faster than hand calculation.

The block diagram of the computer is shown in Fig. 1. The digital part selects the data for each atom, one at a time, calculates the arguments

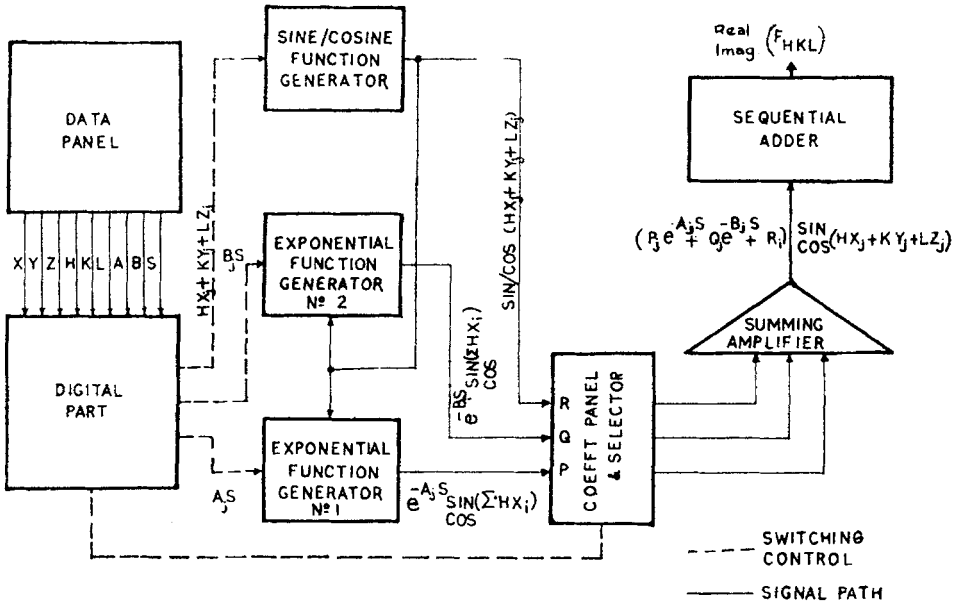

FIG. 1. Block diagram of the computer.

and feeds them into the proper digital-analog function generators which actually consist of high precision resistance potential-divider circuits switched by relays. The d.c. output voltages of these are then multiplied by the appropriate coefficients and summed up by the summing amplifier to produce a d.c. voltage proportional to the selected term. The sequential adder, which is a digital voltmeter, measures this voltage and generates a proportional number of pulses which are counted by the final accumulator. The latter is a reversible dekatron counter which adds or substracts as required after comparing the signs of the input voltage and its own contents. The computer repeats the above cycle for all the N terms so that by the end of a run the dekatron counter accumulates and displays the required sum as a signed 4-digit number.

Evidently the computer functions as a digital computer with analog function generators and actually goes through the following program.

Instruction No.	Instruction
1	Start (set $j = 1$).
2	Compute H_i X_j and store in the argument accumulator (AA).
3	Compute KY_j and add to AA contents.
4	Compute LZ_j and add to AA contents.
5	Read in the AA contents to sin/ cos F.G.
6	Clear AA and compute A_jS.
7	Read in the AA contents to Exp. F.G. No. 1.
8	Clear AA and compute B_jS.
9	Read in the AA contents to Exp. F.G. No. 2.
10	Add the summing amp. out put to final accumulator contents.
11	Clear the function generators and set $j = j + 1$.
12	Stop if $j > N$, otherwise go to inst. No. 2.

The first instruction is carried out manually by the operator by a push-button operation while the instructions 2 to 10 are controlled by a program counter and the last two by means of certain relay circuits as described later.

The various parts of the computer may be considered in brief detail now.

The Digital Part

The functions of the digital part are the calculation of arguments and over-all control of program sequence. This requires that it should perform addition, subtraction and multiplication of three-digit numbers. Thus it is a quasi-synchronous d.c. digital machine, with floating point decimal arithmetic (the decimal point is taken into account only when reading into the F.Gs). The numbers are binary coded decimals, the binary digits 1 and 0 being represented by 50 V and 75 V respectively. The block diagram is shown in Fig. 2.

The major waveforms in the digital part are shown in Fig. 3. Two sets of clock pulses delayed with reference to each other by half the period (at a frequency of about 25 kcps.) are generated, one (C_1 δ of which is used only to drive the minor cycle counter which has 4 binary stages and associated

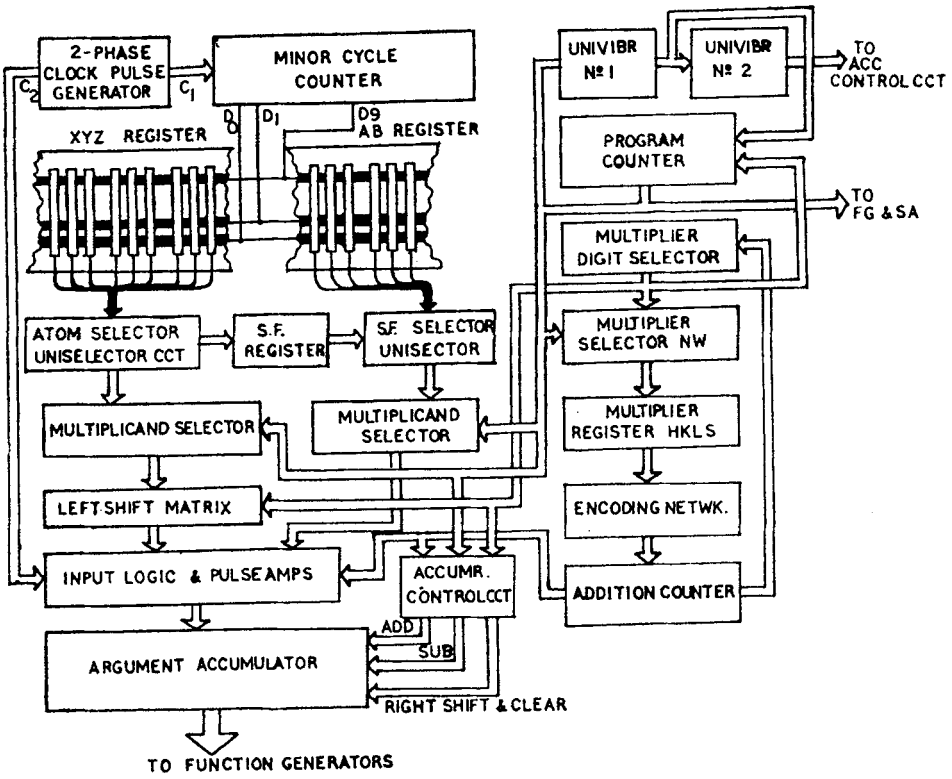

FIG. 2. Block diagram of the digital part.

diode logic to generate the digit gate pulses (D_n) and the operational pulses (O_n) shown in Fig. 3. The total width of D_n which represents the decimal digit n is n clock-pulse intervals. To minimise the number of diodes, only D_1, D_2, D_4 and D_8 are directly generated, the rest being combinations of these, which accounts for their odd shapes. The counter recycles at every 12th pulse, so that the above forms are generated at 1/12th of the clock-pulse frequency.

The arithmetic operations may be considered in detail now. The argument accumulator (AA) is a reversible 4 stage binary coded decade counter-*cum*-shifting register. The method of feeding a decade digit into an accumulator stage is evident from Figs. 4 and 5. The required D_n and C_2 are fed into the AND gate, the ouptut of which will be n clock-pulses, which are counted by the stage, so that n is added (or subtracted by reverse counting) to the contents of that stage. Parallel addition is used so that each stage receives the proper number of pulses simultaneously during the first of clock-

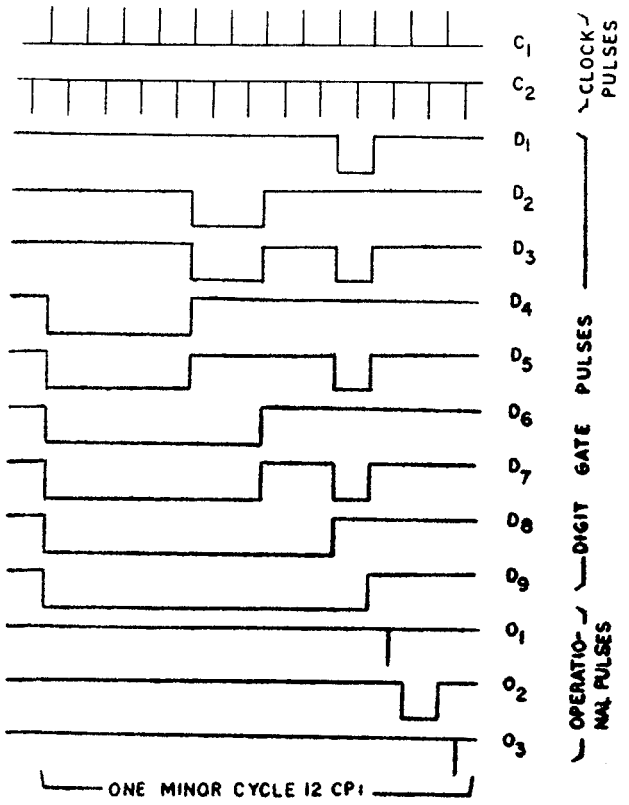

FIG. 3. Waveforms in the digital part.

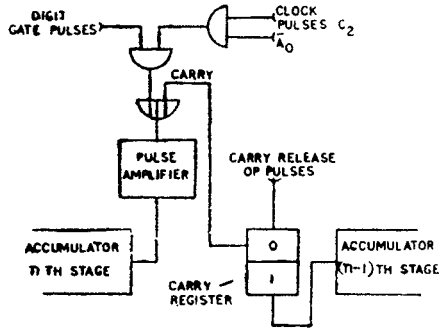

FIG. 4. Input logic for an argument Accumulator stage. The signal $\bar{A}_0 = 1$ when AC is in a non-zero state.

pulse intervals of the minor cycle. The carry propagation is delayed and takes place during the remaining three c.p. intervals of the minor cycle by

means of the circuit shown in Fig. 4. Thus it is evident that to add, say ·3720 to the accumulator contents, the stages 1, 2, 3 and 4 receive respectively 0, 2, 7 and 3 pulses during a minor cycle. Thus the time taken for one addition is one minor cycle. Negative values of X, Y and Z are fed in as complements of 1·000, while for negative values of H, K and L the accumulator counting is reversed to subtract by proper circuits.

Multiplication is carried out as usual by repeated addition and shifting. Evidently two types of multiplications are required.

1. For products of the type HX_j, only (HX_j modulo 1·000) is required so that only the three least significant digits of the product need be retained by AA. This is achieved by shifting the multiplicand left by means of a left-shift matrix and allowing AA to overflow.

2. For multiplications of A_jS and B_jS, only the three most significant digits are required which is achieved by shifting the accumulator contents right by means of properly timed O_2 pulses. The shifting register circuitry is similar to that described by Booth (1953). The counteraction of the accumulator is inhibited during shifting.

The numbers handled by the digital part may be divided into two classes. The multiplicands X_j, Y_j, Z_j, A_j and B_j are represented by digit gate pulses and vary from term to term, while the multipliers H, K, L and S are constant throughout a run and determine the number of repeated additions as follows. The whole process of multiplication is controlled by the three counters, the Program Counter (PC), the Multiplier Digit Selector (MDS) and the Addition Counter (AC), the last two recycling every 4 and 10 steps respectively. AC is driven by O_3 pulses until it reaches zero where it will remain unless reset to some other state. Only when AC is at zero, MDS is driven by O_1 (provided the program requires argument calculation) and only when AC is not at zero, digit gate pulses are added to AA as shown in Fig. 4. PC selects the multiplicand (*i.e.*, the three D_n pulses) and the multiplier, through diode selector networks as in Fig. 2. Since AC and MDS are initially at zero, MDS is stepped once, selecting the first multiplier digit say n, and through the encoding network, resets AC to $(10-n)$. AC, now being in a non-zero-state, is driven to zero by O_3, in minor cycles later during which time the multiplicand is added n times in AA. After shifting, MDS selects the second multiplier digit and so on, completing the multiplication.

The multiplicands which require maximum storage space are stored on matrix switches (Harigovindan, 1965) in XYZ and AB registers (Fig. 2). To each multiplicand 3 vertical strips are assigned corresponding to three

decimal digits and by inserting plugs into proper row each vertical strip can select the proper D_n, which are connected to the 10 horizontal strips. Two sets of uniselectors, the atom selector (AS) and the scatter function selector (SFS) selects the proper blocks of vertical strips out of these representing X_j, Y_j, Z_j and A_j, B_j respectively. Further selection is carried out by diode networks as mentioned earlier.

The PC, which is a 4-stage binary counter with associated translating network, executes the instructions Nos. 2 to 10 as it steps through its 1 to 9 states respectively. It is driven by MDS during argument calculation steps and by univibrator No. 1 during argument read-in instructions. The duration for which PC remains at each of these latter steps is determined by its stable period (80 msec). Also whenever PC changes from the above steps, it triggers univibrator No. 2 (20 msec) during the unstable period of which MDS is prevented from starting the calculation and a train of "Right-shift" pulses is applied to clear AA.

The atom selector consists of two 25-way uniselector of 8 and 6 levels. The first position of these is used as a " Ready " position and the remaining 24 positions correspond to $j = 1$ to 24 respectively. Of the 14 levels, 9 levels are used to select $X_jY_jZ_j$ and one level is used to position SFS through the 24 decade switches in SF Register. The " Reset ground " for all binaries in the digital part is grounded through a level of AS with nonbridging wiper, in series with a make contact on the SFS control relay so that digital part will not function when these uniselectors are stepping and also when AS is at the " Ready " position. This also permits resetting of all binaries after calculating each term when the AS is stepped by means of a relay operated by a univibrator which is triggered by the sequential adder. Also certain relay networks ensure that AS is recycled to " Ready " position whenever it reaches a position $j = N + 1$ in accordance with instruction No. 12, N being set on a 24-way switch manually.

The SFS also consist of two 25-way uniselectors of 8 and 4 levels. Only the first 9 positions out of 25 are used corresponding to the 9 scatter functions. 6 levels are used for selecting A_j and B_j while 3 levels are used to select the potentiometers on which P_j, Q_j and R_j are set. The position of the SFS for each position of AS is determined by corresponding 24 decade switches in the SF register.

Function Generators

The function generators accept the arguments as digital numbers from AA and provide sin/cos function as well as its products with exponenti$_a$

functions and thus belong to digital-analog type (Hoffheimer and Perry, 1958). The sin/cos F.G. has been described by the author (under publication) in detail elsewhere so that it is sufficient to mention that it generates sin/cos function (full scale 10 volts) to an accuracy of 0·1%.

The exponential function generator No. 1 is shown schematically in Fig. 6. The argument x for the function is provided by AA in the form

$$x = a_1 + \frac{a_2}{10} + \frac{a_3}{100} \tag{5}$$

where a_1, a_2, a_3 are integers (0 to 9) and it is evident that

$$e^{-x} = e^{-a_1}\, e^{-a_{2/10}}\, e^{-a_{3/100}}. \tag{6}$$

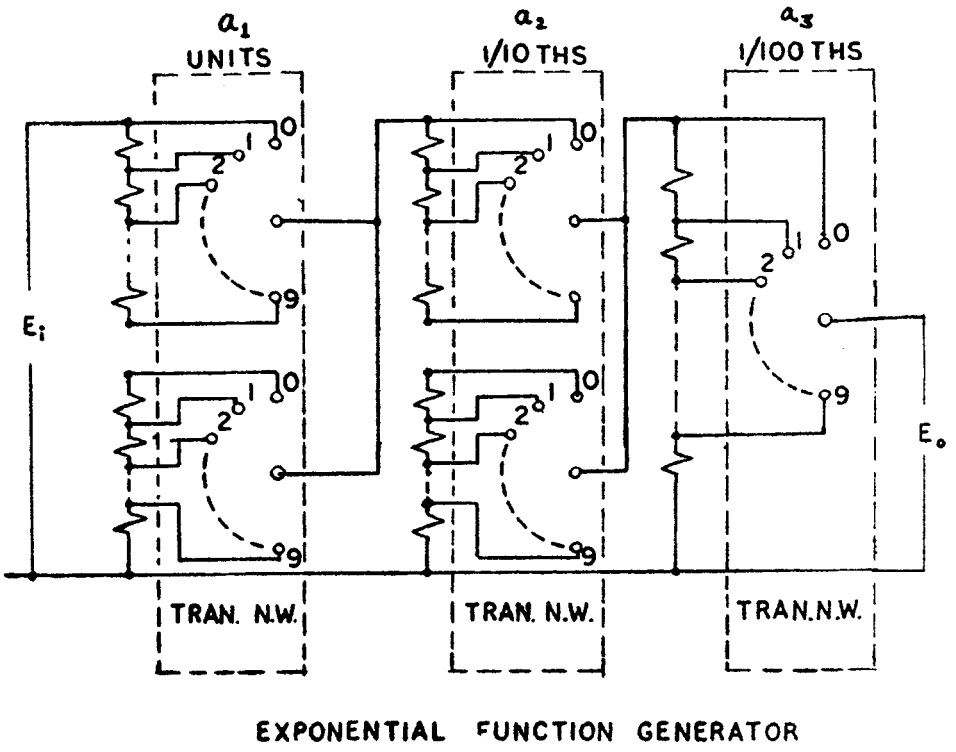

FIG. 6. The exponential function generator No. 1.

The three stages have potential division ratios of e^{-a_1}, $e^{-a_{2/10}}$ and $e^{-a_{3/100}}$, respectively so that the output is $E_i\, e^{-x}$, E_i being the input voltage. To provide for loading correction and to keep the input resistance constant (4 KΩ) both the arms of the first two potential divider stages are varied. The 10-way switches of Fig. 6*a* are actually relay translating networks shown

in Fig. 7. Each decimal digit (a_1, a_2, a_3) being supplied by AA in binary 8421 code, is held by 4 relays, representing correspondingly numbered binary digits.

In the case of Exp. F.G. No. 2 since the range of B_j is 0 to 100, the argument is given by

$$x = 10a_1 + a_2 + a_3/10. \tag{7}$$

Since $e^{-x} \ll 0{\cdot}001$, for $a_1 \geqslant 1$, negligible error is introduced by assuming $e^{-x} = 0$ for $a_1 \geqslant 1$. Hence in this case the potential divider stages corresponding to a_2 and a_3 only are provided, and a_1 is set on the 4 relays of Fig. 7, which ground the output whenever $a_1 \geqslant 1$.

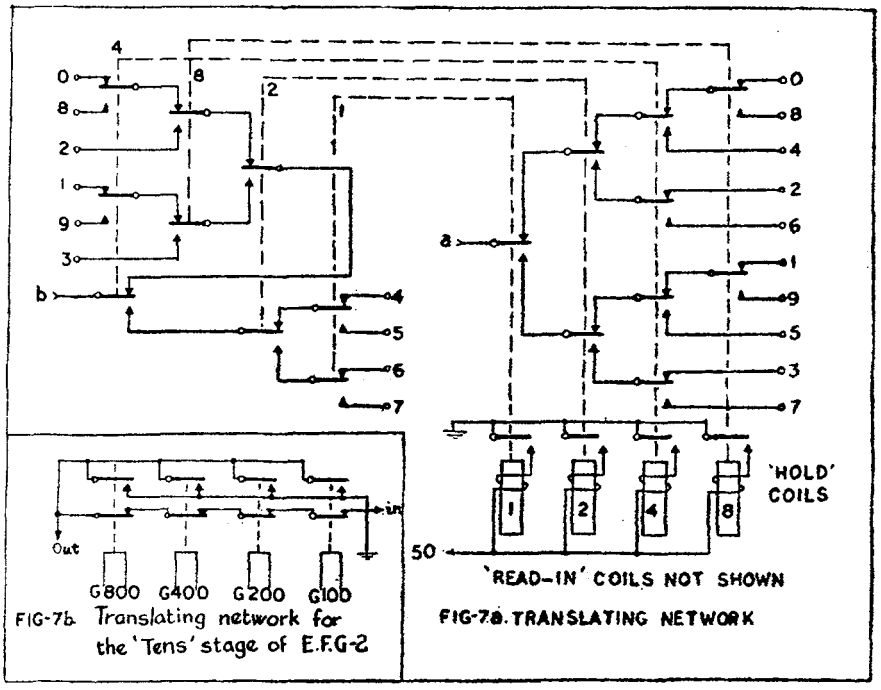

FIG. 7. The relay switching circuits for a stage of the exponential function generator.

The numbers a_1, a_2, a_3 are from the outputs of the stages 4, 3, 2 respectively of AA. The argument read-in-process may be considered now. Each of the 12 relays for each function generator (similar to those of Fig. 7) have two coils, one for " Read-in " (20 KΩ, 50 V) and one for " Hold " (2 KΩ, 50 V). The actual read-in circuit for a stage is shown in Fig. 8. The " read-in " coils (E, F, G) of the corresponding relays in the three function generators are connected to the plates of the switching tubes (V_4 and V_5 of Fig. 8), which

are switched by the corresponding binaries in AA. However the plate voltage to those tubes are applied only when one of the " Function-selectro relays" RE, RF, RG are operated by PC during "read-in" instructions. Thus the " read-in " coils of proper relays of the selected function generator are energised for the duration (80 msec. as mentioned earlier) when PC is at the corresponding step, after which the function selector relay is deenergised. The relays operated during this interval remain self-locked through their " hold " coils, thus holding the argument until when the calculation of the term is over and AS steps to the next position, a relay cuts-off the power to the " Hold " coils thus clearing the arguments from all function generators. Since the release time of the function selector relays is high compared to argument calculation time, to avoid " cross-talk " the next argument calculation is delayed by 30 msec. until these relays are completely released, as mentioned earlier.

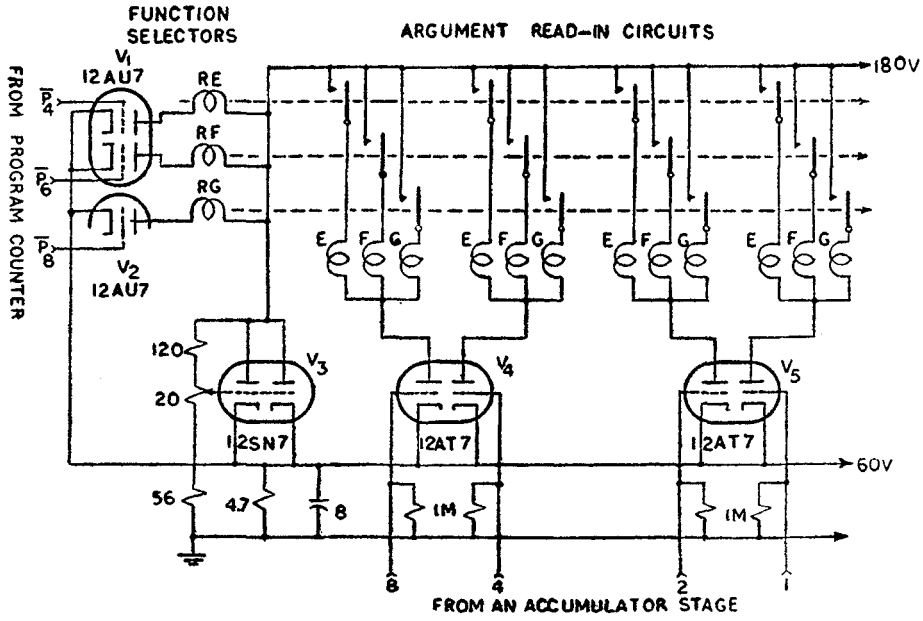

FIG. 8. The function selector and argument read-in circuits.

The outputs of the function generators are fed to the summing amplifier through unity-gain buffer amplifiers to prevent loading.

SEQUENTIAL ADDER

The sequential adder is a novel " time-encoding " type digital voltmeter, using a loop of three operational amplifiers for automatic polarity selection as shown schematically in Fig. 9.

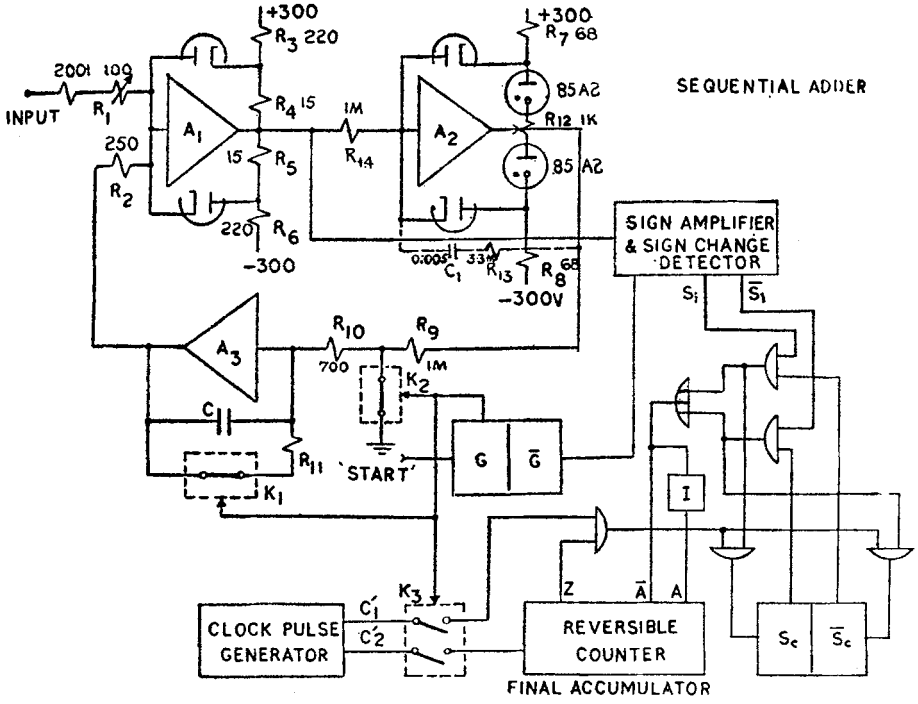

FIG. 9. The sequential adder.

The output of the summing amplifier is applied to the input of A_1. A_1 and A_2 function as comparators (Morril and Baum, 1962) using feed-back diodes and A_3 is an integrator, the output of which is held normally at OV with the electronic switches K_1 and K_2 closed. Thus the output of A_2 will be $\pm$ 85 V independent of the magnitude of the input but will have the same sign. When sequential addition is to be started PC triggers the binary G, which opens the switches K_1 and K_2 and closes K_3 which is normally open. Since the input of A_3 is a d.c. voltage having the same sign as the input, its output will be a saw tooth voltage having the opposite polarity. These two voltages are added by A_1 and when the output of A_1 starts changing sign (*i.e.*, when the input voltages cancel out each other), the sign change detector triggers G back, thus closing K_1 and K_2 and opening K_3. Evidently K_3 remains closed for an interval proportional to the input voltage, so that the counter receives a proportional number of pulses.

The novelty of the circuit lies in the use of the feed-back loop, by which the saw tooth generated has always a polarity opposing that of the input voltage, the slope remaining constant. Thus a single channel can deal with

positive and negative inputs. The RC circuits across A_2 is to ensure loop stability.

The final accumulator (FA) is a reversible dekatron counter (Harigovindan, 1963) which adds or subtracts depending upon two bias voltages A and $\bar{A}$ respectively. The sign of FA contents is displayed on neon lamps by the binary which also gives the outputs S_c (= 1 for positive sign) and $\bar{S}_c$. The sign of the input is given by the sign amplifier which gives the outputs S_i (= 1 for positive sign) and $\bar{S}_i$. Since FA adds when the two signs are same and subtracts when they are opposing, the bias for subtraction $\bar{A}$ is given by

$$\bar{A} = \bar{S}_c \bar{S}_i + \bar{S}_c S_i \tag{8}$$

and the bias for addition A is obtained by inverting $\bar{A}$ as shown in Fig. 9.

When a simple reversible counter crosses zero and counts backward to $-x$, it actually indicates only $(10^n - x)$ where n is the number of stages. Thus to provide proper sign and magnitude display, it is necessary to trigger the binary holding the FA signs into the proper state whenever the counter crosses zero. If $T(S_c)$ and $T(\bar{S}_c)$ are the pulses resetting the binary to S_c and $\bar{S}_c$ respectively, then

$$T(_c) = ZC_1' S_i \bar{S}_c \tag{9}$$

$$T(\bar{S}_c) = ZC_1' \bar{S}_i S_c \tag{10}$$

where Z is the signal given by FA when it reaches zero and C_1' are clock-pulses, with respect to which the clock-pulses C_2 (which are the actual driving pulses for FA) are delayed so that the sign change takes place while FA is still at zero.

Special circuits are provided for calibrating the sequential adder by means of R_1 (Fig. 9). There is also provision for selecting the full-scale accuracy to be 1% or 0·1%, the time taken for full-scale measurements being 25 msec. and 250 msec. respectively, since the clock-pulse frequency is only 4 kcps.

When the binary G triggers back at the end of the measurement, it also triggers a univibrator which causes AS to step as noted earlier.

CONSTRUCTION AND PERFORMANCE OF THE COMPUTER

The computer was constructed using locally available materials and is quite economic. The digital part makes use of optimally synthesised self-biased triode binaries (Harigovindan, 1962) and crystal diode-logic. The major aim in the design of the digital part was economy and simplicity rather

than speed, since the overall speed of the computer is limited by the relays and uniselectors. The function generators require high precision (0·1% tolerance) high stability resistors, which were mostly hand-wound from manganin wire. Some of the high value resistors proved unreliable later, which have been temporarily replaced by 1% carbon resistors. The relays and uniselectors used were all manufactured to the author's specifications by the I.T.I., Bangalore. The operational amplifiers used in the computer are quite simple, employing 3 twin triodes each, with a total open loop gain of 5×10^4 and band width of 50 cps., without any chopper stabilisation. The complete computer employs about 180 tubes, 260 diodes, 60 relays and 4 uniselectors and is housed in a $5' \times 1\frac{1}{2}' \times 6'$ cabinet.

The performance of the computer is quite satisfactory. The accuracy achieved in structure factor calculations is mainly limited by the errors already inherent in the approximations for f_j and the low accuracy to which A_j and B_j are specified. Average accuracy achieved is about 1% full scale. For Fourier summation the error is less because the exponential functions are not involved. The speed of the computer depends to a certain extent on the desired accuracy as already mentioned and is about 500 to 700 msec. per term.

Conclusion

The present combination of the analog and digital techniques is particularly suited for the problem. Since a large amount of data has to be processed, use of digital input has resulted in convenient feeding and economic storage of data, which would not have been possible with analog techniques. Another advantage is that the computer introduces no error in the calculation of $(HX_j + KY_j + LZ_j)$ modulo 1, whereas, if analog techniques were used the errors introduced will be quite high for large values of (H, K, L), unless very sophisticated techniques are used. On the other hand, the use of analog techniques for function generation provides comparatively simple and economic circuits with sufficient accuracy, whereas an equivalent digital system will be more costly and complicated.

The computer can easily be adapted for punched tape input and output, though the present input system, in spite of its limited capacity, has the advantage that data can be easily altered and the effects observed immediately, which is important to the crystallographer.

Acknowledgements

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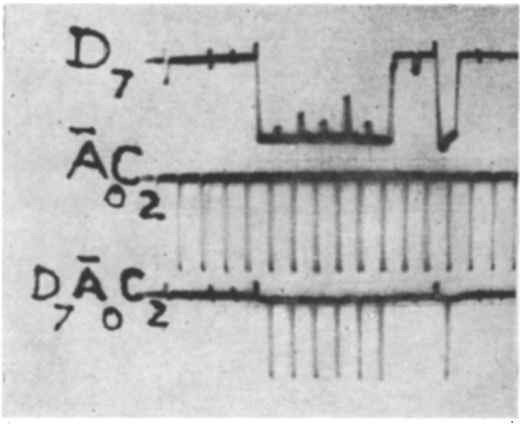

FIG. 5. Actual waveforms at the input and output of the ANO Gate of Fig. 4 showing the generation of the digit pulses for D_7.