

A Front end Switched Rectifier DC Source for Neutral Point Balancing of A NPC Three-Level Inverter for The Full Modulation Range

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Abstract- A switched DC voltage three level NPC is proposed in this paper to eliminate capacitor balancing problems in conventional three-level Neutral Point Clamped (NPC) inverter. The proposed configuration requires only one DC link with a voltage $V_{dc}/2$, where V_{dc} is the DC link voltage in a conventional NPC inverter. To get rated DC link voltage (V_{dc}), the voltage source is alternately connected in parallel to one of the two series capacitors using two switches and two diodes with device voltage rating of $V_{dc}/2$. The frequency at which the voltage source is switched is independent and will not affect the operation of NPC inverter. The switched voltage source in this configuration balances the capacitors automatically. The proposed configuration can also be used as a conventional two level inverter in lower modulation range, thereby increases the reliability of the drive system. A space vector based PWM scheme is used to verify this proposed topology.

I. INTRODUCTION

Multilevel inverters are becoming popular for high power industrial drives. The major advantages of multilevel inverters are improved harmonic performance, reduced stress on the switches and reduced electromagnetic interference (EMI) emission. Various multi-level inverter topologies were proposed in [1-9]. Three level NPC inverter is proposed [1] by Nabae et al. for the first time. But the NPC inverter has a major disadvantage that there will be voltage unbalance in DC-Capacitors. The H-bridge topology proposed in reference [2, 3] does not have the voltage unbalance problem, but it requires three isolated DC power supplies. The open-end winding induction motor drive topology proposed in [4] and cascading two two-level inverters topology proposed in [5] eliminate this problem but require two power supplies. Dual two-level inverter scheme for an open-end winding induction motor drive with a single DC power supply is proposed in [6] but it requires four extra four-quadrant switches. A modification of the conventional NPC inverter is suggested in [7], in which a capacitor is added across the neutral clamping diodes to ensure dynamic balancing of the DC-bus capacitors. But this method does not eliminate the neutral-point fluctuations completely. A generalized multi-level inverter topology suggested in [8]. But this topology requires individual capacitor banks for each phase. Three level PWM Switched voltage source Inverter proposed in [9], requires one extra capacitor bank for each phase and the modulation index is restricted by the inductance value. In [11] a DC link voltage balancing is proposed using dc-dc converter technology on the DC link side. This needs

extra inductors and components, making the power bus assembly, very complicated. A DC link capacitor balancing using PWM based virtual vectors is reported in [12]. But the modulating signal generation in all the modulation range and the PWM control with DC link balancing in the over modulation region is not properly addressed. The DC link balancing for diode clamped inverter is possible, for all the modulation range, with back-to-back inverter structure [13]. But this will increase the power circuit complexity and the cost. The redundant two-level inverter structure present in the conventional NPC-three-level inverter is effectively utilised for DC link capacitor balancing in [14], in the lower modulation range. But the neutral point balancing with DC link voltage control, is not addressed for the higher modulation ranges in [14].

In this paper, a power circuit configuration of switched rectifier voltage source for a NPC three-level inverter is proposed. The DC link Voltage required is half compared to the conventional NPC inverter. In the lower modulation ($M < 0.433$) range NPC inverter can be operated as a two level inverter, by clamping the voltage source across the bottom capacitor or to the top capacitor. This will also increase the reliability of the drive system, and also the capacitor balancing problem in lower modulation indices, without resorting to redundant switching state selection, in PWM control. In the higher modulation range the voltage fluctuations of the neutral point are eliminated by switching the voltage source between two capacitors. Only two switches and two diodes are required additionally for achieving this. The switching of the voltage source between the two capacitors will not affect the operation of the NPC inverter.

II. CONVENTIONAL THREE-LEVEL NPC INVERTER

The conventional three-level NPC inverter shown in Fig.1 has 27 switching states, and the switching states are presented in Fig.2. These 27 switching states are classified into three groups A, B and C, as shown in Table I. When switching states in Group A are used in a three level NPC inverter, the load is connected between terminal P and N or to either one. In this case, the current through the capacitors will be equal and there will not be any voltage unbalance problems, in capacitors (C1 and C2, Fig.1). When switching states in Group-B are used for

inverter control, the neutral point is connected along with the terminals P and N to the output load. So the currents flowing through the capacitors will be different and causes voltage unbalance. When switching states in Group-C are used the load is connected between the terminal P and the neutral point or terminal N and the neutral point. Here the capacitor currents are equal, but the flow is in opposite direction. In this condition, when one capacitor charges, the other capacitor discharges at the same rate. This can lead to unbalance in voltage across the capacitors C1 and C2.

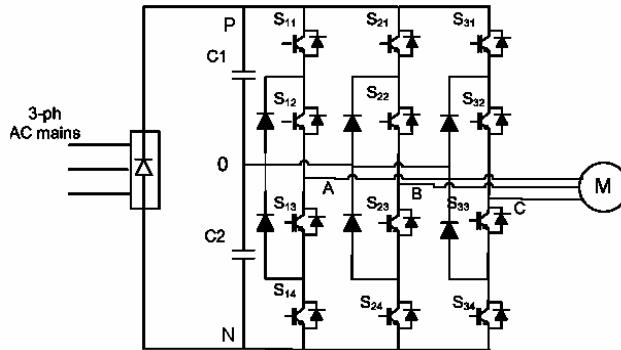


Fig.1. conventional three-level NPC inverter

TABLE I

SWITCHING STATES GROUPS BASED ON THE DC CAPACITOR CHARGING AND DISCHARGING

Group-A	000, ---, +++, +-- , ++-, -+-, -++ , --+, +-+
Group-B	+0-, 0+-, -+0, -0+, 0-+, +0-
Group-C	00+, 0+0, 0++ , +0+, +00, ++0, 0--, 00-, -0-, -00, --0, 0-0

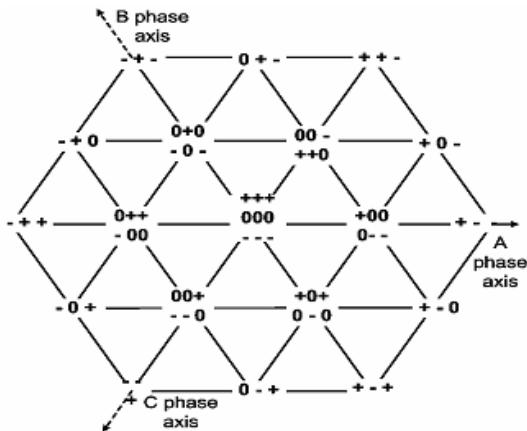


Fig.2. Space-vector combinations for three level NPC

III. PROPOSED SWITCHED VOLTAGE SOURCE THREE LEVEL NPC INVERTER

Fig.3. shows the proposed switched voltage source three level NPC inverter configuration. In the proposed topology,

only one active voltage source of $V_{dc}/2$ is used. The rated DC link voltage can be obtained by switching the voltage source ($V_{dc}/2$) between the top (C1) and bottom (C2) capacitors with a duty ratio of 0.5. Capacitors are charging to $V_{dc}/2$ with a constant frequency irrespective of the load currents. So the load current flowing through the capacitors will not create any neutral point fluctuations. Here the diode bridge rectifier and filter capacitor (C3) is used as an input voltage source. To switch the voltage source between the capacitors C1 and C2, extra two switches and two diodes are required, as shown in the Fig.3. The ratings of these devices are also, $V_{dc}/2$ as in the case of the NPC inverter switches of Fig.1

From Fig.3 it can be seen that when the switch S1 is ON, the voltage difference between the source and capacitor C1 will make the diode D1 forward biased, and connects the voltage source in parallel to the capacitor C1 as shown in Fig. 4(a). The voltage across the S2 and D2 is $V_{dc}/2$. When the switch S2 is turned ON, the voltage difference between the source and capacitor C2 will make the diode D2 forward biased, and connects the voltage source in parallel to the capacitor C2, as shown in Fig.4(b). In both the cases, the capacitor C3 is parallel to C1 or C2, so a low value of capacitor for C3 will not alter the original C1 and C2 values of the NPC inverter of Fig.1. In the present study 220 μ F is used for C3 and 2200 μ F is used for C1 and C2.

In the proposed topology extra switches are used to maintain the rated DC link voltage across the two capacitors. These extra switches and the capacitor C3 will not affect the inverter switching operation. So the inverter can be operated like a conventional three level NPC inverter.

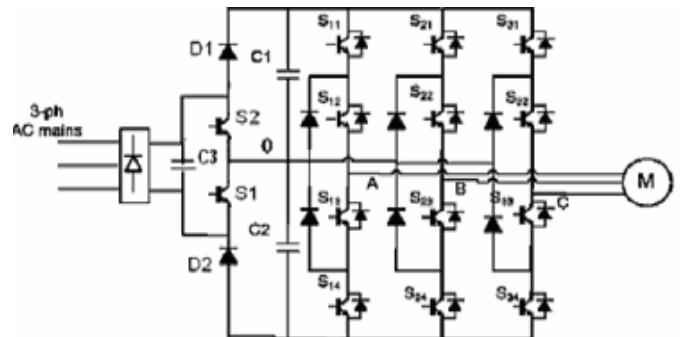


Fig.3. proposed Switched Voltage Source Three level NPC Inverter

IV. THE DC LINK VOLTAGE CONTROL

For the modulation index less than 0.433 the reference voltage space vector will be in the inner hexagon (Fig.2) and it indicates that the inverter will switch with the switching states shown in the group-C, as shown in Table-1 and the zero switching states. In this operating region, for the conventional NPC, the capacitor balancing problem is serious. Here, one capacitor (either the top or the bottom depending on the active inverter switching state) will be discharging with the full load current, and the other gets charged. This can lead to large

neutral point fluctuations. This problem is completely eliminated in the proposed topology by operating NPC as a two-level inverter. By switching on S2 the voltage source will be parallel to the capacitor C2 (Fig.4 (b)) for the active inverter switching states, 0--, 00-, -0-, -00, --0, and 0-0. the zero states will not contribute to the DC link capacitor voltage fluctuations. Similarly by selecting the redundant states (+00, ++0, 0+0, 0++00+), the upper inverter with the DC link capacitor C1 can also be used as conventional two-level inverter.

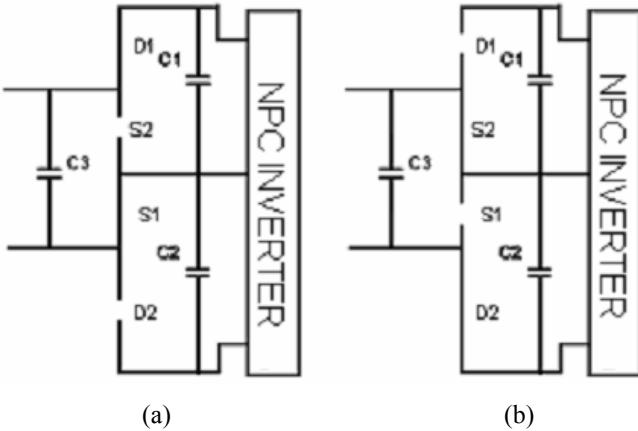


Fig.4.(a) Source capacitor C3 is parallel to the Capacitor C1 when S1 is ON. (b). Source capacitor C3 is parallel to the capacitor C2 when S2 is ON

For the modulation index more than 0.433 the reference space vector will cross the inner hexagon and the inverter has to operate as a three level inverter. The rated DC link voltage across the NPC inverter can be maintained by switching the Switches S₁ and S₂ at constant frequency with a duty ratio of 0.5 as mentioned earlier. The minimum switching frequency (f_s) of the switches S₁ and S₂ for an 'n' pulse rectifier can be determined as follows.

$$f_{sw} = N * ((n * f_1)/2) \quad \text{----- (1)}$$

Where

f_{sw} = Switching frequency of extra switches

f₁ = Supply frequency

N = odd integer

Taking the supply frequency of 50Hz, for a six pulse rectifier the minimum switching frequency of the extra switches (S₁ and S₂) is 150Hz (N=1 in eqn (1)). From the Fig. 5(a) it can be observed that the capacitor (C₁ or C₂) is connected to the diode bridge rectifier in alternate peaks, so that each capacitor will charge to the peak value of the input voltage. Loss of synchronisation between the gating pulses and the diode bridge rectifier output will not cause any serious problem because of the symmetry.

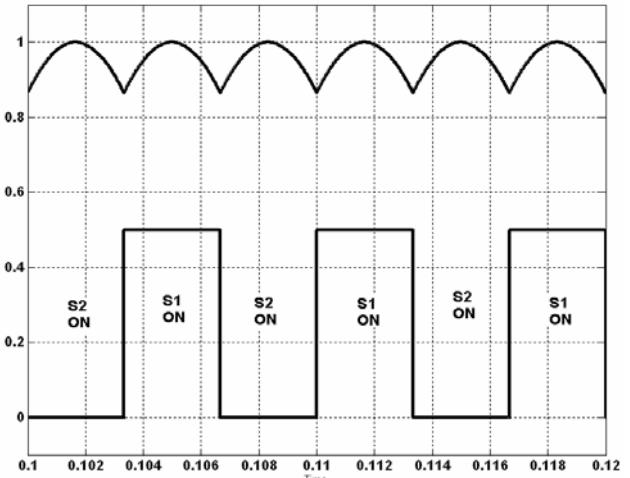


Fig.5 (a): Top trace is output voltage of the diode bridge rectifier and bottom trace is gating pulse of the extra switch S₁ (Scale X axis: 2ms/div).

If N is 2 (even integer) the capacitors C₁ and C₂ will charge unequally. From the Fig.5 (b) it can be observed that one of the capacitor is always connected to the diode bridge rectifier, during the input ripple peak. So one capacitor will charge to the input peak value and other capacitor will charge to less than the peak value. This will result in constant voltage difference between the two capacitors C₁ and C₂.

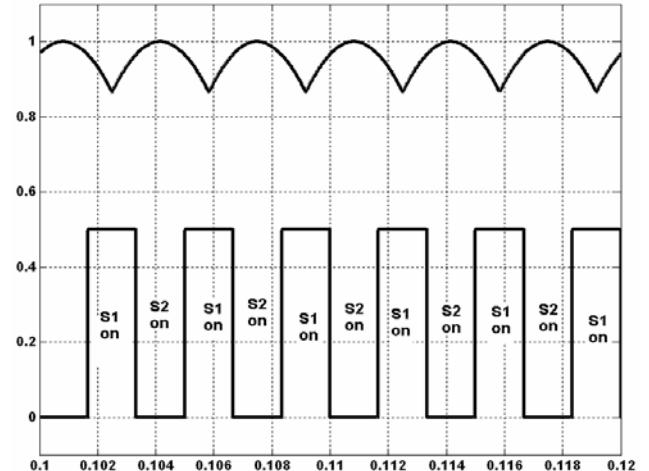


Fig.5 (b): Top trace is output voltage of the diode bridge rectifier and bottom trace is gating pulse of the extra switch S₁ X axis: 2ms/div, f_{sw}=300Hz

When the input DC source is switched between C₁ and C₂, using the switches S₁ and S₂, there can be sudden interruption of the rectifier current due to the dead time between S₁ and S₂ (typically 5μsec). During this period the capacitor C₃ is provided to give the current path to take care of the leakage inductance due to the front end rectifier transformer and due to line inductance. The value of the capacitor C₃ will be low, compared to C₁ and C₂, because the dead time is small, and can be approximately determined from (2).

$$C = \frac{(i^* \Delta T)}{\Delta V} \quad \text{----- (2)}$$

Where

i = rectifier output current

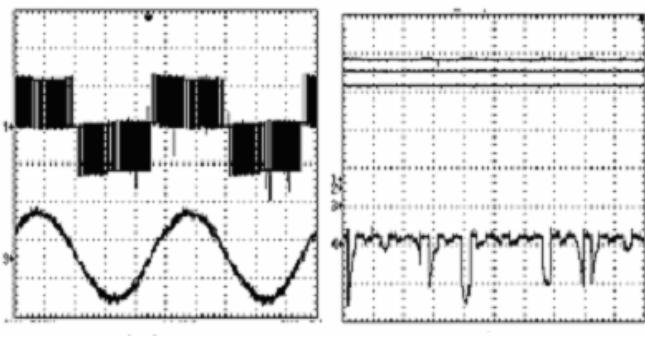
ΔT = Dead time between the switches S1 and S2

ΔV = voltage ripple in capacitor C_3 (typically 5% of V_{dc})

V. EXPERIMENTAL RESULTS

The proposed topology is experimentally verified on a 1KW three phase induction motor drive. It is tested for the entire speed range by using V/f control. Space vector PWM scheme [10] is used to generate the switching pulses for the three level NPC inverter. The inverter switching frequency is 1 KHz and the switches S1 and S2 used for DC link voltage control are switched at a constant frequency of 750Hz. The value of capacitor C3 is $220\mu F$. the gating signals are generated using TMS320 F 2812 DSP and GAL22V10B platforms.

The experimental results for modulation index 0.4 (i.e. 20Hz operation) are presented in Fig.6. Fig.6 (a) shows Pole voltage and Phase current. Fig.6(b) shows (upper trace) the three capacitor (C_1 , C_2 and C_3) voltages and the charging current of C_1 from the switched rectifier. Here the inverter is operated as a conventional NPC three level inverter. It can be observed from Fig.6(b) that the proposed switched rectifier is capable of maintaining the DC link capacitor balance. It can also be noted that the C_1 capacitor charging current pulses (bottom trace Fig.6 (b)) are of unequal amplitudes due to the front end rectifier switching with 750Hz. But, in lower modulation indices, by appropriately clamping the DC source to C_1 or C_2 , depending on the inverter switching state, the capacitor charging current will be similar to that of a front rectifier charging the output DC capacitor, similar to that of a diode bridge rectifier charging the DC link capacitor. Fig.6(c) shows the phase voltage, voltage across the switch S_1 , phase current and the charging current C_1 through the switch S_2 from top to bottom trace. From the waveform it can be observed that the front end rectifier switches (S_1 and S_2) are switching



(a) (b)
Fig.6(a)Top trace is Pole voltage and bottom trace is phase current at $M=0.4$ [X-axis 10 ms/div Y-axis 50 V/div and 0.3A/div]. (b) Top three traces are Capacitor Voltages and bottom trace is Switched rectifier current to $C1$ [X- axis 2.5 ms/div, Y-axis 20V/div and 1A/div].

at 750 Hz for charging the NPC DC link capacitors. As mentioned before, the present scheme is also run as a conventional two-level inverter in lower modulation indices, by clamping the rectifier across C2 of the NPC three-level inverter and appropriate switching states are only used for the present operation. The phase voltage, pole voltage, line voltage and phase current are presented in fig.6 (d). This two level operation will completely eliminate the capacitor balancing problem (neutral point voltage fluctuations), in lower modulation indices.

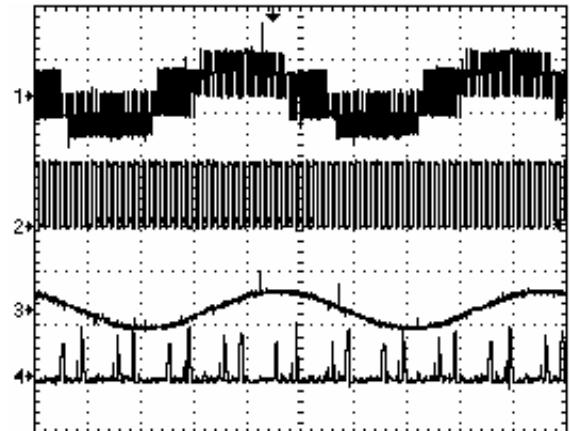


Fig. 6(c) Top trace is phase voltage, Second trace is voltage across the switch S1, Third trace is phase current and bottom trace is Switched rectifier current to C1 at $M=0.4$. [X-axis 10 ms/div, Y-axis 50V/div and 1A/div].

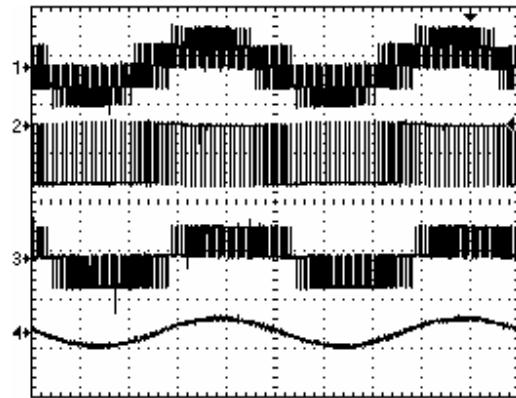


Fig. 6(d) Top trace is phase voltage (V_{an}) [Y-axis 50V/div], second trace is Pole voltage(V_{ao}) [Y-axis 50V/div], third trace is line voltage (V_{ab})[Y-axis 100V/div] and bottom trace is Phase current [Y-axis 1A/div and X-axis 10ms/div]

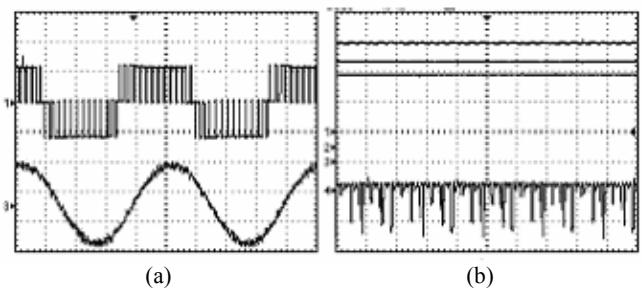


Fig.7(a) Top trace is pole voltage and bottom trace is phase current at $M=0.8$ [X-axis 10 ms/div Y-axis 50 V/div and 0.3A/div]. (b) Capacitor Voltages and Switch current [X- axis 10ms/div, Y-axis 20V/div and 1A/div].

The pole voltage and phase current for modulation index 0.8 (i.e. 40Hz operation) are presented in Fig. 7(a). The capacitor voltages and switch currents are presented in Fig.7(b). Fig.7(c) shows the phase voltage, voltage across the switch S₁, phase current and Switch (S₁) current.

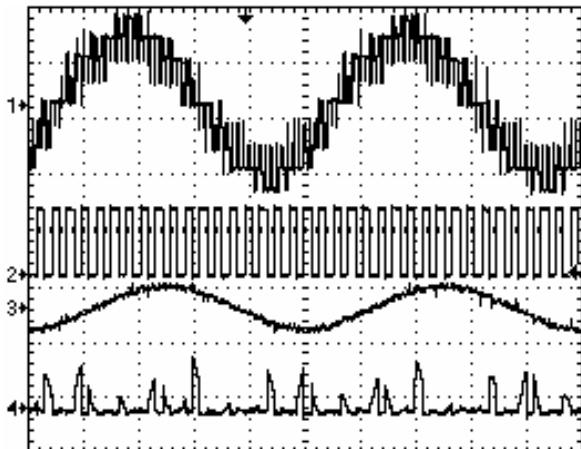


Fig. 7(c) Top trace is phase voltage, second trace is voltage across the input switch, third trace is phase current and bottom trace is Switch current at M=0.8. [X-axis 5 ms/div, Y-axis 50V/div, 1A/div (third trace) and 2A/div(fourth trace)].

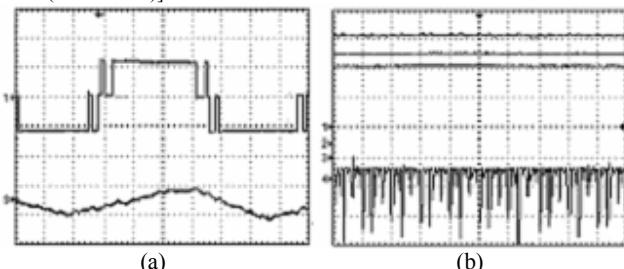


Fig.8(a) Top trace is pole voltage and bottom trace is phase current at M= 1.15 [X-axis 2.5 ms/div Y-axis 50 V/div and 1A/div]. (b) Top three traces are capacitor voltages and bottom trace is switch (S₁) current [X- axis 10 ms/div, Y-axis 20V/div and 1A/div].

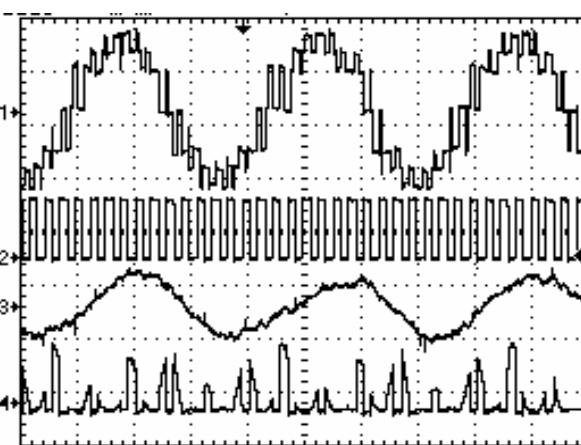


Fig. 8(c) Top trace is phase voltage, second trace is voltage across the switch (S₂), Third trace is phase current and bottom trace is switch (S₁) current at M=1.15. [X-axis:10ms/div, Y-axis: 50V/div and 1A/div (third trace), 2A/div (bottom trace)].

The pole voltage and phase current for modulation index 1.15 (i.e. over modulation) are presented in Fig. 8(a). The capacitor voltages and switch currents are presented in Fig.8 (b). Fig.8(c) shows the phase voltage, voltage across the switch S₁, phase current and Switch (S₁) current. All these experimental results show that the present switched DC link structure can effectively balance the DC link voltage of a conventional NPC inverter with additional conventional two-level inverter like operation and thereby increase the efficiency and reliability of the drive system in the lower modulation indices. Fig. 9 to Fig. 11 shows the transient performance of the proposed drive topology. Fig.9. shows the phase voltage and phase current when speed command is accelerating from 20Hz to 40Hz operation. Here the inverter is operated as a NPC three level inverter in the entire period of acceleration. From the oscillograms, it can be observed that in transients the load current increased by 5 to 6 times with very good DC link voltage control.

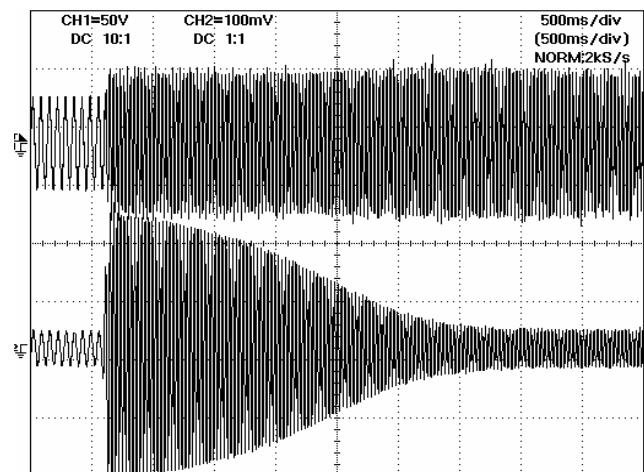


Fig.9.Top trace is phase voltage and bottom trace is phase current during the acceleration from 20Hz to 40Hz [X-axis 500ms/div, Y-axis 50V/div and 2A/div]

Fig. 10 shows the pole voltage and phase current of the inverter when the speed command is accelerating from 15Hz to 30Hz. Here the inverter is operated as a conventional two level inverter in lower modulation indices (<0.43) and as NPC three level inverter in higher modulation indices (>0.43), with sudden acceleration. In Fig.10 for modulation index from 0.3 to 0.433, the drive scheme is operated as a conventional two level inverter and from modulation index from 0.43 to 0.6 it is operated as a three level inverter, with correct DC link voltage control

Fig. 11 shows the voltage across the capacitor (C2) and the phase current during the sudden acceleration from 20Hz to 40Hz.

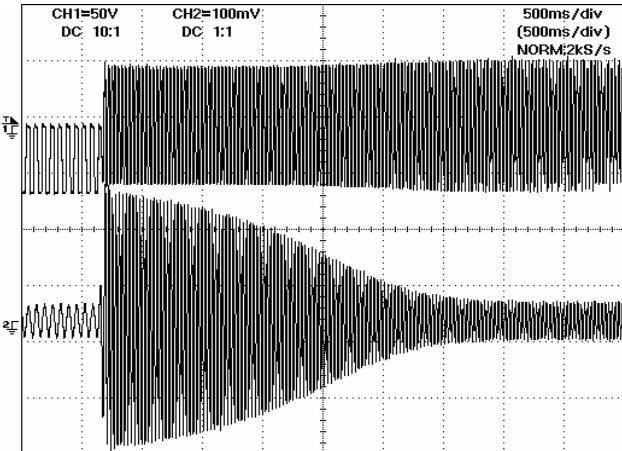


Fig.10. Top trace is pole voltage and bottom trace is phase current during the acceleration form 15Hz to 30Hz [X-axis 500ms/div, Y-axis 50V/div and 2A/div]

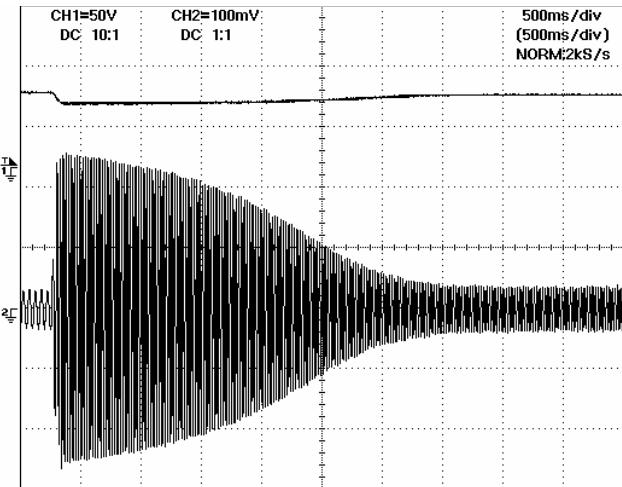


Fig.11. top trace is capacitor voltage and bottom trace is phase current during the acceleration form 20Hz to 40Hz [X-axis 500ms/div, Y-axis 50V/div and 2A/div]

VI. CONCLUSIONS

In the proposed topology the voltage fluctuations of the neutral point of a conventional NPC three level inverter fed drive are avoided by switching the voltage source between two capacitors at constant frequency independent of NPC inverter operation. This configuration can be operated as a two level inverter or as a three level inverter in lower modulation indices (<0.43). The voltage fluctuations of neutral point in lower modulation indices can be completely eliminated by operating as a two level inverter.

The DC link Voltage required is half compared to the conventional three level NPC inverter. The voltage rating of all the devices used in proposed topology is equal to the source voltage (i.e. $V_{dc}/2$).

This configuration needs only one power supply compared to an H-bridge topology and other cascaded two-level inverters topologies. The proposed switched DC link topology is experimentally verified for the full modulation range, on a 1KW Induction motor drive, for steady state as well as in the transient operation, with very good control of the DC link voltage. This can also be extended further to diode clamped inverters of level more than three.

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