# Electrical and Reliability Studies of "Wet $N_2O$" Tunnel Oxides Grown on Silicon for Flash Memory Applications

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***Abstract*—In this paper, we report the electrical characteristics and reliability studies on tunnel oxides fabricated by "wet $N_2O$" oxidation of silicon in an ambient of water vapor and $N_2O$ at a furnace temperature of 800 °C. Tunnel oxides that have an equivalent oxide thickness of 67 Å are subjected to a constant-current stress (CCS) amount of $-100$ mA/cm$^2$ using a MOS capacitor to obtain information on stress-induced leakage current (SILC), interface, and bulk trap generation. The obtained results clearly demonstrate the superior performance features of the present tunnel oxides with reduced SILC, lower trap generation, minimum change in gate voltage, and higher charge-to-breakdown during CCS studies. X-ray photoelectron spectroscopy depth profile studies of the tunnel oxide interfaces have shown that the improved performance characteristics and reliability can be attributed to the incorporation of about 8.5% nitrogen at the oxide–silicon interface of the samples formed by the "wet $N_2O$" process that involves low-temperature oxidation and annealing at 800 °C.**

***Index Terms*—Charge-to-breakdown, interface traps, stress-induced leakage current (SILC), wet $N_2O$ oxidation.**

## I. Introduction

The recent aggressive scaling of Flash memory devices and the subsequent increase in functionality per chip require robust and reliable tunnel oxides for continued scaling. According to the International Technology Roadmap for Semiconductors (ITRS) 2005, the tunnel oxides of NAND Flash memory cells will have a thickness of 6–7 nm by the end of this decade [1]. The use of conventional dry oxide as the tunnel oxides in Flash memory devices has not shown favorable results at reduced thickness due to severe stress-induced leakage current (SILC) [2]–[4] and increase in traps during stress reliability studies. As a result, various nitridation technologies have emerged to achieve better immunity to trap generation during electrostatic stress and reduce the SILC [5], [6] compared to conventional dry oxides. Historically, ammonia ($NH_3$) was the first approach used for nitridation of tunnel oxides [7], [8]. However, it was found that $NH_3$ nitridation introduces large amounts of hydrogen at the interface, which gives rise to electron traps and, hence, the deterioration of the device performance [9]–[11]. It was reported that the nitridation in pure nitrous oxide ($N_2O$) or the reoxidation of thermal oxide in $N_2O$ at high temperatures would provide tunnel oxides of better quality and reliability [12]. However, as controlling the oxide thickness was difficult in a high-temperature process due to the high growth rate, it was necessary to carry out low-temperature thermal oxidation in pure $N_2O$. Nevertheless, it has been shown that the low-temperature nitridation in $N_2O$ does not introduce any significant nitrogen [13] into the tunnel oxide. Recently, it has been reported that the nitridation of wet or dry oxides in nitric oxide (NO) [14]–[17] provides good immunity to trap buildup, good interface, and high charge-to-breakdown ($Q_{\mathrm{bd}}$).

We have recently shown that tunnel oxides of excellent quality and thickness control can be achieved by a process called "wet $N_2O$" oxidation at a temperature of 800 °C in a furnace oxidation process [18]. In this paper, we address the reliability studies of this "wet $N_2O$" oxide of thickness 6–7 nm. The tunnel oxides are studied using MOS capacitor test structures with heavily doped n-type polysilicon gate. The obtained results are compared with the data reported in the literature for other nitridation processes. We also show from the X-ray photoelectron spectroscopy (XPS) studies that with this new process of tunnel oxide growth at 800 °C in a "wet $N_2O$" ambient, followed by $N_2O$ annealing, a maximum concentration of 8.5% nitrogen can be introduced at the interface to enhance the reliability of the tunnel oxide. The results demonstrate that the MOS capacitors fabricated with this oxide show excellent reliability in terms of lowest value of SILC, highest charge-to-breakdown, and minimum saturated values of electron and hole trap generation during the stress studies.

## II. Wet $N_2O$ Oxidation Process and MOS Capacitor Fabrication

MOS capacitors, whose structure is shown in Fig. 1, were fabricated using the "wet $N_2O$" process for growing the gate tunnel oxide. A field plate structure is used to overcome the edge effects. The starting silicon wafer is p-type (100), which has a resistivity of 0.1–0.2 $\Omega \cdot$ cm. The silicon active surfaces were prepared by standard RCA1 and RCA2 procedures, followed by a dilute hydrofluoric acid (HF) dip to remove the native oxide. A thick field oxide that has a thickness of about 0.5 $\mu$m is first grown by the conventional dry–wet–dry oxidation process at 1000 °C, and a window is opened in this oxide

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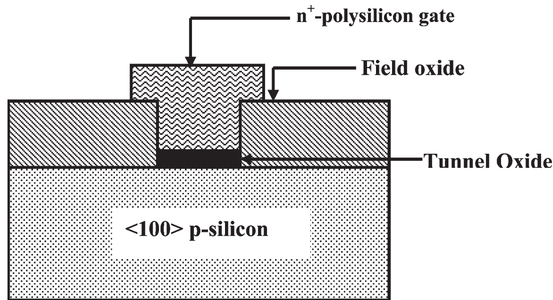


Fig. 1. Cross section of the MOS capacitor structure having an area of $2.83 \times 10^{-5}$ cm$^{-2}$.

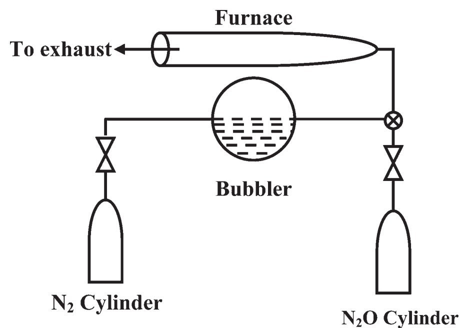


Fig. 2. Schematic diagram of the "wet $N_2O$ oxide" process set up.

using a single-mask lithographic process to define the active region for tunnel oxide growth. In this "wet $N_2O$" process, the oxidation of silicon is carried out at 800 °C in an ambient of low partial pressure of water vapor and $N_2O$ by bubbling $N_2$ through water in a quartz bubbler maintained at 80 °C and simultaneously passing $N_2O$ directly to the furnace, as shown in Fig. 2. The details of the process and the oxide growth rates are presented in [18]. Excellent control on the oxidation growth rate is obtained due to the reduced vapor pressure achieved by keeping the bubbler temperature at 80 °C. The "wet $N_2O$" oxidation shows two distinct growth regions. Region I is up to an oxidation time of 15 min and has a growth rate of 2.52 Å/min, whereas Region II has an oxidation time that is beyond 15 min and a growth rate of 0.87 Å/min. This difference is attributed to the direct participation of $N_2O$ during the initial stages of oxidation. On the other hand, during the later stages of oxidation, the direct participation of $N_2O$ is less, compared to the water vapor present in the oxidation process. During this stage, the nitrogen incorporated during the initial phase retards the oxidation rate. The polysilicon gate electrodes that have a thickness of 0.5 $\mu$m were deposited by a low-pressure chemical vapor deposition process at 620 °C and subsequently doped using phosphorous from a $POCl_3$ source to achieve a sheet resistance of 30 Ω/□ in a furnace at a temperature of 950 °C for 20 min. After phosphorus diffusion, each sample is annealed at a temperature of 400 °C for about 20 min. The gate region was defined by lithography and wet etching of polysilicon, and the device area for this study was around 2830 $\mu$m$^2$. The equivalent oxide thickness is measured from the accumulation capacitance of the capacitance–voltage ($C$–$V$) measurement.

For the purpose of determining the impact of annealing ambient on the reliability of the tunnel oxide, the MOS structures

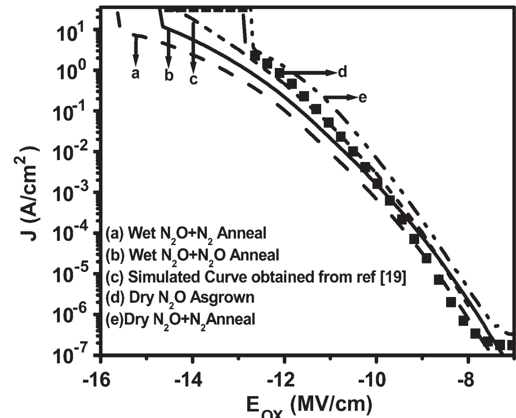


Fig. 3. $J$–$E$ plots of the "wet $N_2O$" tunnel oxides in the F–N tunneling region are shown along with the dry $N_2O$ oxides and the simulated curve obtained from [19].

shown in Fig. 1 were fabricated using tunnel oxides of thickness 67 Å grown by the "wet $N_2O$" process, which were annealed in $N_2$ in one set of devices and in $N_2O$ in another set. These samples were annealed at a furnace temperature of 800 °C for 30 min. Both sets of devices were characterized by measuring their current density $J$ versus electric field $E$ characteristics. The reliability studies were carried out by studying the SILC, the interface trap density buildup during constant-current stress (CCS), and the charge-to-breakdown.

## III. Characterization of Tunnel Oxides and Reliability Studies With CCS Applications

The tunnel oxides are characterized by the $C$–$V$ and current–voltage ($I$–$V$) characteristics of the MOS capacitors in the Fowler–Nordheim (F–N) tunneling region before and after subjecting to CCS. The relative concentration of nitrogen that is incorporated into the tunnel oxide is estimated through XPS studies to assess the performance and reliability of MOS structures that have this "wet $N_2O$" oxide as the tunnel gate dielectric material.

### A. *J–E Characteristics*

The $I$–$V$ characteristics of the MOS capacitors were measured using an HP 4155 B parameter analyzer in the accumulation region of the device. The voltage is converted into the electric field across the oxide as follows:

$$E_{\text{ox}} = \frac{V_g - V_{\text{FB}}}{t_{\text{ox}}} \tag{1}$$

where $V_g$ is the gate voltage, $V_{\text{FB}}$ is the flatband voltage determined from the $C$–$V$ characteristics, and $t_{\text{ox}}$ is the oxide thickness equal to 67 Å obtained from the accumulation capacitance. The $J$–$E$ plots obtained for the two cases, namely, wet $N_2O$ oxides annealed in $N_2$ and $N_2O$, respectively, are shown in Fig. 3 by the curves (a) and (b). The $J$–$E$ plots of the as-grown dry $N_2O$ oxide (curve "d") and $N_2$-annealed dry $N_2O$ oxide (curve "e") are also shown in Fig. 3 for the purpose of comparison. In the same figure, a simulated curve obtained, assuming a barrier height of 3.22 eV using the F–N tunneling

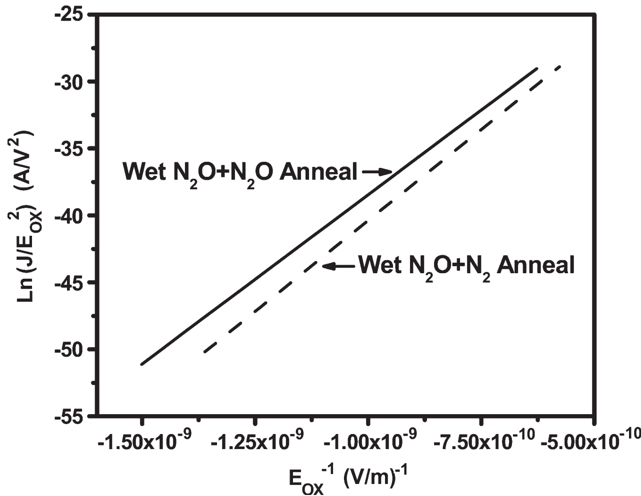


Fig. 4. F–N plot of the $N_2$- and $N_2O$-annealed “wet $N_2O$” tunnel oxides.

equation (2), as reported in the literature [19], is shown for comparison purposes. The dry $N_2O$ oxides have shown lower current density and field strength at the breakdown point (the point at which the current density shows a discontinuous jump) compared to the “wet $N_2O$” oxides. It can be seen in both cases of annealing that the MOS devices fabricated using the “wet $N_2O$” process show excellent F–N tunneling region over a wide range of current densities, ranging from $10^{-7}$ up to 10 A/cm$^2$, with the breakdown field strength well above 14 MV/cm. The tunnel oxide barrier heights in these devices are determined by considering the following expression for the current density in the F–N tunnel region:

$$J = AE_{\mathrm{ox}}^2 \, e^{\frac{-B}{E_{\mathrm{ox}}}} \tag{2}$$

where $A$ and $B$ are constants. This expression is rearranged and plotted as $\ln(J/E_{\mathrm{ox}}^2)$ versus $(1/E_{\mathrm{ox}})$, as shown in Fig. 4, for the $N_2$- and $N_2O$-annealed samples. Assuming the effective electron mass to be $0.46m_e$, where $m_e$ is the vacuum electronic mass, the barrier heights that were extracted from the slopes of these F–N plots are found to be equal to 3.26 and 3.08 eV for wet $N_2O$ samples annealed in $N_2$ and $N_2O$, respectively. The lower barrier height observed in the samples annealed in $N_2O$ is attributed to the incorporation of a higher percentage of nitrogen at the oxide–silicon interface compared to that in the nitrogen-annealed samples. This is confirmed from the results of XPS analysis of the tunnel oxides described below.

### B. XPS Studies on Tunnel Oxide

XPS is employed to understand the chemical nature of the interface formed and to relate it to their respective performance characteristics. Depth profiles of Si 2p, N 1s, and O 1s photoelectron peaks were obtained in terms of atomic composition and sputter time for the annealed “wet $N_2O$” oxide samples using a 4-keV $Ar^+$ ion sputter source, and the results are shown in Fig. 5(a) and (b) for $N_2$- and $N_2O$-annealed samples, respectively. In the case of the $N_2$-annealed sample, as shown in Fig. 5(a), the oxygen level monotonically decreases from 10 min and becomes negligible after about 40 min of sputtering. The decrease in oxygen gives rise to an increase in silicon content, as the oxide is eroded, and the substrate is being exposed with sputtering. The nitrogen signal appears after about 10 min of sputtering and increases up to about 45 min of sputtering before it declines to 0% after 60 min of sputtering.

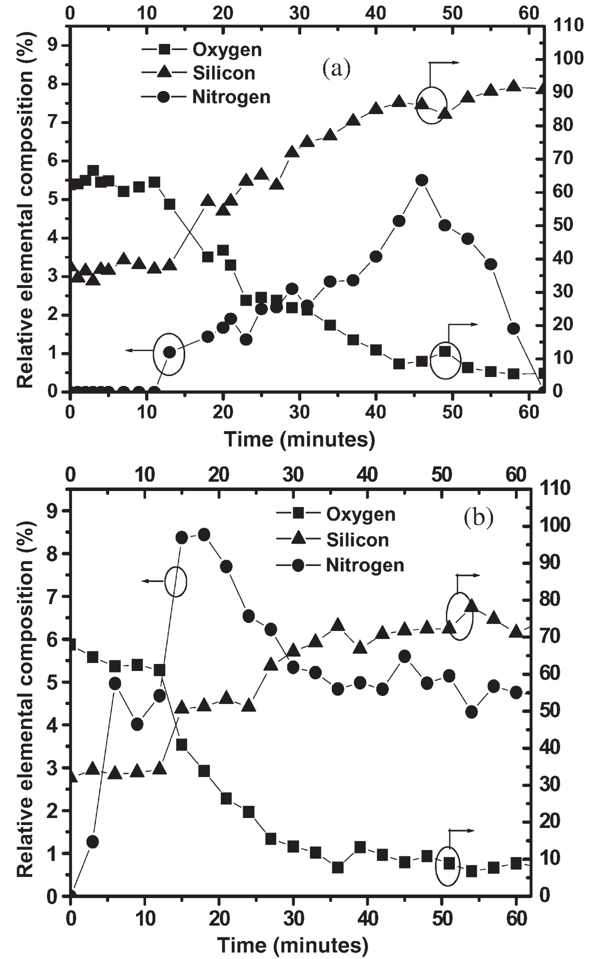


Fig. 5. XPS depth profiles of Si, O, and N in atomic % for the (a) $N_2$-annealed wet $N_2O$ oxide and (b) $N_2O$-annealed wet $N_2O$ oxide.

However, Fig. 5(b) shows a different depth profile, which was acquired for the $N_2O$-annealed tunnel oxide sample. Here, we clearly see that the nitrogen is incorporated at the interface itself. In fact, we see a peak in the 10- to 30-min interface region, where about 8.5 at.% of nitrogen is observed. For deeper regions, the nitrogen concentration is constant at about 5% into the depth of the substrate at least up to the 60-min sputtering time employed. In contrast to the $N_2$-annealed samples, a significantly higher nitrogen incorporation (approximately four times) at the interface is observed in the case of the tunnel oxide formed by annealing in $N_2O$. A detailed implication of these XPS results on the reliability and interface state density, charge-to-breakdown, etc., is addressed in Section IV.

### C. SILC Studies

SILC is one of the major reliability concerns in Flash memory devices. The prolonged operation of the devices

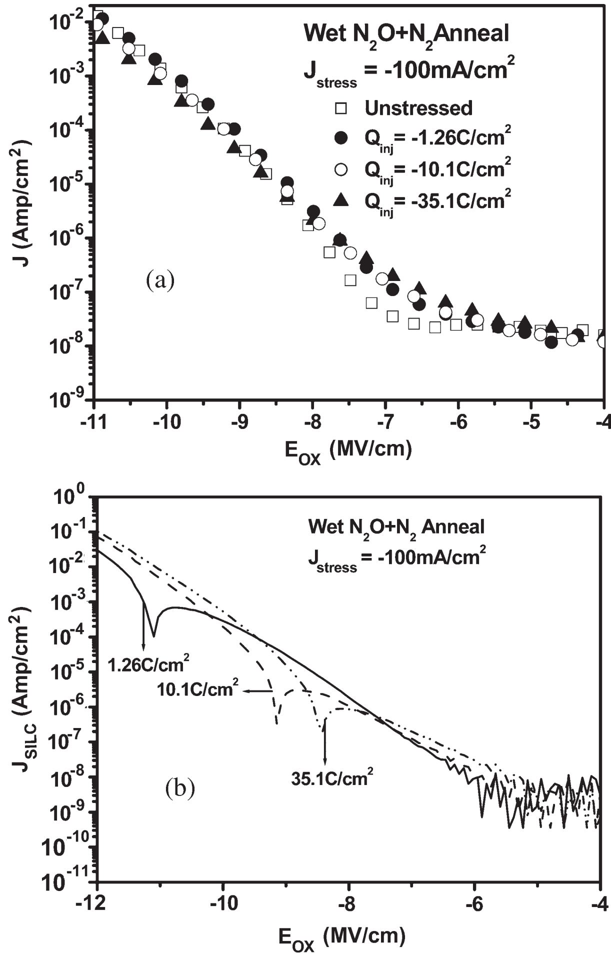


Fig. 6. (a) Leakage current obtained after F–N stress with different charge injection under a CCS of $-100$ mA/cm$^2$ is shown for the "wet $N_2O$" tunnel oxide annealed in $N_2$. (b) SILC for the above characterization conditions.

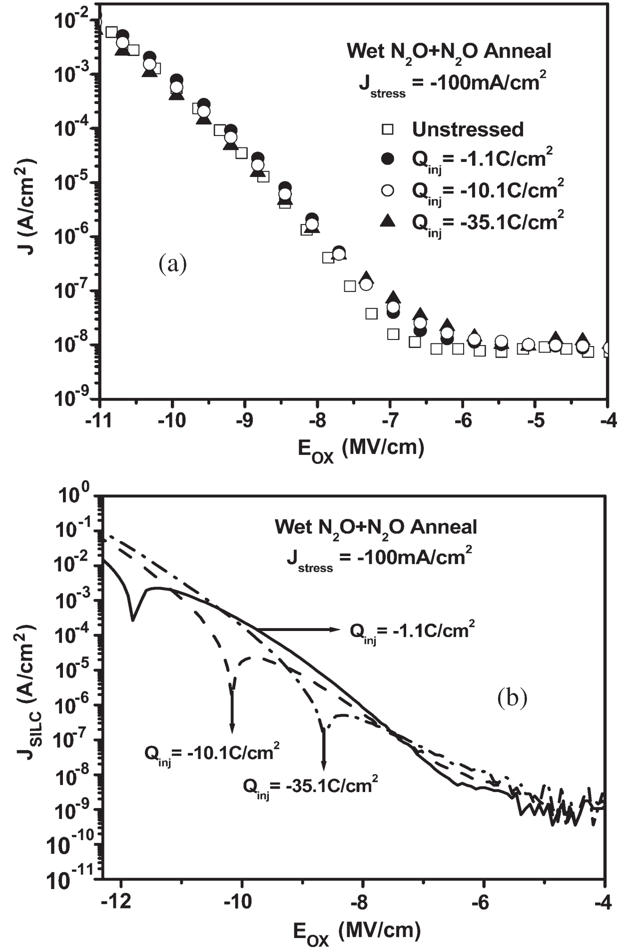


Fig. 7. (a) Leakage current obtained after F–N stress with different charge injection under a CCS of $-100$ mA/cm$^2$ is shown for the "wet $N_2O$" tunnel oxide annealed in $N_2O$. (b) SILC for the above characterization conditions.

accompanied by the frequent stressing of the tunnel oxides introduces a large amount of traps in the bulk and interface regions of the tunnel oxide, which results in significant SILC [20], [21]. The magnitude of the SILC increases with the stressing voltage or current level. During the past decades, considerable efforts have been expended to study the mechanisms for SILC [22]–[24]. The results have clearly shown that the presence of nitrogen at the interface of nitrided oxide and silicon improves the wear out properties and reduces the SILC. In this paper, the SILC is experimentally investigated for "wet $N_2O$" grown oxides annealed in $N_2$ and $N_2O$, respectively. Devices are stressed at a constant current density of $-100$ mA/cm$^2$ in the F–N region, and the corresponding magnitude of charge injected is computed. The $I$–$V$ characteristic is measured at the end of each charge injection step. Fig. 6(a) shows the $J$–$E$ curves for the MOS capacitor fabricated using a 67-Å gate oxide grown by "wet $N_2O$" oxidation process and annealed in $N_2$ for the four cases, namely unstressed, and stressed until the injected charge $Q_{\rm inj}$ is equal to $-1.26$, $-10.1$, and $-35.1$ C/cm$^2$. It can be seen in the figure that the low field leakage current increases from 24 to 110 nA/cm$^2$, which was measured at an oxide field of 6.5 MV/cm as the stress level goes up. However, with increasing electric field, the stressed $J$–$E$ curves cross the unstressed $J$–$E$ curve. This shift is due to the trapping of positive charges inside oxide, which modifies the F–N tunneling characteristics of the tunnel oxide. The SILC is defined as [25]

$$J_{\rm SILC} = J_{\rm ST} - J_{\rm UN} \quad (3)$$

where $J_{\rm ST}$ is the current density at any $E_{\rm ox}$ obtained from devices after subjecting them to CCS, and $J_{\rm UN}$ is the current density obtained at the same value of $E_{\rm ox}$ of the samples that were not subjected to prior stress. From the SILC plot, as shown in Fig. 6(b), it is observed that the SILC at lower fields (below 7 MV/cm) is higher in devices that were subjected to higher charge injection. It is also interesting to note that the SILC shows a turnaround as the absolute value of $E_{\rm ox}$ is increased. This is due to the onset of change in the F–N current and attributed to the increase in the formation of positively charged traps in the tunnel oxide when the applied field is increased. It can also be noticed from Fig. 6(b) that the turnaround point occurs at a lower electric field in the samples in which $Q_{\rm inj}$ was higher. The $J$–$E$ curves and SILC plots for "wet $N_2O$" oxide annealed in $N_2O$ show similar trends and are presented in Fig. 7(a) and (b). As before, the SILC curve shows a turnaround at higher field, and this point occurs at lower electric fields as

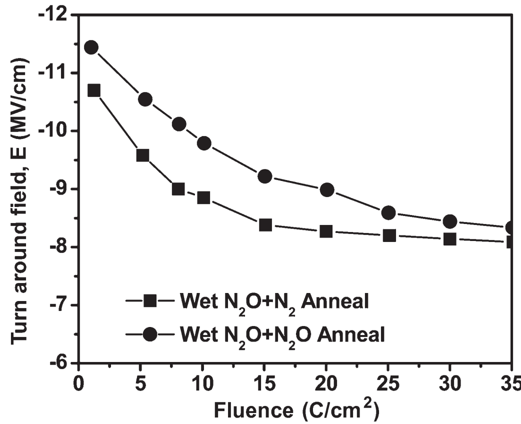


Fig. 8. Turnaround electric fields are shown as a function of injected fluence for "wet $N_2O$" tunnel oxides for the two cases of annealing in $N_2$ and $N_2O$, respectively.

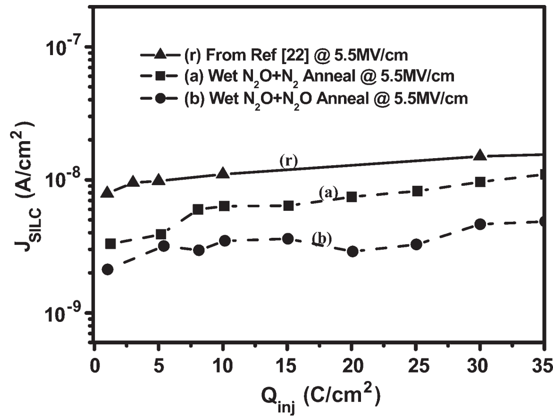


Fig. 9. SILCs measured at 5.5 MV/cm for various injections are plotted for "wet $N_2O$" tunnel oxides annealed in (a) $N_2$ and (b) $N_2O$. Curve (r) shows the results reported in the literature [22].

$Q_{\mathrm{inj}}$ is increased. A comparison of the nature of variation of the magnitude of the electric field at which the turnaround of the SILC curve occurs is shown in Fig. 8 for the two cases of annealing conditions. It can be observed from the figure that the shift in electric field is gradual in the $N_2O$-annealed tunnel oxide compared to that annealed in $N_2$. As shown in the following section, this is due to the lower generation rate of the positively charged traps in the "wet $N_2O$ oxide" when annealed in $N_2O$.

The SILC values at an electric field of $E_{\mathrm{ox}} = 5.5$ MV/cm on the present "wet $N_2O$" grown tunnel oxides annealed in $N_2$ and $N_2O$ are shown by the SILC curves in Fig. 9(a) and (b), respectively, and are plotted as a function of charge $Q_{\mathrm{inj}}$ injected by a CCS amount of $-100$ mA/cm$^2$ in the F–N region. For the purpose of comparison, the SILC results reported by Lai *et al.* [22] for a tunnel oxide of thickness 71 Å and measured at the same field of 5.5 MV are also plotted and shown as reference curve (r) in Fig. 9. It is interesting to note that the reference tunnel oxide was fabricated by growing the oxide by dry oxidation in $O_2$ ambient, followed by annealing in $N_2O$ at 950 °C, and that the device was stressed at 10 mA/cm$^2$ to measure the SILC. As compared to this reported result, the present "wet $N_2O$" grown oxides show considerably lower values of SILC, irrespective of the annealing ambient, in spite of stressing these devices at a much higher current density of $-100$ mA/cm$^2$. The "wet $N_2O$" tunnel oxide annealed in nitrogen shows a 43% SILC reduction compared to the reference oxide at a fluence of 20 C/cm$^2$, whereas the $N_2O$-annealed tunnel oxide shows a 76.6% SILC reduction compared to the reference. The improved SILC performance of the tunnel oxide fabricated in this paper is due to the strong interfacial silicon oxynitride bonding as a result of better incorporation of nitrogen into the tunnel oxide. It may also be noted that the SILC of the wet $N_2O$ oxide annealed in $N_2O$ is lower compared to that annealed in $N_2$. The $N_2O$-annealed tunnel oxide exhibits a 59% SILC reduction at a fluence of 20 C/cm$^2$ compared to the tunnel oxide annealed in nitrogen. The observed lower value of SILC is attributed to the lower trap generation rate in this oxide due to the incorporation of a higher atomic percentage of nitrogen into the tunnel oxide for the $N_2O$-annealed samples. This is further substantiated below from a detailed study of the generation of interface and oxide traps during CCS.

### D. Interface and Oxide Trapping Studies

The deterioration of the $SiO_2$–Si interface is a major reliability concern for the long-term operation of the device. An enhanced trap generation rate would lead to the reduction of transconductance and the subsequent failure of the oxide. The interface and bulk trap generation of the present "wet $N_2O$ oxides" are evaluated under a CCS amount of $-100$ mA/cm$^2$. The interface and bulk trap generation of the present "wet $N_2O$ oxides" are evaluated using the high-frequency $C$–$V$ (HFCV) measured at 100 kHz before and after subjecting the MOS capacitors to a CCS amount of $-100$ mA/cm$^2$ up to a certain value of injected charge. The interface state density distributions across the energy bandgap are extracted using Terman's method [26] using the following relation:

$$qD_{\mathrm{it}} = C_{\mathrm{ox}}\left(\frac{dV_g}{d\phi_s}\right) - C_s \tag{4}$$

where $D_{\mathrm{it}}$ is the interface state density, $C_{\mathrm{ox}}$ is the oxide capacitance, $dV_g/d\phi_s$ is the slope of the gate voltage $V_g$ versus surface potential $\phi_s$ curve, and $C_s$ is the depletion capacitance. The slope $dV_g/d\phi_s$ is extracted using the HFCV curve by converting the high-frequency capacitance value into the depletion capacitance using the following equation:

$$C_{\mathrm{HF}} = \frac{C_{\mathrm{ox}}C_s}{C_{\mathrm{ox}} + C_s}. \tag{5}$$

The interface state density distributions are given in Fig. 10 by the dotted lines (i.e., a1, a2, and a3) for "wet $N_2O$" oxides annealed in $N_2$. The solid lines (i.e., b1, b2, and b3) show the results obtained from the tunnel oxides annealed in $N_2O$. The curves a1 and b1 correspond to the unstressed device, and the curves a2 and b2 are the results obtained from two sets of devices after subjecting them to a stress of 5 C/cm$^2$. The curves a3 and b3 are the results obtained from devices that have been subjected to a stress of 20 C/cm$^2$. Fig. 10 shows that the minimum and midgap interface state densities are lower in the case of $N_2O$-annealed "wet $N_2O$ oxides" compared to the

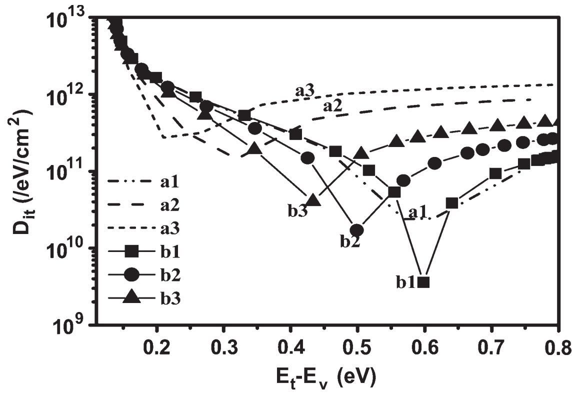


Fig. 10. Interface state density across the bandgap extracted using Terman's method for the $N_2$-annealed "wet $N_2O$" tunnel oxide (dotted lines a1, a2, and a3) and the $N_2O$-annealed "wet $N_2O$" tunnel oxides (solid lines b1, b2, and b3).

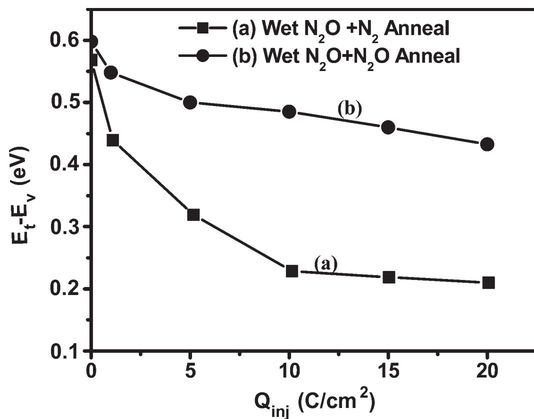


Fig. 11. Minimum interface trap density ($D_{it}$) position shown as a function of injected fluence for the "wet $N_2O$" tunnel oxides annealed in (a) $N_2$ and (b) $N_2O$.

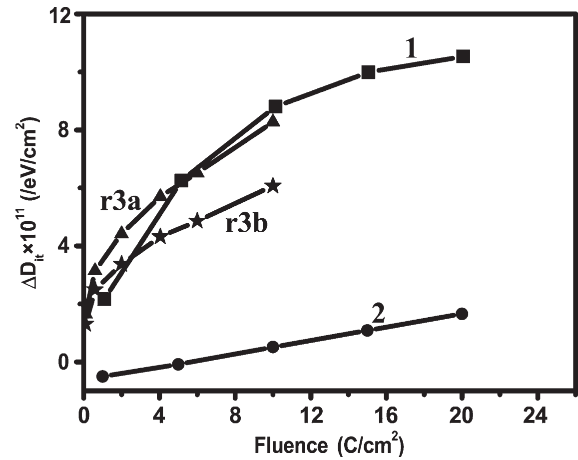


Fig. 12. Change in $D_{it}$ shown as a function of injected fluence for the "wet $N_2O$" tunnel oxides annealed in $N_2$ (curve "1") and $N_2O$ (curve "2"). The reference curves r3a (82-Å tunnel oxide grown in dry oxygen at 950 °C and annealed in NO) and r3b (74-Å tunnel oxide grown in $N_2O$ at 950 °C and annealed in NO) were reported in the literature [17].

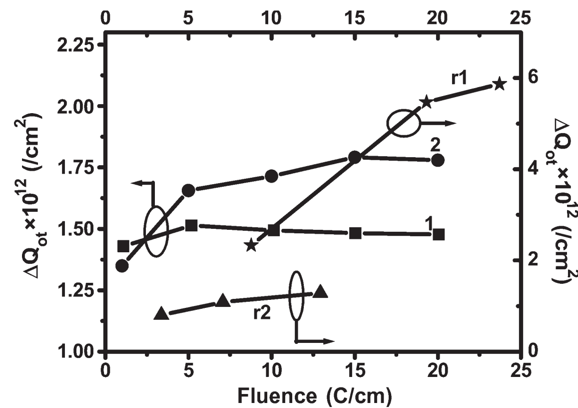


Fig. 13. Change in bulk oxide trap plotted as a function of injected fluence for the $N_2$-annealed "wet $N_2O$" tunnel oxide (curve "1") and the $N_2O$-annealed "wet $N_2O$" oxide (curve "2"). The reference curves r1 and r2 were reported in the literature [27].

$N_2$-annealed oxides for all the stress levels. It can also be noticed in the figure that, in both cases of the tunnel oxides, the minimum $D_{it}$ position shifts toward the valence band when subjected to CCS. To further ascertain this phenomenon, the position of the minimum $D_{it}$ ($E_t$) with respect to the valence band is estimated over the entire range of injection levels between 0 and 20 C/cm$^2$ by determining the energy position $E_t$ that gives the minimum value of $D_{it}$ for each fluence. The results are shown in Fig. 11 for the $N_2$- and $N_2O$-annealed "wet $N_2O$" oxides. This shift in $E_t$ toward the valence band at higher values of fluence indicates the generation of more acceptor-type interface states, which compensate the existing donor states near the valence band. Fig. 11 also shows that the shift of $E_t$ is considerably less in the oxide annealed in $N_2O$ compared to the $N_2$-annealed samples for identical stress conditions. This indicates that the acceptor trap generation rate for the $N_2O$-annealed "wet $N_2O$ oxides" is considerably lower and provides better interface stability during stressing.

For the purpose of ascertaining the usefulness of the present approach of "wet $N_2O$" oxidation, we compare in Fig. 12 the change in midgap interface state density $\Delta D_{it}$ of "wet $N_2O$" oxides annealed in $N_2$ (curve "1") and $N_2O$ (curve "2") with the results (curve r3a and r3b) reported in the literature [17]. Curve r3a represents the tunnel oxide of thickness 82, which was fabricated by "NO" annealing of dry oxide in a furnace at a temperature of 950 °C. Curve r3b represents the tunnel oxide having thickness of 74 Å and was fabricated by NO annealing of $N_2O$-grown oxide at 950 °C. The interface state densities for these tunnel oxides were evaluated under a CCS amount of $-10$ mA/cm$^2$, whereas in this paper, the interface state densities are evaluated under a CCS amount of $-100$ mA/cm$^2$. It can be seen in Fig. 12 that the change in midgap interface state density $\Delta D_{it}$ is lowest for the $N_2O$-annealed "wet $N_2O$" oxides throughout the range of stress levels. On the other hand, the $N_2$-annealed "wet $N_2O$" oxides (curve 1) initially show a lower $\Delta D_{it}$ and then gradually increases with stress, and at higher stresses, it becomes comparable with the reference oxides (r3a and r3b) that are obtained at $-10$ mA/cm$^2$ of the CCS compared to $-100$ mA/cm$^2$ in the present case. These comparisons demonstrate the superior features of the $N_2O$-annealed "wet $N_2O$" oxides.

The bulk oxide traps $Q_{ot}$ were extracted by noting the flatband voltage shift in the $C$–$V$ curve relative to the flatband voltage in the $C$–$V$ of the unstressed oxide. The HFCV is measured after a particular fluence injected by a CCS amount of $-100$ mA/cm$^2$. Fig. 13 shows the $\Delta Q_{ot}$ calculated for wet

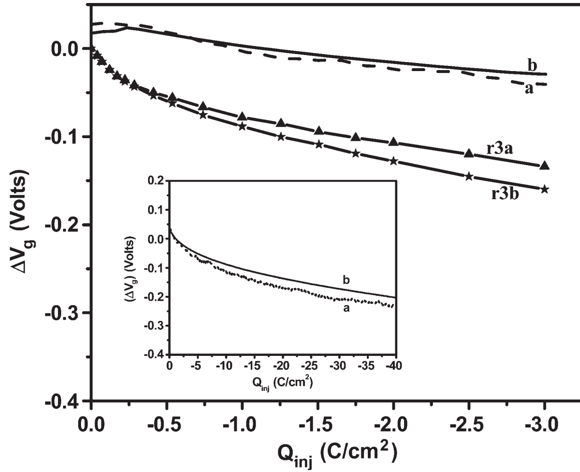


Fig. 14. Change in gate voltage during constant current stress shown as a function of injected fluence for "wet $N_2O$" tunnel oxides annealed in $N_2$ (curve "a") and $N_2O$ (curve "b"). The curves r3a and r3b show $\Delta V_g$ for similar fluences reported in the literature [17]. The inset shows the change up to $-40$ C/cm$^2$.

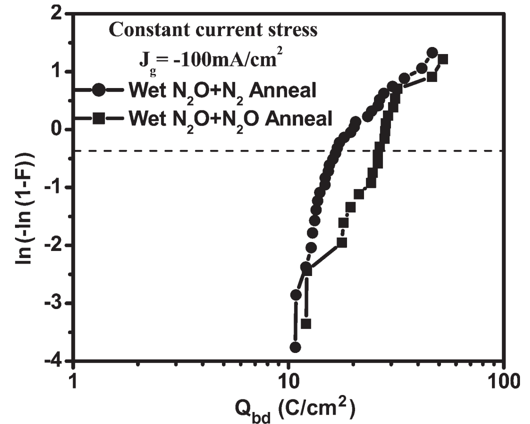


Fig. 15. Weibull plot of charge-to-breakdown obtained from constant current stress for "wet $N_2O$" oxides annealed in $N_2$ and $N_2O$.

$N_2O$ oxides annealed in $N_2$ (curve "1") and $N_2O$ (curve "2") along with the reference curves of conventional dry oxides of thickness 93 Å (curve "r1") and 56 Å (curve "r2") reported recently in the literature [27]. The curve "1" initially shows an increase in $\Delta Q_{\mathrm{ot}}$; however, at higher fluences, it shows a slight tendency to decrease in $\Delta Q_{\mathrm{ot}}$, which indicates electron trapping to a small extent in addition to hole trapping at very high fluences in the case of the "wet $N_2O$ oxide" annealed in $N_2$. On the other hand, in the case of curve "2," $\Delta Q_{\mathrm{ot}}$ increases slowly and saturates at high fluence levels. In comparison with the curve "r1," the present oxides show a minimum trapping and a saturated behavior, which shows superior reliability characteristics of the tunnel oxide grown by the "wet $N_2O$" process. On the other hand, the reference curves show a continuous increase in trapping as the fluence is increased. It may also be noted that the oxide thickness is lower in the case of curve "r2" and, hence, shows lower $\Delta Q_{\mathrm{ot}}$. However, curve "r2" also shows an increase in $\Delta Q_{\mathrm{ot}}$ as the fluence increased.

The oxide trapping is also monitored by the change in gate voltage during CCS. Fig. 14 shows the change in gate voltage for the "wet $N_2O$ oxide" annealed in $N_2$ (curve "a") and $N_2O$ (curve "b") as a function of time when stressed at a constant current of $-100$ mA/cm$^2$. Both oxides initially show a very slight positive shift in gate voltage, which indicates electron trapping to a marginal extent. It can be seen that as the injected fluence is increased further, the gate voltage shifts toward the negative side due to the generation of hole traps. However, it is important to note that the shift in gate voltage in the present tunnel oxides grown and annealed at 800 °C is very low compared to the results shown by the reference curves r3a and r3b reported in the literature [17] for the same fluences. The wet $N_2O$ oxide annealed in $N_2$ (curve "a") shows a $\Delta V_g$ of $-40$ mV and that annealed in $N_2O$ shows a $\Delta V_g$ of $-27$ mV for a fluence of up to $-3$ C/cm$^2$. On the other hand, the reference devices (curves r3a and r3b) that are grown, respectively, in $O_2$ and $N_2O$, followed with annealing in NO at a higher temperature of 950 °C, and stressed at a lower current density ($-10$ mA/cm$^2$) show a shift higher than $-100$ mV for an injected fluence of $-3$ C/cm$^2$. The inset in Fig. 14 shows the gate voltage change for our tunnel oxides until $-40$ C/cm$^2$, at which the $N_2$-annealed samples give rise to $\Delta V_g$ of $-230$ mV, whereas the $N_2O$-annealed samples show $-200$ mV.

### E. Charge-to-Breakdown ($Q_{\mathrm{bd}}$)

The charge-to-breakdown $Q_{\mathrm{bd}}$ is the measure of the quality of the oxides. In this paper, the charge-to-breakdown is measured during a CCS amount of $-100$ mA/cm$^2$. The charge-to-breakdown is plotted as a linearized two-parameter Weibull [28] plot, as shown Fig. 15. It can be seen in the figure that the mean value point (the point at which 50% of the devices have broken) for the wet $N_2O$ oxide annealed in $N_2O$ is 25 C/cm$^2$, whereas for those annealed in $N_2$ is 17 C/cm$^2$. This indicates that the wet $N_2O$ oxide annealed in $N_2O$ has a higher $Q_{\mathrm{bd}}$, and this is due to the better incorporation of nitrogen into the tunnel oxide.

## IV. Discussion

The improved performance of the "wet $N_2O$" oxides is attributed to the higher nitrogen incorporation into the tunnel oxides during the annealing steps. The oxide–silicon interface is defined as the point at which the oxygen level falls from its stoichiometric percentage to its half. However, the interface in this case seems to have a finite width. Based on this definition of the interface, the tunnel oxide formed by wet $N_2O$ oxidation, followed by nitrogen annealing [Fig. 5(a)], shows nearly 2.5 percentage of nitrogen at the interface, and the peak concentration of 5% is not exactly at the defined interface, which indicates that the interface region has a finite width. On the other hand, the $N_2O$-annealed "wet $N_2O$" grown oxide shows a peak interface nitrogen level of 8.5 at.%. In this case also, the nitrogen does not immediately decay to zero but extends further down, as reported in the literature. An examination of the results reported in the literature shows that such high concentration of nitrogen has not been achieved when the $N_2O$ annealing is carried out on tunnel oxides grown by wet oxidation process steps [15], [16]. The observation of N peak at different depths in the two cases [Fig. 5(a) and (b)] shows the bonding of N to Si in Fig. 5(a), and nitrogen seems to replace oxygen in Fig. 5(b), but within the interface itself, and is responsible for the enhanced

presence of nitrogen in Fig. 5(b) when the annealing is carried out in $N_2O$. However, the extension of N in Fig. 5(b) suggests that there could be incorporation of nitrogen into the wafer. Such extensions of nitrogen into silicon have, indeed, been reported in the literature [29].

The enhanced presence of nitrogen in the interface region of the present tunnel oxide grown in a combined atmosphere of controlled value of water vapor and $N_2O$ at 800 °C and annealed in $N_2O$ at 800 °C gives highly reliable results when compared to those reported in the literature. The higher percentage of nitrogen incorporated into the tunnel oxide leads to bond formation with silicon and possibly in the form of silicon oxynitrides. The bonds formed by the silicon oxynitrides require a higher energy to deform or for breaking compared to the silicon dioxide [21]. Therefore, the $N_2O$ annealing of "wet $N_2O$" oxides considerably improves the reliability. Although, at present, we do not have any conclusive evidence to prove that the enhanced quality of "wet $N_2O$" oxide is due to the bond-strengthening mechanism, since any broken bond would appear as a trap in the oxide, the reduced trapping characteristics of the present oxide clearly indicate that in the present tunnel oxides, the bond breaking or distortion is minimum. The reduced barrier height obtained for the $N_2O$-annealed oxide is due to the enhanced incorporation of nitrogen compared to the $N_2$-annealed oxides, as shown in Fig. 5. It has been reported by several authors [20], [21], [23] that SILC also depends on the formation of neutral traps apart from the creation of interface and bulk traps. The improved SILC of the "wet $N_2O$" tunnel oxides in this paper suggests the reduction in the creation of neutral traps and interface and bulk traps during stress. The present tunnel oxides grown by the "wet $N_2O$" process and annealed in $N_2O$ have shown the lowest SILC compared to reference oxides reported in the literature, and this can be attributed to the higher incorporation of nitrogen into the tunnel oxide. In addition, this higher nitrogen concentration at the interface enables to give the tunnel oxide higher immunity to bond breaking during CCS and gives improved interface and bulk trap properties. Further work is necessary to obtain fundamental levels of understanding the nature of bonds and their implication on the results.

## V. Summary and Conclusion

This paper on "wet $N_2O$" oxides has shown that these tunnel oxides have superior qualities for application in Flash memory devices with low SILC, minimum increase in traps during constant-current stressing, and high charge-to-breakdown. The $J$–$E$ characterizations have shown that a higher incorporation of nitrogen into the tunnel oxide reduces the barrier height. The interface and oxide trapping studies have demonstrated that the present oxides have indeed good immunity to trap generation compared to the various nitrided tunnel oxides reported in the literature. Based on the XPS studies, we have demonstrated for the first time that a nitrogen concentration of 8.5% can be introduced into the oxide–silicon interface by this low-temperature "wet $N_2O$" oxidation and $N_2O$ annealing process at 800 °C, which is responsible for the improved performance characteristics and reliability of the MOS devices.

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