Twelve-Sided Polygonal Voltage Space Vector Based Multilevel Inverter for an Induction Motor Drive With Common-Mode Voltage Elimination

Sanjay Lakshminarayanan, Student Member, IEEE, Gopal Mondal, Student Member, IEEE, P. N. Tekwani, Student Member, IEEE, K. K. Mohapatra, and K. Gopakumar, Senior Member, IEEE

Abstract—In this paper, a 12-sided polygonal voltage space vector generation with common-mode voltage elimination (CME) is proposed for an induction motor drive. An open-end winding configuration is used for the motor. The proposed multilevel structure is achieved by cascading only the conventional two-level inverters with asymmetrical dc link voltages. By appropriately selecting the voltage vectors with identical common-mode voltage from the opposite ends, a pulsewidth modulation (PWM) strategy with zero common-mode voltage variation can be achieved for the entire modulation range with a common dc link requirement for both the inverter systems. Along with the CME, the proposed 12-sided polygonal space vector based multilevel inverter structure has increased modulation range with the absence of 5th, 7th, 17th, 19th, etc., harmonics up to 12-step operation. The bandwidth problems associated with conventional hexagonal voltage space vector structure current controllers due to the presence of 5th and 7th harmonics in the overmodulation region are absent in the present 12-sided structure. So a simple PWM voltage control with linear voltage control up to 12-step operation is possible from the present 12-sided scheme with less current control complexity.

Index Terms—Common-mode voltage elimination (CME), multilevel inverter, polygonal voltage space vector.

I. INTRODUCTION

TWO-LEVEL inverters are seldom preferred for drive applications at higher power levels due to problems such as electromagnetic interference, switching losses, switch voltage stress, and harmonic distortion. Neutral-point-clamped (NPC) three-level inverters, cascaded H-bridge, and flying capacitor multilevel structures are some of the popular schemes used for high-power applications [1]–[7]. For the H-bridge topology, the dc link power supply requirements increase with the increase in output levels [3], [5]–[7]. Normally, the number of switching devices and the complexity go up with the number of levels [3]. In the extreme modulation range, pulsewidth modulation (PWM) based on the hexagonal voltage space phasor structure [3]–[6] from these multilevel converters will have substantial 5th and 7th harmonics in the motor phase voltage. These harmonic currents restrict the bandwidth of the closed-loop current controllers and require a different approach for current controller design in the overmodulation region [8].

Multilevel inverter-fed induction motor drives can also be realized by feeding the motor from both ends (open-end winding) using conventional inverter structures [9]–[11]. In [11], a three-level voltage structure is realized for an open-end winding drive by feeding the motor from the opposite ends with reduced dc link voltages. A three-level inverter configuration can also be built by cascading conventional two two-level inverters [12] and will have a simple power bus structure compared to the conventional NPC three-level inverters. A seven-level voltage space vector structure is realized in [13] for an open-end winding drive by feeding a cascaded three level [12] from one end and a conventional two level from the other end. But all these multilevel structures have a hexagonal voltage space vector periphery that results in the same PWM control complexity in the overmodulation region, as in the case of conventional two-level structure, due to the presence of low 5th- and 7th-order harmonics. Multilevel inverters reduce the common-mode voltage variations compared to a conventional two-level inverter. The presence of common-mode voltage variations at pole voltages can lead to leakage currents between the motor and the inverter through motor bearings [14]–[16]. This can lead to bearing failure in the long run. Different schemes and modulation techniques have been reported to eliminate common-mode voltage (CME) variation at the inverter poles [17]–[19]. In [18] and [19], the common-mode voltage variation elimination for a three-level and a five-level voltage space vector structure for an open-end winding drive is achieved by using only the switching state redundancies.

A 12-sided polygonal space vector based multilevel inverter is an improvement over the conventional hexagonal space vector based inverter. The maximum value of the fundamental component that can be generated is 0.658 $V_{dc}$ (12-step operation) compared to 0.637 $V_{dc}$ in the conventional hexagonal space vector method. Since a 12-sided polygon is used for space vector PWM control, all the $6n \pm 1 (n = 1, 3, 5, \ldots)$ harmonics will be absent through the modulation range extending up to the 12-step operation and require a simple voltage and current control for the entire modulation range. A 12-sided polygonal voltage space phasor structure is reported in [20] for an open-end winding induction motor drive. The 12-sided polygonal structure in [20] is achieved by inverters with asymmetrical dc link voltages. In [21], a 12-sided polygonal voltage space vector structure is realized using cascaded two-level inverters.
Fig. 1. (a) Power circuit of the 12-sided polygonal space vector based multi-level inverter. (b) Asymmetrical dc link voltage generation.

for an IM drive without using the open-end winding structure. Here, the lower cascaded inverter needs high blocking voltages. The disadvantage of the 12-sided voltage phasor generation proposed in [20] and [21] is that large common-mode voltage variation is present at the motor pole voltages. In this paper, a method is proposed for achieving the 12-sided polygonal space vectors for an induction motor drive with CME for the entire modulation range using inverters with reduced dc link voltage when compared to [20] and [21].

II. POWER CIRCUIT OF THE PROPOSED INVERTER DRIVE

A schematic of the power circuit of the proposed induction motor drive is shown in Fig. 1(a). An open-end winding configuration is used for the motor drive. The overall configuration consists of two three-level inverters INV-A and INV-B realized by cascading two conventional two-level inverters [12] fed from two asymmetrical dc link voltages of 1 and 0.366 kV dc [Fig. 1(a)]. The factor “k” can be chosen such that the radii of the 12-sided polygon and the conventional hexagonal structure are equal. The high-voltage dc link (1 kV dc) can be split into two levels of 0.634 and 0.366 kV dc, and knowing that 0.634 is equal to $\sqrt{3} \times 0.366$, the dc links can be realized using transformer secondaries of the same number of turns, as shown in Fig. 1(b) with star–delta connection. Alternately, two secondaries with turns ratio of 1 : 0.366 can also be used for front-end rectifiers for realizing the dc link voltages. Each pole of an inverter (INV-A or INV-B) can attain three different voltage levels depending on the inverter switching state. Switches on the same leg such as $S_{21}$ and $S_{24}$ are operated complementary to each other. When switch $S_{24}$ is on, pole A assumes a voltage level of zero, and when $S_{14}$ and $S_{21}$ are on, the inverter pole A attains 0.366 kV dc. When $S_{11}$ and $S_{21}$ are on, inverter pole A attains 1.366 kV dc. Table I summarizes the switching states. A “0” represents the OFF-state and “1” the ON-state of a switch. A “0/1” implies that the switch can be on or off. In each inverter, switches of the upper leg such as $S_{11}$ and $S_{14}$ need to have a voltage blocking capacity of 1.0 kV dc, while the switches of the lower leg such as $S_{21}$ and $S_{24}$ need to have a voltage rating of 1.366 kV dc.

III. GENERATION OF 12-SIDED POLYGONAL VOLTAGE SPACE VECTORS

Any of the poles of the two inverters can take on one of three levels independent of the other. “$\phi$” represents any arbitrary level and carries a “don’t care”-like meaning. Fig. 2 shows 12-pole voltage space vectors from INV-A and INV-B. The voltage space vectors at location P, Q, E, F, I, and J (Fig. 2) are realized from the pole voltages of INV-A, and the voltage space vectors at location R, S, G, H, K, and L are realized from the pole voltages of INV-B. Consider the space vector OQ of INV-A shown as $(210)$ in Fig. 2. Pole-A at level 2 produces 1.366 kV dc (Table I), which is shown by OA along the A phase axis; pole B at level 1 produces 0.366 kV dc, which is shown by AQ along the B axis; pole C is
at level 0; and the resultant is OQ. The resultant voltage space vector OQ will have a magnitude equal to 1.225 \( V_{dc} \). This can be easily verified from the geometry in Fig. 2. The voltage space vector “OQ” is generated from INV-A alone and is independent of the switching state of INV-B. So for the voltage space vector generation OQ, the poles of INV-B can be in any state and is represented by \( (\varphi\varphi\varphi)_0 \) in Fig. 2. In a similar way, vector OP is a voltage space vector generated from the pole voltages of INV-A, which is represented by \( (201)^{\ast} \). Voltage space vectors OR and OS are close to the negative axis-c and are generated from the pole voltages of INV-B. For the voltage space vector “OR,” the pole voltage levels of INV-B are given by \( (\varphi\varphi\varphi)(0'1'2') \). Here, INV-A can also be in any state. The voltage space vector “OB” is along the negative axis-c with a magnitude of 1.366 \( V_{dc} \); the magnitude of “BR” is 0.366 \( V_{dc} \) along the negative axis-b; and the vector addition results in the voltage space vector “OR.” The inverter switching states for the other locations are shown in Fig. 2.

The phase winding of the open-end induction machine is connected across the poles of the two inverters INV-A and INV-B. If we select voltage space vector combinations from the two inverters of INV-A (dashed lines in Fig. 2) and INV-B (solid lines in Fig. 2), which are 60° apart, a combined 12-sided polygonal structure (Fig. 3) will be obtained from the drive system. For example, the inverter vector OP from INV-A (dashed line in Fig. 2) and the vector OR from INV-B (solid line in Fig. 2) will together generate the vector at location -1 (Fig. 3). The resultant 12-sided voltage space vector combinations from INV-A and INV-B are shown in Fig. 3. Table II gives the voltage levels at the inverter poles for all the 12 locations of the 12-sided polygon. From Table II, it can be noted that the 12-sided voltage space vector structure in Fig. 3 is achieved by the vector addition of voltage space vectors (with a magnitude of 1.225 \( V_{dc} \) each [20]) from INV-A and INV-B, which are separated by 60°. The inverter switch transitions for generating the combined 12-sided polygonal voltage vector structure in Fig. 3 can be realized using Fig. 4(a)–(c) and Table II. Fig. 4(a) shows the ON or OFF conditions of the inverter switches for realizing the combined voltage space vector structure location at “12” in Fig. 3. Here, the left-hand side inverter [INV-A, Fig. 1(a)] pole voltage level is (210), and the right hand side inverter (INV-B) pole voltage level is (0'2'1'). Fig. 4(b) and (c) shows the switch transitions for the voltage space vector locations at “1” and “2” of Fig. 3. In a similar way, the inverter switch transitions for other locations can also be easily found out. The resultant radii of the 12-sided polygon generated from the combined inverters is (Fig. 3)

\[
\text{Magnitude of OR is } = 2 \times 1.225 \times \frac{\sqrt{3}}{2}. \tag{1}
\]

The value of “k” can be selected to be 0.471 \( (1/1.225 \times \sqrt{3}) \), so that the magnitude of the radii of the 12-sided voltage space vector (Fig. 3) will be \( V_{dc} \), which is the magnitude of the radii of the hexagonal voltage space vector structure from the conventional two-level inverter. Now for a resultant 12-sided polygonal radii of \( V_{dc} \) (same as that of a hexagonal structure from the conventional two-level inverter), the lower dc link requirement (Fig. 1) of the inverter is \( k = 0.471 \)

\[
\text{Lower dc link voltage (Fig. 1)} \]

\[
0.366 \times V_{dc} = 0.366 \times 0.471 \times V_{dc} = 0.172 \times V_{dc}. \tag{2}
\]

\[
\text{Upper dc link voltage (Fig. 1)} \]

\[
1.0 \times V_{dc} = 1.0 \times 0.471 \times V_{dc} = 0.471 \times V_{dc}. \tag{3}
\]

This shows that only low dc link voltages are needed for the the proposed multilevel inverters with 12-sided polygonal voltage space vector structure (17% and 47% of the dc link voltage \( V_{dc} \) of a conventional two-level inverter). The inverter structure can be realized by cascading conventional two-level inverters, which results in reduced power circuit complexity for the proposed multilevel structure. The proposed PWM voltage control is based on a 12-sided polygon, and it will give an increased modulation range with the absence of \( 6n \pm 1 \) \( (n = 1, 3, 5, \ldots) \) order harmonics for the entire modulation range. In the extreme modulation range (12-step operation), the phase peak maximum amplitude is 0.658 \( V_{dc} \) when compared to 0.637 \( V_{dc} \) for hexagonal voltage space phasor based conventional multilevel inverters. Since the proposed scheme does not

**Table II: Combinations for 12-Sided Polygonal Active Vectors and Zero Vectors**

<table>
<thead>
<tr>
<th>Space vector location (Fig.3)</th>
<th>INV-A active vectors</th>
<th>INV-B active vectors</th>
<th>Inverter switching states from INV-A and INV-B for Zero voltage vector for PWM operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>201 ( 0'1'2' )</td>
<td>201 ( 2'0'1' )</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>210 ( 1'0'2' )</td>
<td>210 ( 2'1'0' )</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>120 ( 0'1'2' )</td>
<td>012 ( 0'1'2' )</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>021 ( 1'0'2' )</td>
<td>102 ( 1'0'2' )</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>120 ( 2'0'1' )</td>
<td>120 ( 1'2'0' )</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>021 ( 2'1'0' )</td>
<td>021 ( 0'2'1' )</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>012 ( 2'0'1' )</td>
<td>201 ( 2'0'1' )</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>102 ( 2'1'0' )</td>
<td>210 ( 2'1'0' )</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>012 ( 1'2'0' )</td>
<td>012 ( 0'1'2' )</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>102 ( 0'2'1' )</td>
<td>102 ( 1'0'2' )</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>201 ( 1'2'0' )</td>
<td>120 ( 1'2'0' )</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>210 ( 0'2'1' )</td>
<td>021 ( 0'2'1' )</td>
<td></td>
</tr>
</tbody>
</table>
have $6n \pm 1 (n = 1, 3, 5, \ldots)$ harmonics in the motor phase current waveform, the current will be very smooth in the extreme 12-step mode operation. So, special compensated synchronous reference frame proportional–integral (PI) controllers [8] are not needed in the overmodulation region (as in the case of conventional hexagonal space phasor PWM scheme) for operation in high dynamic performance applications such as vector control scheme. Another advantage of the present inverter-fed drive scheme is that common-mode voltage variation can be eliminated (CME) for the entire modulation range up to 12-step mode. This will eliminate the problem associated with common-mode voltage variation such as leakage currents and bearing erosion, which eventually leads to drive system failure in the long run [14]–[16].

### IV. PWM WITH 12-SIDED POLYGONAL SPACE VECTORS

Consider the case of a reference space vector $V_r$ moving inside the 12-sided polygon formed by space vectors from INV-A and INV-B in Fig. 3. The rotating voltage space vector $V_r$ is sampled with a time period $T_S$. The reference vector can be generated by time averaging the two nearest voltage space vectors, which forms a sector (12 sectors), within which the reference voltage falls. For example, for the reference vector $V_r$ lying in the sector between the space vector locations “12” and “1” in Fig. 3, the vector location at “12” is switched on for time period $T_1$ and the vector “1” for time $T_2$. A zero voltage is maintained for a time $T_0 = T_S - T_1 - T_2$. In the present scheme, the zero voltage is maintained for time period $T_0/2$ at the beginning of the sampling period $T_S$ and at the end of the sampling period. Note that a zero vector is chosen as in Table II such that there is no variation in the common-mode voltage in INV-A and INV-B.

A. **PWM Switching With CME**

The common-mode voltage generated at the pole voltages of INV-A for the vector generation “OP” (Fig. 2) is

$$V_{cm-A}(201) = \frac{1.366 \, kV_{dc} + 0 + 0.366 \, kV_{dc}}{3}. \quad (4)$$

Similarly, the common-mode voltage generated at the pole voltages of INV-B for the vector generation “OR” (Fig. 2) is

$$V_{cm-B}(021) = \frac{0 + 1.366 \, kV_{dc} + 0.366 \, kV_{dc}}{3}. \quad (5)$$

The combination of these two vectors will have the resultant location at “1,” which is shown in Fig. 3. In all the 12 active vector formations (Fig. 3), it can be noted from Table II (INV-A and INV-B levels) that the common-mode voltage generated is constant at the inverter poles. Thus, by properly selecting the voltage space vectors from INV-A and INV-B in Fig. 2, a resultant 12-sided polygonal voltage space vector structure with zero common-mode voltage variation can be achieved for the induction motor drive. But for PWM operation at various modulation indices, apart from switching the adjacent vectors of the 12-sided polygon (Fig. 3) from the opposite inverters, for modulation indices less than for the 12-step operation, the motor phases need to be at zero voltage state in a sampling interval. One way to get the zero voltage state for the motor phases is to clamp both inverter poles to zero state (Table I). Here, the motor phases will have zero voltage during zero inverter vector states, and during the active vector states, in all the 12 sectors, according to (4) and (5), the motor phases will not have common-mode voltage (triplet order harmonics). Hence, the two inverters can be fed from a common dc link (Fig. 1). But, in order to eliminate the common-mode voltage variation (from the inverter poles and across the machine phase windings), a constant common-mode voltage (implies zero common-mode voltage variation) during active as well as zero vector states is sufficient. This can be achieved for the present drive by switching appropriate vectors during the zero-vector period in the sampling interval, as shown in Table II. From Table II and using (4) and (5), it can be noted that during the zero-vector periods, INV-A and INV-B also generate constant common-mode voltage (zero common-mode voltage variation).
Let \( V \) be the magnitude of the space vectors 1–12 in Fig. 3, and let \( \text{"m"} \) be the sector number of the sector in which \( V_r \) lies (Fig. 5).

### A. \( T_1 \) and \( T_2 \) Computation From Sampled Reference Phase Amplitudes

The volt–second balance equation for the reference voltage in any sector is

\[
T_1.\beta V ((m-1)30^\circ - 15^\circ) + T_2.\beta V((m30^\circ - 15^\circ) = T_S.(V_\alpha + jV_\beta) \tag{6}
\]

where \( \text{"m"} \) is the sector (\( m \) varies from 1 to 12).

The 15° accounts for the shift in the \( \alpha \)-axis [the \( \alpha \)-axis is not coinciding with the sector side (Fig. 3)]. If the 12 voltage space vectors were shifted by 15° clockwise, the \( \alpha \)-axis will coincide with the sector side (Fig. 5). Now the volt–second balance for the 12-sided polygon in Fig. 5 can be rewritten as

\[
T_1.V \beta((m-1)30^\circ) + T_2.V \beta(m30^\circ) = T_S.(V_\alpha + jV_\beta). \tag{7}
\]

On equating real and imaginary parts and simplifying, the switching periods \( T_1 \) and \( T_2 \) can be written as

\[
\begin{align*}
\left( \frac{T_1}{T_2} \right) &= \frac{2T_S}{V} \left( \sin((m30^\circ)) - \cos((m30^\circ)) \right) \times \left( V_\alpha \right) \tag{8}
\end{align*}
\]

\( V_\alpha \) and \( V_\beta \) can be substituted in terms of the sampled reference phase amplitudes \( v_A, v_B, \) and \( v_C \) using

\[
\begin{align*}
V_\alpha &= \frac{3}{2}v_A \\
V_\beta &= \frac{\sqrt{3}}{2}(v_B - v_C). \tag{9}
\end{align*}
\]

From (8) and (9), the switching periods \( T_1 \) and \( T_2 \) can be evaluated in each sector in terms of the sampled reference phase amplitudes in that sector, as shown in Table III, and can be computed very fast. This does not require any complicated computations. Sector identification can also be done very easily based on sampled reference phase amplitudes using the algorithm given below.

#### In quadrant 1:
- If \( |v_B - v_C| \leq |v_A| \) then sector 1, else
- If \( |v_B - v_C| \leq 3, |v_A| \) then sector 2, else sector 3

#### In quadrant 2:
- If \( |v_B - v_C| \leq |v_A| \) then sector 6, else
- If \( |v_B - v_C| \leq 3, |v_A| \) then sector 5, else sector 4

#### In quadrant 3:
- If \( |v_B - v_C| \leq |v_A| \) then sector 7, else
- If \( |v_B - v_C| \leq 3, |v_A| \) then sector 8, else sector 9

#### In quadrant 4:
- If \( |v_B - v_C| \leq |v_A| \) then sector 12, else
- If \( |v_B - v_C| \leq 3, |v_A| \) then sector 11, else sector 10

A detailed account of the derivation is available in [21]. Here, it can also be seen that sector identification is very fast and only requires sampled reference phase amplitudes, and it can be easily implemented in a drive scheme with digital signal processor based controllers. Once the inverter switching times are computed for various sectors, the PWM control of the voltage space vector structure in Fig. 3 can be realized by using the inverter gating sequence from Table II for the corresponding sector.

### V. Simulation and Experimental Verification

A simple \( V/f \) scheme is used in this paper. The drive scheme is first simulated using Simulink and later experimentally verified in a 2-kW induction motor drive with insulated-gate bipolar transistor inverters. A total dc link voltage of 124 V is used for the simulation study. The upper dc link voltage is 91 V, and the lower one is 33 V. The \( V/f \) scheme is implemented using a TMS 320 F2407 platform. The inverter switching times are calculated from the sampled reference phase amplitudes using expressions presented in Table II and from the sector identification technique presented in the previous section. Based on the sector and the timing signals, the inverter gating signals are generated using PALCE22v10.

The number of samples in a sector is so chosen so that the overall switching frequency is limited (<1000 Hz) in order to keep the switching losses low while maintaining sufficient resolution.

If \( \text{"f"} \) is the operating frequency, the following sampling scheme is used:

1. \( 0 < f <= 15 \) Hz: four samples per sector;
2. \( 15 < f <= 30 \) Hz: three samples per sector;
3. \( 30 < f <= 45 \) Hz: two samples per sector;
4. \( 45 < f <= 50 \) Hz: one sample per sector.

The drive scheme is operated at various modulation indices, and the inverter switching times are computed using Table III. The inverter active vectors for PWM control are selected from Table II. For modulation indices less than for the 12-step operation, initially, the zero-vector states are achieved by switching both inverter poles to the lower dc link rail (zero level, Table I). This will result in common-mode voltage
TABLE III

<table>
<thead>
<tr>
<th>Sector 1</th>
<th>Sector 2</th>
<th>Sector 3</th>
<th>Sector 4</th>
<th>Sector 5</th>
<th>Sector 6</th>
</tr>
</thead>
<tbody>
<tr>
<td>( T_1 )</td>
<td>( \frac{\sqrt{3}}{P} V_g )</td>
<td>( \frac{\sqrt{3}}{P} V_g )</td>
<td>( \frac{\sqrt{3}}{P} V_g )</td>
<td>( \frac{\sqrt{3}}{P} V_g )</td>
<td>( \frac{\sqrt{3}}{P} V_g )</td>
</tr>
<tr>
<td>( T_2 )</td>
<td>( \frac{\sqrt{3}}{P} V_g )</td>
<td>( \frac{\sqrt{3}}{P} V_g )</td>
<td>( \frac{\sqrt{3}}{P} V_g )</td>
<td>( \frac{\sqrt{3}}{P} V_g )</td>
<td>( \frac{\sqrt{3}}{P} V_g )</td>
</tr>
<tr>
<td>Sector 7</td>
<td>Sector 8</td>
<td>Sector 9</td>
<td>Sector 10</td>
<td>Sector 11</td>
<td>Sector 12</td>
</tr>
<tr>
<td>( T_1 )</td>
<td>( \frac{\sqrt{3}}{P} V_g )</td>
<td>( \frac{\sqrt{3}}{P} V_g )</td>
<td>( \frac{\sqrt{3}}{P} V_g )</td>
<td>( \frac{\sqrt{3}}{P} V_g )</td>
<td>( \frac{\sqrt{3}}{P} V_g )</td>
</tr>
<tr>
<td>( T_2 )</td>
<td>( \frac{\sqrt{3}}{P} V_g )</td>
<td>( \frac{\sqrt{3}}{P} V_g )</td>
<td>( \frac{\sqrt{3}}{P} V_g )</td>
<td>( \frac{\sqrt{3}}{P} V_g )</td>
<td>( \frac{\sqrt{3}}{P} V_g )</td>
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</table>

Fig. 6. (a) INV-A pole voltage with common-mode voltage variation. (b) Common-mode voltage variation at inverter poles (simulation study: –30 Hz).

variation at inverter poles [Fig. 6(a)]. But for the phase voltage waveform (subtraction of the opposite inverter pole voltages), there will be no common-mode voltage variation. The simulation result in Fig. 6(a) shows the pole voltage-A switchings for 15-Hz operation, and Fig. 6(b) shows the high-frequency common-mode voltage variation (triplen order). To eliminate problems associated with common-mode voltage variations such as leakage currents and bearing erosion [14], the common-mode voltage variation at the inverter poles also needs to be eliminated for the complete speed range. This is achieved by switching identical inverter switching vectors from INV-A and INV-B [Fig. 1(a)] during the zero-vector periods for PWM operation in a sampling period. The inverter vector states (to eliminate common-mode variation) during the zero-interval period in each sector are shown in Table III. From Table III, it can be noted that the common voltage generation [4] and (5)] is the same for the active and zero vectors, which results in zero common-mode voltage variation. The simulation results of the pole voltage and the zero common-mode voltage variation (constant common-mode voltage) are shown in Fig. 7. The pole voltages and the phase voltages from the experimental result with zero common-mode voltage variation are presented in Fig. 8(a). The pole voltage variation from the experimental result [Fig. 8(a)] is identical to the simulation result in Fig. 7. Fig. 8(b) shows the relative harmonic content of the pole voltage in Fig. 8(a). Fig. 8(b) shows the absence of triplen content (common-mode voltage) with the proposed PWM technique, as shown in Table III with inverter switching vector selection. Once the common-mode voltage variation is eliminated, the two inverters [INV-A and INV-B, Fig. 1(a)] can be connected with a common dc link. The same technique is used for all the modulation indices extending up to the 12-step mode. The fundamental and harmonic amplitudes of the motor phase voltage are computed for different speeds of operation up to 50 Hz (12-step mode) for the aforementioned number of samples in a sector. The motor phase voltage and its relative harmonic content for 15 Hz, 30 Hz, 45 Hz, and 12-step mode are presented in Figs. 9–12, respectively. The harmonic spectrums for various speed ranges show that the triplen content is absent from the motor phase voltage, and all the 5th and 7th harmonic contents are also eliminated from the drive system, which results in a nearly sinusoidal current, compared to multilevel inverters with hexagonal space vector structure [10]–[12], [18], [19]. This will enable a simple current control operation, and special compensated synchronous reference frame controllers [8] are not needed for the proposed scheme when used in high-dynamic performance applications such as vector control. In an inverter pole, the high-voltage inverter leg is switched only for the 50% duration in a cycle of operation. This is very clear from the pole voltages in Figs. 7 and 8. This will also considerably reduce the inverter...
Fig. 9. (a) Phase voltage and current (no load current) at 15 Hz. x-axis: 1 div = 10 ms, y-axis: upper trace: 1 div = 100 V, lower trace: 1 div = 1 A (experimental result). (b) Relative harmonic spectrum of phase voltage.

Fig. 10. (a) Phase voltage and current (no load current) at 30 Hz. x-axis: 1 div = 5 ms, y-axis: upper trace: 1 div = 70 V, lower trace: 1 div = 1 A (experimental result). (b) Relative harmonic spectrum of phase voltage.

Fig. 11. (a) Phase voltage and current (no load current) at 45 Hz. x-axis: 1 div = 5 ms, y-axis: upper trace: 1 div = 70 V, lower trace: 1 div = 1 A (experimental result). (b) Relative harmonic spectrum of phase voltage.

Fig. 12. (a) Phase voltage and current (no load current) at 50 Hz. x-axis: 1 div = 5 ms, y-axis: upper trace: 1 div = 70 V, lower trace: 1 div = 1 A (experimental result). (b) Relative harmonic spectrum of phase voltage.

Fig. 13. Fundamental and the harmonics for the complete speed range (triplet order and 6n ± 1, n = 1, 3, 5, ...) harmonics are absent).

VI. CONCLUSION

A 12-sided polygonal voltage space phasor generation for an induction motor drive with CME is proposed in this paper. An open-end winding structure is used for the induction motor drive. The proposed multilevel structure is achieved by using switching losses for the proposed multilevel inverter scheme. Also, the proposed scheme gives a very simple linear control throughout the modulation range from the proposed PWM scheme (Fig. 13). Fig. 13 shows the fundamental amplitude and harmonics for the full modulation range. It can be seen that the fundamental is varying linearly (for the full modulation range), and lower-order harmonic amplitudes are highly suppressed with the total absence of 5th, 7th, 17th, 19th, etc., harmonics.

The experimental results and the harmonic analysis show that the proposed 12-sided polygonal voltage space phasor based PWM drive is capable of eliminating the common-mode voltage variation at the poles and in the motor phase for the entire modulation range with a simple power circuit structure.

The proposed PWM voltage control is based on a 12-sided polygon, and it will give an increased modulation range with the absence of 6n ± 1 (n = 1, 3, 5, ...) order harmonics for the entire modulation range. In the extreme modulation range, the phase peak maximum amplitude is 0.658 Vdc when compared to 0.637 Vdc for hexagonal voltage space phasor based conventional multilevel inverters. Since the proposed scheme does not have 6n ± 1 (n = 1, 3, 5, ...) harmonics in the motor phase current waveform, the current will be very smooth in the extreme 12-step mode operation. So, complicated compensated synchronous reference frame PI controllers [8] are not needed in the overmodulation region (as in the case of conventional hexagonal space phasor PWM scheme) for operation in high dynamic performance applications such as the vector control scheme. Also, the proposed scheme gives a motor operation with zero common-mode voltage, which thus totally eliminates all the problems associated with common-mode voltage variation [14], [15]. Also, the high-voltage inverter of the cascaded structure...
is switched only for 50% duration in a cycle of operation. This will considerably reduce the inverter switching losses and thereby increase the efficiency of the overall drive system. So the proposed scheme can be considered for inverter-fed induction motor drives in low- and medium-voltage high-power applications.

REFERENCES


Sanjay Lakshminarayanan (’95) received the B.Tech. degree from the Indian Institute of Technology (IIT), Kharagpur, India, in 1990 and the M.Sc. (Engg.) degree in electrical engineering from the Indian Institute of Science (IISc), Bangalore, India, in 1995. He is currently working toward the Ph.D. degree at IISc.

He has been in the industry for about ten years. He was with Reliance Technologies, Haldia, Haldia Insulators Ltd., Haldia, and GE Medical Systems, Bangalore. His present area of research is in multilevel inverters.

K. K. Mohapatra (M’94–SM’96) received the B.E. degree in electrical engineering from Regional Engineering College (R.E.C.), Rourkela, India, in 1993, the M.Tech. degree in electrical engineering from the Indian Institute of Technology, Kharagpur, India, in 1996, and the Ph.D. degree from the Indian Institute of Science, Bangalore, India, in 2003. He is currently working toward a Postdoctoral Fellowship at the University of Minnesota, Minneapolis.

From 1995 to 2000, he was a Design and Development Engineer at the National Radio and Electronics Company Ltd., Maharashtra, India. His research interests are in the area of power converters, PWM strategies, and motor drives.

Gopal Mondal (S’06) received the B.E. degree in power electronics from Saurashtra University, Morbi, India, in 1995 and the M.E. degree in electrical engineering from the M.S. University, Vadodara, India, in 2000. He is currently working toward the Ph.D. degree at the Indian Institute of Science, Bangalore, India.

From 1995 to 1996, he was with Amtech Electronics, Gandhinagar, India. From 1996 to 2001, he was with the Electrical Research and Development Association (ERDA), Vadodara, India. Since 2001, he has been a member of the Faculty at the Nirma University of Science and Technology, Ahmedabad, India.