# A Dual Five-Level Inverter-Fed Induction Motor Drive With Common-Mode Voltage Elimination and DC-Link Capacitor Voltage Balancing Using Only the Switching-State Redundancy—Part II

P. N. Tekwani, *Student Member, IEEE*, R. S. Kanchan, *Student Member, IEEE*, and K. Gopakumar, *Senior Member, IEEE*

***Abstract*—The open-loop control scheme presented in part I of this paper for a dual five-level-inverter-fed induction motor (IM) drive with two dc power supplies maintains dc-link capacitor voltage balancing and common-mode voltage (CMV) elimination throughout the operating range of the drive. The operating limitation of the proposed open-loop control scheme to take corrective action toward the existing unbalance in the dc-link-capacitor voltages is also pointed out in part I of this paper. As a solution to this, a simple closed-loop control scheme, which is based only on the switching-state redundancy, is proposed in this part of the paper. The proposed closed-loop control scheme not only prevents further unbalancing of capacitor voltages but also takes corrective actions to bring back the capacitor voltages in the balanced state. The proposed closed-loop scheme achieves dc-link capacitor voltage balancing and elimination of CMV together in the complete modulation range, including overmodulation of up to the 24-step operation. The proposed control scheme does not affect the output fundamental voltage generated by the inverter, as it effectively utilizes only the availability of redundant switching states of the inverter, and does not call for additional power circuit hardware. The scheme is presented with the simulation studies and experimentally verified with a 1.5-kW open-end winding IM drive.**

***Index Terms*—Closed-loop control, common-mode voltage (CMV) elimination, dc-link capacitor voltage balancing, induction motor (IM) drive, multilevel inverter, switching-state redundancy.**

## I. Introduction

MULTILEVEL converters are considered for high-power medium-voltage drive applications, because the power structure can be realized with devices of lower voltage ratings [1]–[10]. A five-level inverter structure by cascading conventional two-level and three-level inverters is proposed in Part I of this paper [20]. An open-loop control scheme is presented in Part I to maintain dc-link capacitor voltage balancing and common-mode voltage (CMV) elimination in a dual five-level inverter-fed open-end winding induction motor (IM) drive, which effectively uses only the available redundant switching states of the inverter. It is pointed out that the proposed open-loop controller is unable to take any corrective action to reduce the unbalance in the capacitor voltages that may arise in actual practice due to the use of asynchronous pulsewidth-modulation (PWM) with low switching frequency, unbalanced load currents, mismatch in power device characteristics, etc. Hence, a closed-loop control action is needed that stops not only the further unbalancing of capacitor voltages but also takes the corrective actions to bring back the capacitor voltages in the balanced state.

Various closed-loop control schemes for balancing the dc-link-capacitor voltages in the multilevel-inverter-fed IM drives have been proposed in the literature [11]–[18]. A comprehensive study of the neutral-point balancing problem and various approaches to solve the same are provided (with their theoretical limitations) for the three-level neutral-point-clamped (NPC) PWM voltage-source inverter (VSI) in [11]. It is suggested in [12] that the neutral-point control for the three-level inverter can be done from either the grid-side converter or the inverter itself by the coordinated control. The neutral-point balancing scheme proposed in [12] determines the time duration of the various inverter vectors in the switching interval such that the total error in the capacitor voltages is less than the threshold limit. The time intervals for the initial and end inverter switching vectors (in a PWM sampling interval) are thus not equal, and the PWM implementation, in this way, is no longer a space-vector PWM. A back-to-back structure of the controlled converter and inverter is proposed in [13] and [14] for the multilevel-inverter-fed IM drive system. By monitoring the voltages of each of the dc-link levels, adjustments of either the inverter switching angles or the controlled rectifier switching angles are proposed in [14], which will transfer a net charge into or out of a particular voltage level to adjust the dc-link voltage levels. A three-phase five-level voltage-source PWM front-end converter controlled by multiband hysteresis comparators has been proposed in [15] to supply the dc-link of a five-level-inverter-fed IM drive. However, the level control carried out by the converter proposed in [15] leads to significant input-current distortion. A balancer circuit that consists of eight series-connected and sequentially switched insulated-gate bipolar transistors and two inductors to provide temporary energy storage is proposed in [16], which takes the form of a fourth inverter leg in a five-level inverter. The voltage-vector time-compensation method and the voltage-vector output-sequence-reversing method are proposed in [17] to achieve the neutral-point voltage control in three-level voltage NPC VSI, which does not need any extra power

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The authors are with the Centre for Electronics Design and Technology, Indian Institute of Science, Bangalore 560012, India (e-mail: pntek@cedt.iisc.ernet.in; rkanchan@cedt.iisc.ernet.in; kgopa@cedt.iisc.ernet.in).

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hardware. However, in [17], the elimination of CMV is not discussed. A classic survey of various neutral-point voltage-balancing schemes and its coordination among other control requirements in the case of controlled ac–dc–ac conversion is described in [11]. A closed-loop control scheme is presented in [18], for the dc-link capacitor voltage balancing in a dual three-level-inverter-fed open-end winding IM drive, which also provides elimination of CMV without the use of extra power hardware. Recently, some other variants of capacitor voltage-balancing schemes for multilevel inverts are proposed in [4], [6], and [19]; however, these schemes use either extra power hardware or complex control for the capacitor voltage balancing.

This part of the paper proposes a simple closed-loop control scheme, based only on the switching-state redundancy, as a solution to the operating limitation of the open-loop control scheme presented in part I of this paper. The unbalance in dc-link capacitors is sensed, and the switching-state combinations, which can provide proper corrective action for that unbalance, are effectively used in the proposed closed-loop scheme. Effective utilization of the redundant switching states of the inverter voltage vectors eliminates the need for extra hardware for achieving capacitor voltage balancing, without affecting the fundamental output voltage of the inverter. The proposed closed-loop control scheme simultaneously achieves CMV elimination and dc-link capacitor voltage balancing in the linear as well as overmodulation range of operation (up to 24-step mode operation) of the drive. The results of simulation studies are presented, and the same are experimentally verified on a 1.5-kW open-end winding IM drive.

## II. Proposed Closed-Loop Control Scheme for DC-Link Capacitor Voltage Balancing

Fig. 1(a) shows the power schematic of the proposed dual five-level-inverter-fed open-end winding IM drive with two dc power supplies, as described in part I of this paper. The proposed drive of Fig. 1(a) provides a five-level-inverter voltage space vector structure [Fig. 1(b)] with zero CMV, as described in part I of this paper. The five-level voltage space vector structure of Fig. 1(b) is obtained by a total of 361 switching-state combinations, which are responsible for producing a total of 61 voltage space vector locations with zero CMV. These 361 switching-state combinations are used effectively in the proposed closed-loop control scheme to obtain the dc-link capacitor voltage balancing in association with CMV elimination for the entire operating range of the IM drive [Fig. 1(a)]. In the proposed scheme, the unbalance in the dc-link-capacitor voltages is sensed, and the switching-state combinations, which can provide proper corrective action for that sensed unbalance, are effectively used, without disturbing the output fundamental voltage.

### A. Generation of Controller States (CSs) for Closed-Loop Control

In the proposed closed-loop control scheme, the voltages of all four capacitors of the dc-link of Fig. 1(a) are sensed, and the difference in voltages between the two outer capacitors (i.e., $\Delta v_{\rm CC1} = v_{C4} - v_{C1}$) as well as that between the two inner capacitors (i.e., $\Delta v_{\rm CC2} = v_{C3} - v_{C2}$) are used as inputs to two separate hysteresis comparators, as shown in Fig. 2(a). However, assuming constant amplitudes of the two dc power supplies of Fig. 1(a), $V_{\rm dc}/2$ and $V_{\rm dc}/4$, the difference in voltages between the two outer capacitors (i.e., $\Delta v_{\rm CC1} = v_{C4} - v_{C1}$) as well as that between the two inner capacitors (i.e., $\Delta v_{\rm CC2} = v_{C3} - v_{C2}$) can be obtained by using only two voltage sensors. Each of the two three-state hysteresis comparators of Fig. 2(a) can be represented, as shown in Fig. 2(b) [8]. If the input to the comparator ($\Delta v_{{\rm CC}S}$, where $S$ can be 1 or 2) is within the control band, then the hysteresis comparator outputs a state $C_{\rm SN}$, where "N" stands for normal condition, or the comparator outputs a state $C_{\rm SH}$, when its input is greater than or equal to the positive limit of the control band, where "H" indicates high; otherwise, the comparator outputs a state $C_{\rm SL}$, where "L" indicates low. The control band in Fig. 2(b), i.e., $P_{\rm HS} - N_{\rm HS}$, is set depending on the maximum deviation that can be allowed

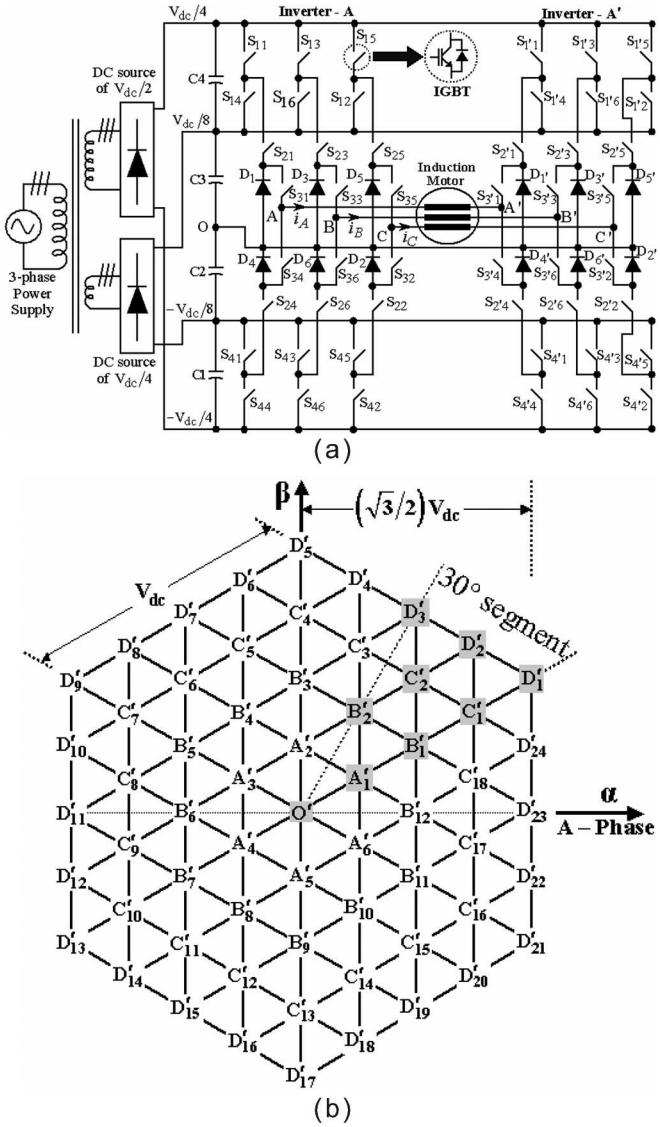



Fig. 1. (a) Power schematic of the proposed IM drive with capacitor voltage balancing and CMV elimination. (b) Five-level-inverter voltage space vector structure of the proposed IM drive generating zero CMV.

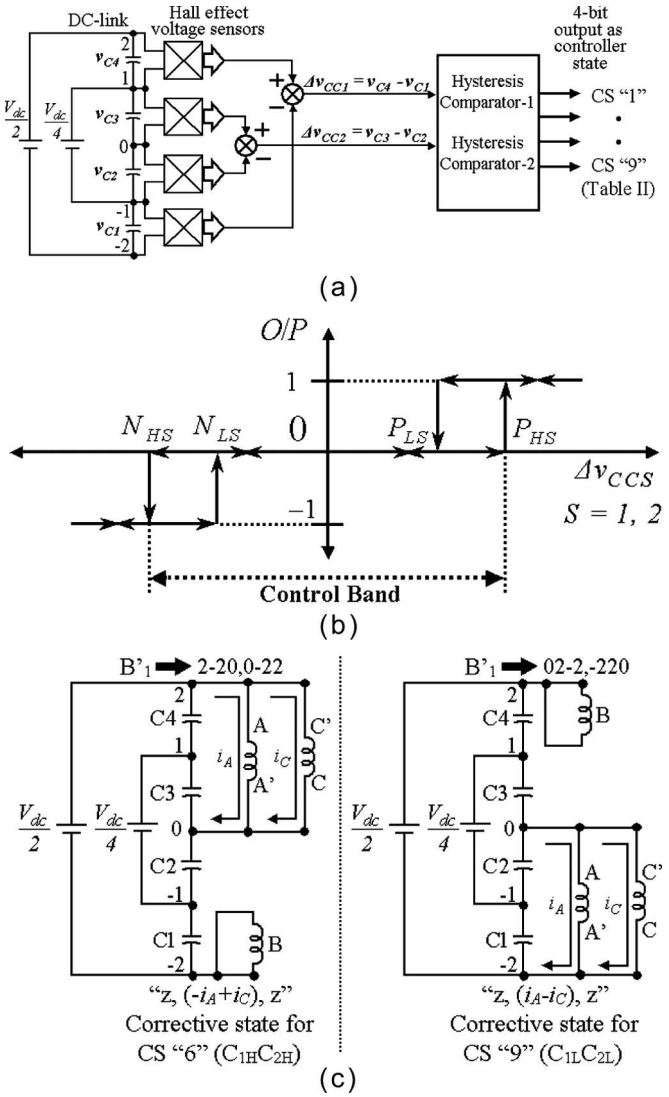



Fig. 2. (a) Block schematic for generation of the CSs for closed-loop control using two three-state hysteresis comparators. (b) Three-state hysteresis comparators used for generation of the CSs in Fig. 2(a). (c) Corrective states of voltage vector $B_1'$: "2–20, 0–22" for CS "6" ($C_{1H}\ C_{2H}$) and "02–2, −202" for CS "9" ($C_{1L}\ C_{2L}$) in the three-level and four-level modes of operation of the proposed drive.

TABLE I
OUTPUT STATES OF EACH OF THE THREE-STATE HYSTERESIS COMPARATORS*

| Input to comparator-1: $\Delta v_{CC1}=v_{C4}-v_{C1}$<br>Input to comparator-2: $\Delta v_{CC2}=v_{C3}-v_{C2}$ | Output states |
|---|---|
| $\Delta v_{CCS} \Rightarrow$ within the control band ($P_{HS}$ - $N_{HS}$) | $C_{SN}$ |
| $\Delta v_{CCS} \geq$ positive limit of the control band ($P_{HS}$) | $C_{SH}$ |
| $\Delta v_{CCS} \leq$ negative limit of the control band ($N_{HS}$) | $C_{SL}$ |

* S=1, 2.

for each pair of dc-link capacitors. It means that, at any given instant, each of the comparators of Fig. 2(a) can output any of the three states, which are listed in Table I. As a result of the combined effects of the two three-state comparators of Fig. 2(a), a total of nine states can be generated, as shown in Table II, which are hereafter referred as Controller States (CSs) "1" to "9." The controller outputs a 4-bit signal [Fig. 2(a)] to uniquely identify these nine CSs. These CSs, in association

TABLE II
CONTROLLER-STATE ASSIGNMENT BASED ON THE UNIQUE COMBINATION OF OUTPUT STATES FOR EACH OF THE THREE-STATE COMPARATORS

| Controller state | Corresponding unique assignment |
|---|---|
| $C_{1N}\ C_{2N}$ | CS "1" |
| $C_{1N}\ C_{2H}$ | CS "2" |
| $C_{1N}\ C_{2L}$ | CS "3" |
| $C_{1H}\ C_{2N}$ | CS "4" |
| $C_{1L}\ C_{2N}$ | CS "5" |
| $C_{1H}\ C_{2H}$ | CS "6" |
| $C_{1H}\ C_{2L}$ | CS "7" |
| $C_{1L}\ C_{2H}$ | CS "8" |
| $C_{1L}\ C_{2L}$ | CS "9" |

with the Sequence (SEQ) signal (as defined in Section V of part I of this paper), are used to select the appropriate redundant switching-state combination, for a particular voltage vector, to achieve dc-link capacitor voltage balancing with closed-loop control.

### *B. Selection of Switching-State Combinations for Closed-Loop Control*

It is clear from Tables I and II that CS "1" represents a normal state of both hysteresis comparators (i.e., $\Delta v_{\rm CC1}$ and $\Delta v_{\rm CC2}$ are within the control band). Hence, CS "1" does not demand any further corrective action, and only the existing balance of capacitor voltages is to be maintained. The open-loop control scheme, which is described in part I of this paper, is best suited for this condition (CS "1"). Therefore, the closed-loop controller switches the switching-state combinations for alternate sampling intervals (i.e., for P_S and N_S durations, as defined in Section V of part I of this paper) for different voltage vectors, as shown in Table III under the column heading CS "1." These switching states are the same as those proposed for open-loop control action, as presented in Table V of part I of this paper. These are chosen in such a way that the average voltage unbalance caused in one sampling interval (P_S duration) gets nullified in the next sampling interval (N_S duration). Hence, in the maximum of two sampling intervals, the alternate switching of selected redundant switching-state combinations for each voltage vector provides balancing condition "$x$, z, $-x$" for the dc-neutral currents (as defined in Section VI of part I of this paper), where $x$ is zero or any nonzero value. As discussed in part I of this paper, these switching-state combinations are selected in such a way that during two-level and three-level modes of operation, the two middle capacitors C3 and C2 [supplied by $V_{\rm dc}/4$, Fig. 1(a)] are only supplying the currents to the machine. Hence, in the two-level and three-level modes of operation of the proposed drive, during CS "1," the voltage balance of the upper and lower capacitors of the dc link [i.e., $\Delta v_{\rm CC1} = v_{C4} - v_{C1}$, Fig. 1(a)] is not at all disturbed.

Now, for CSs "2" to "9" (Table II), which represent the unbalanced condition of two or four capacitor voltages of the dc-link, the redundant switching-state combinations of each voltage vector (as defined in Table I of part I of this paper) are properly utilized. If there is any unbalance sensed in the capacitor voltages, redundant switching-state combinations, which can bring back the capacitor voltages into the balanced condition CS "1" (by producing proper charging or discharging

TABLE III
CHOSEN SWITCHING-STATE COMBINATIONS FOR VOLTAGE VECTORS IN THE 30° SEGMENT OF FIG. 1(b) FOR CLOSED-LOOP CONTROL*

| Voltage Vector and group | Possible combinations of state of comparators 1 and 2 and selection of the switching states for Inverter-A and Inverter-A' (Inv.-A, Inv.-A') | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $C_{1N}C_{2N}$ (CS "1") | | $C_{1N}C_{2H}$ (CS "2") | | $C_{1N}C_{2L}$ (CS "3") | | $C_{1H}C_{2N}$ (CS "4") | | $C_{1L}C_{2N}$ (CS "5") | | $C_{1H}C_{2H}$ (CS "6") | | $C_{1H}C_{2L}$ (CS "7") | | $C_{1L}C_{2H}$ (CS "8") | | $C_{1L}C_{2L}$ (CS "9") | |
| | P_S | N_S | P_S | N_S | P_S | N_S | P_S | N_S | P_S | N_S | P_S | N_S | P_S | N_S | P_S | N_S | P_S | N_S |
| O' (ZV) | 000, 000 | | | | | | | | | | | | | | | | | |
| $A'_1$ (2LV) | 10-1, 000 | 000, -101 | 1-10, 0-11 | | 01-1, -110 | | 10-1, 000 | 000, -101 | 10-1, 000 | 000, -101 | 1-10, 0-11 | | 01-1, -110 | | 1-10, 0-11 | | 01-1, -110 | |
| $B'_1$ (3LV) | 10-1, -101 | | | | | | | | | | 2-20, 0-22 | | 10-1, -101 | | | | 02-2, -220 | |
| $B'_2$ (3LV) | 01-1, -101 | 10-1, 0-11 | 01-1, -101 | 10-1, 0-11 | 01-1, -101 | 10-1, 0-11 | 000, -1-12 | | 11-2, 000 | | 01-1, -101 | 10-1, 0-11 | 01-1, -101 | 10-1, 0-11 | 01-1, -101 | 10-1, 0-11 | 01-1, -101 | 10-1, 0-11 |
| $C'_1$ (4LV) | 20-2, -101 | 10-1, -202 | 20-2, -101 | 10-1, -202 | 20-2, -101 | 10-1, -202 | 2-1-1, -1-12 | | 11-2, -211 | | 20-2, -101 | 10-1, -202 | 20-2, -101 | 10-1, -202 | 20-2, -101 | 10-1, -202 | 20-2, -101 | 10-1, -202 |
| $C'_2$ (4LV) | 2-1-1, 0-22 | 02-2, -211 | 2-1-1, 0-22 | | 02-2, -211 | | 2-1-1, 0-22 | 02-2, -211 | 2-1-1, 0-22 | 02-2, -211 | 2-1-1, 0-22 | | 10-1, -1-12 | | 11-2, -101 | | 02-2, -211 | |
| $D'_1$ (5LV) | 20-2, -202 | | | | | | | | | | | | | | | | | |
| $D'_2$ (5LV) | 11-2, -202 | 20-2, -1-12 | 11-2, -202 | 20-2, -1-12 | 11-2, -202 | 20-2, -1-12 | 11-2, -202 | 20-2, -1-12 | 11-2, -202 | 20-2, -1-12 | 11-2, -202 | 20-2, -1-12 | 20-2, -1-12 | | 11-2, -202 | | 11-2, -202 | 20-2, -1-12 |
| $D'_3$ (5LV) | 11-2, -1-12 | | | | | | | | | | | | | | | | | |

* The corrective states are shown shaded

TABLE IV
EFFECTS OF CORRECTIVE STATES ON THE CHARGING AND DISCHARGING OF DC-LINK CAPACITORS FOR VOLTAGE VECTORS IN THE 30° SEGMENT OF FIG. 1(b) FOR CLOSED-LOOP CONTROL

| Voltage vectors of Fig. 1b and corresponding groups (Table II of part-I of this paper) | Corrective state of Table III | Effect on the dc-link capacitor voltages of Fig. 1a | | | |
|---|---|---|---|---|---|
| | | C1 | C2 | C3 | C4 |
| $A'_1$ (2LV) | 1-10, 0-11 | No effect | Charging | Discharging | No effect |
| | 01-1,-110 | No effect | Discharging | Charging | No effect |
| $B'_1$ (3LV) | 2-20,0-22 | Charging | Charging | Discharging | Discharging |
| | 02-2,-220 | Discharging | Discharging | Charging | Charging |
| $B'_2$ (3LV) | 000,-1-12 | Charging | No effect | No effect | Discharging |
| | 11-2,000 | Discharging | No effect | No effect | Charging |
| $C'_1$ (4LV) | 2-1-1,-1-12 | Charging | No effect | No effect | Discharging |
| | 11-2,-211 | Discharging | No effect | No effect | Charging |
| $C'_2$ (4LV) | 2-1-1,0-22 | Charging | Charging | Discharging | Discharging |
| | 02-2,-211 | Discharging | Discharging | Charging | Charging |
| | 10-1,-1-12 | Charging | Discharging | Charging | Discharging |
| | 11-2,-101 | Discharging | Charging | Discharging | Charging |
| $D'_2$ (5LV) | 20-2,-1-12 | Charging | Discharging | Charging | Discharging |
| | 11-2,-202 | Discharging | Charging | Discharging | Charging |

effect on a particular capacitor or a group of capacitors), are effectively exploited for closed-loop control. These switching-state combinations are hereafter referred to as corrective states. Switching of corrective states may directly bring back the capacitor voltages to the normal state of the controller (CS "1," Table III) or may divert the controller to some other CS [for which, again, the selected corrective states force the capacitor voltages back to the normal state (CS "1")]. The effects of different corrective states (Table III) on the charging and discharging of the dc-link capacitors of Fig. 1(a) for a 30° segment of Fig. 1(b) are shown in Table IV.

As an example, Fig. 2(c) indicates that, for the switching-state combination "2–20, 0–22" of voltage vector $B'_1$ [Fig. 1(b)], the dc-neutral currents "$i_3$, $i_2$, $i_1$" can be equivalently represented as "z, $(-i_A + i_C)$, z" in terms of machine phase currents (as discussed in Table III of part I of this paper). It is evident from Fig. 2(c) (and Table IV) that the switching-state combination "2–20, 0–22" charges capacitor C1 compared to C4 and capacitor C2 compared to capacitors C3 of Fig. 1(a). Therefore, "2–20, 0–22" is used as a corrective state for voltage vector $B'_1$ whenever CS "6" (Table II—C4 is charged more compared to C1, and C3 is charged more compared to C2) is detected in the three-level or four-level mode of operation of the proposed drive [Fig. 1(a)]. In this way, the corrective state "2–20, 0–22" of voltage vector $B'_1$ can bring back the controller from CS "6" to CS "1." It may also happen that because of the corrective action provided by the state "2–20,0–22" of voltage vector $B'_1$ (as per Table IV), capacitor C1 can get overcharged compared to C4 and capacitor C2 can get overcharged compared to capacitor C3. In this case, the closed-loop controller will detect the state CS "9" (Table II—C1 is charged more compared to C4, and C2 is charged more compared to C3). Now, as shown in Table III, for CS "9," the controller selects the corrective state "02–2, −220" (other redundant switching-state combination) of voltage vector $B'_1$. As shown in Table IV, the corrective state "02–2, −1–12" of voltage vector $B'_1$ (Fig. 2(c), with an equivalent representation of "z, $(i_A - i_C)$, z" as per Table III of part I of this paper) helps in bringing back the capacitor voltages into the balanced condition (CS "1") by discharging capacitor C1 compared to C4 and by discharging C2 compared to C3. Hence, "02–2, −220" of voltage vector $B'_1$ can bring back the controller from CS "9" to the balanced condition (i.e., CS "1"). Now, the switching-state combinations shown in Table III for CS "1" (the same for the open-loop control) will be switched by the controller to maintain the existing balance in the capacitor voltages. Corrective states for all the other voltage vectors of Fig. 1(b) for different CSs are found in a similar way. Table III shows the chosen redundant

switching-state combinations for the 30° segment $D_1'O'D_3'$ of Fig. 1(b) for closed-loop control, in which the available corrective state are shown shaded.

It is evident from Table III that, to speed up the balancing action, for a particular CS, the controller switches the same available corrective state continuously (in P_S and N_S duration, Table III) for any given voltage vector until some other CS is detected. On the other hand, if any voltage vector does not possess the appropriate corrective state, then the switching states used in CS "1" for that voltage vector are switched for consecutive P_S and N_S durations (Table III). This prevents further divergence of capacitor voltages and, hence, helps the available corrective states of other voltage vectors in taking corrective action for that CS. While selecting the corrective states for the proposed closed-loop control scheme, efforts are made to ensure the availability of at least one corrective state for each CS (CS "2" to CS "9") among the vectors switched during each level of operation. For example, as shown in Table III, the corrective states of voltage vectors $A_1'$, $B_1'$, and $B_2'$ cover all the possible CSs (CS "2" to "9") for three-level mode of operation. Similarly, the corrective states of voltage vectors $C_1'$, $C_2'$, and $D_2'$ cover all the CSs (CS "2" to "9") for five-level mode of operation. Hence, the corrective states provide capacitor voltage balancing in all five levels of linear operation and overmodulation mode of operation. The switching states for all other voltage vectors of Fig. 1(b), for the closed-loop control, are found in a similar way. Proper care is also taken while choosing all the switching-state combinations for the closed-loop control to ensure that all the pole voltages remain identical (with proper phase shift) for all the operating conditions of the drive.

## III. Simulation Studies of the Closed-Loop Control Scheme

A detailed simulation study of the proposed closed-loop control scheme for the entire operating range of the drive is carried out before the actual implementation. It can be seen from the simulation results of Fig. 3 that during the balanced condition of the capacitor voltages [$v_{C2}$ and $v_{C3}$ in Fig. 3(a), and $v_{C1}$ and $v_{C4}$ in Fig. 3(b)], the controller outputs the state CS "1" [Fig. 3(e)]. During this time, the CMV is eliminated, as shown in Fig. 3(d). When the closed-loop controller is disabled, a gradual divergence in the dc-link-capacitor voltages is clearly observed [$v_{C2}$ and $v_{C3}$ in Fig. 3(a), and $v_{C1}$ and $v_{C4}$ in Fig. 3(b)]. Once it is enabled again, the controller brings back the capacitor voltages back to the normal state (CS "1") by taking corrective action, as per Table III, through different CSs [Fig. 3(e)]. The CMV visible in Fig. 3(d) is mainly because of the disabled controller and unbalanced voltages of the dc-link capacitors. The CMV gets eliminated immediately when the controller is brought into action again [Fig. 3(e)]. Similar results are obtained for the operation of the proposed drive in the two-level, three-level, and four-level modes of operation, also, in the linear range of the drive.

Any drive system should be able to operate also in the overmodulation mode whenever required, based on the demand from load side or to take care of the input voltage fluctuations.

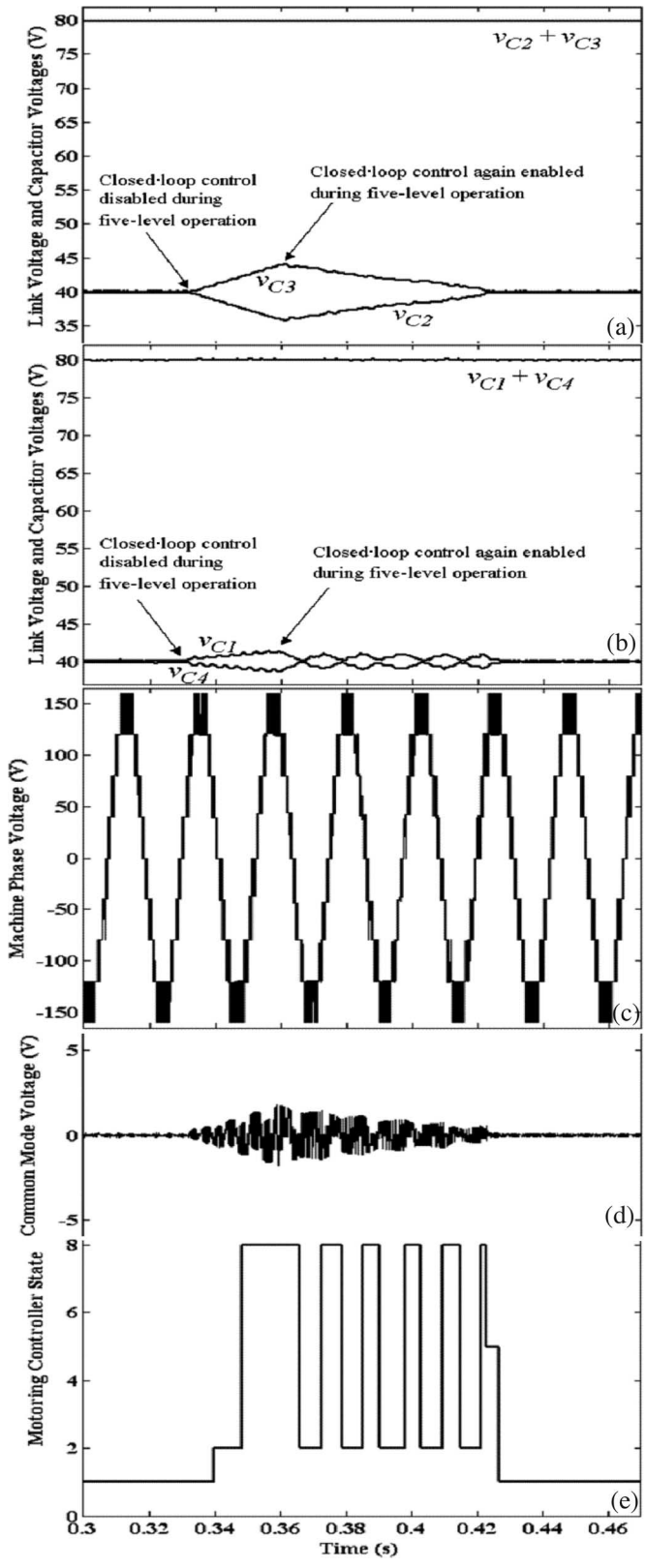



Fig. 3. Capability of closed-loop controller to eliminate the CMV and to bring back the capacitor voltages into the balanced condition during five-level mode of operation (simulation results).

For the proposed drive, in the overmodulation range, the inverter voltage vectors belonging to the 5LV group (Table II, part I of this paper) are switched for more time when compared

to the inverter voltage vectors of the 4LV group, in a sampling interval. Now, as indicated in Table III, for the overmodulation range, most of the corrective states are being provided by the voltage vectors belonging to the 4LV group (e.g., $C_1'$ and $C_2'$ for the 30° segment of Fig. 1(b), and the corrective states contributed by the 5LVgroup are less and limited for certain CSs only [e.g., $D_2'$ for the 30° segment of Fig. 1(b)]. Hence, it is obvious that the controller may take a longer time to bring back the capacitor voltages to the balanced state (CS "1") during overmodulation operation when compared to that during five-level mode of operation. This way, however, the time taken by the closed-loop controller to come back to CS "1" slightly increases with increase in overmodulation for the same amount of unbalance in capacitor voltages. This fact is verified by the simulation results provided in Fig. 4. It can be seen from the different results of Fig. 4 that the proposed closed-loop controller is also able to achieve dc-link capacitor voltage balancing with CMV elimination in the overmodulation mode, which is similar to five-level mode of operation in the linear range (Fig. 3). Thus, the proposed closed-loop controller scheme can simultaneously eliminate the CMV and balance the dc-link-capacitor voltages throughout the operating range of the drive by properly utilizing the redundant switching-state combinations. In the present paper, the five-level inverter is formed by cascading two conventional two-level inverters and a three-level NPC inverter [Fig. 1(a)]; thus, it provides a simple power-bus structure for the implementation. However, the proposed control scheme can be used for any five-level-inverter configuration (NPC, flying capacitor, etc.) with an open-end winding IM structure. In the proposed closed-loop control scheme, the redundant switching-state selection will have opposite effects on the charging and discharging of the dc-link capacitors, during regenerative mode [18]. Thus, in regenerative mode of operation, the corrective states are to be interchanged, with respect to the CSs in motoring mode [20]. Detailed simulation studies of this are presented in [18] and [12].

## IV. Experimental Results and Discussion

The proposed five-level-inverter scheme [Fig. 1(a)] is tested on a laboratory prototype of a 1.5-kW open-end winding IM drive with voltage/frequency control. The digital-signal-processing tool TI TMX320F240PQ and the CPLD XILINX XC95108-20PC84C are used for implementing the proposed closed-loop control scheme, as shown in Fig. 5(a). A total of four Hall-effect voltage sensors (type LEM LV 20-P) are used to sense the voltages of the dc-link capacitor. The dc-link voltage of about 120 V is used for the inverter; thus, the individual dc-link-capacitor voltages are about 30 V. The carrier frequency used for PWM generation is limited to 1.25 kHz. The performance of the drive is verified for steady-state and transient operating conditions at different modulation indexes, covering the entire speed range.

The machine phase-voltage and common-mode current waveforms for inverter operation in linear and overmodulation range are presented in Fig. 5(b) and (c), respectively. The balancing of dc-link-capacitor voltages and elimination of CMV in the steady-state operation of the drive are evident from the waveforms of Fig. 5(b) and (c). Similar results of phase-voltage and common-mode current waveforms are obtained for other operating levels in the linear range of the proposed drive.

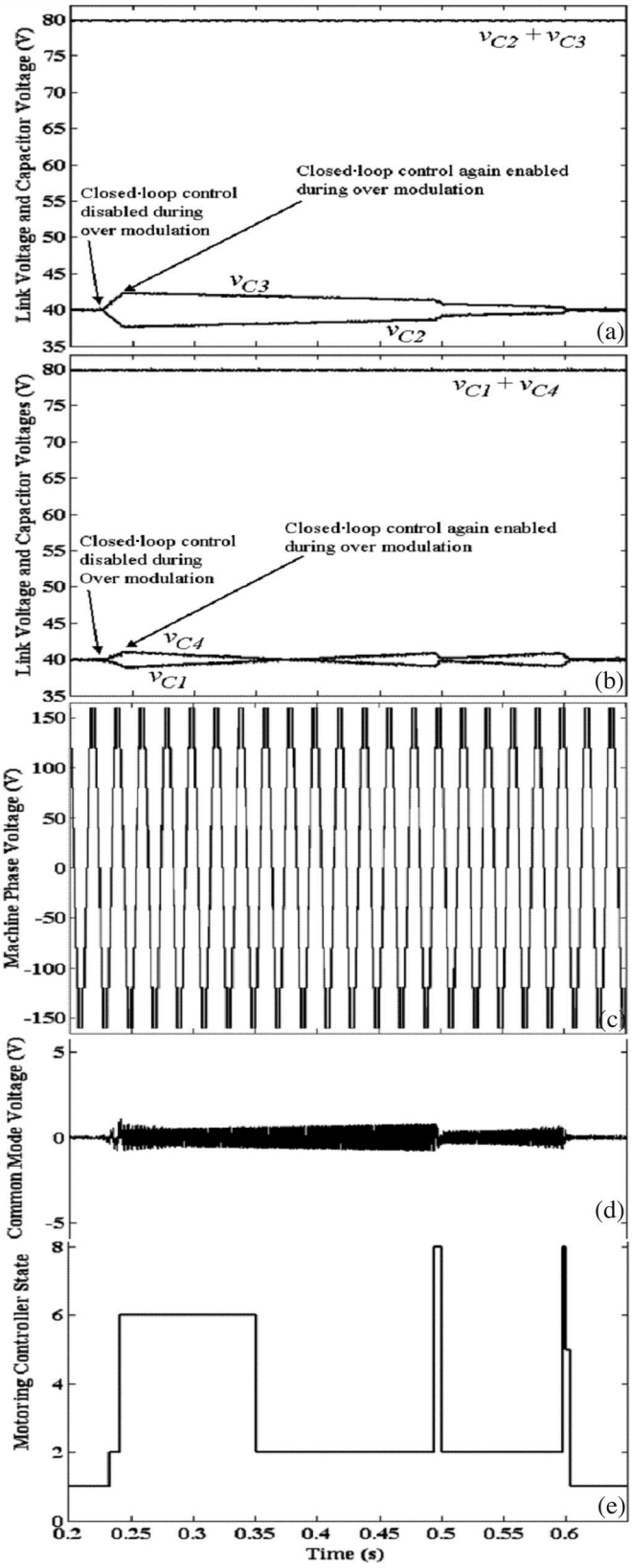
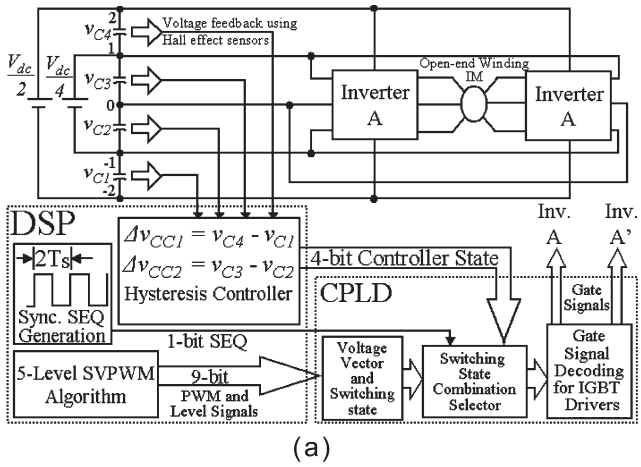



Fig. 4. Capability of closed-loop controller to eliminate the CMV and to bring back the capacitor voltages into the balanced condition during the overmodulation range (simulation results).



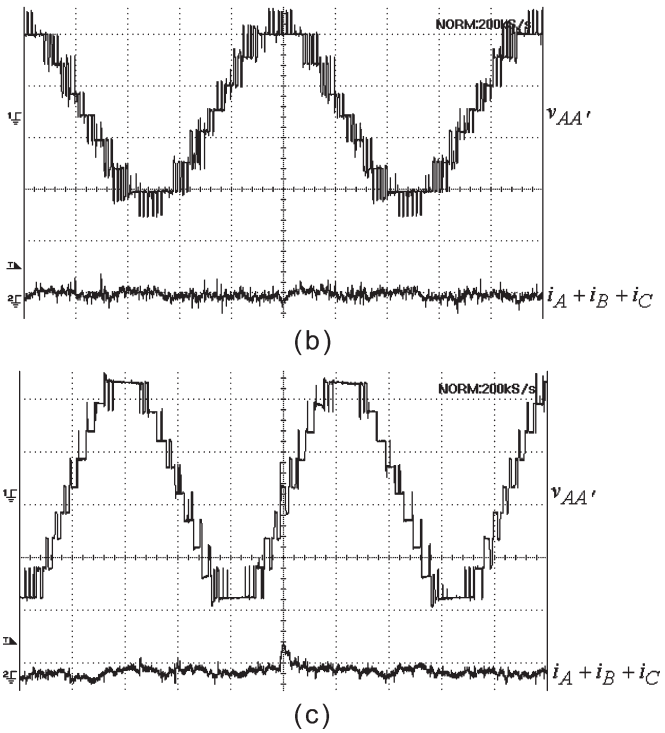




Fig. 5. (a) Block schematic of the hysteresis-comparator-based closed-loop control scheme for the proposed dual five-level-inverter-fed IM drive. (b) Machine phase voltage $v_{AA'}$ and common-mode current $i_A + i_B + i_C$ during the balanced condition of capacitor voltages in five-level mode of operation [$Y$-axis: (upper trace) 1 div = 50 V and (lower trace) 1 div = 2 A, $X$-axis: 1 div = 5 ms]. (c) Machine phase voltage $v_{AA'}$ and common-mode current $i_A + i_B + i_C$ during the balanced condition of capacitor voltages in overmodulation range of operation [$Y$-axis: (upper trace) 1 div = 50 V and (lower trace) 1 div = 2 A, $X$-axis: 1 div = 5 ms].

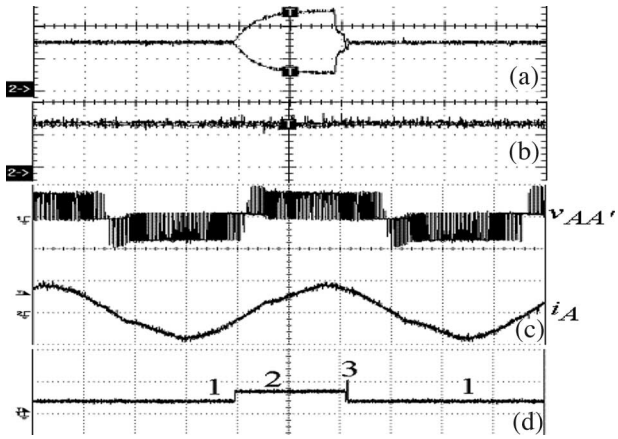



Fig. 6. With controller disabled and enabled again in two-level operation: (a) capacitor voltages $v_{C2}$ and $v_{C3}$ [$Y$-axis: 1 div = 20 V, $X$-axis: 1 div = 500 ms], (b) capacitor voltages $v_{C1}$ and $v_{C4}$ [$Y$-axis: 1 div = 20 V, $X$-axis: 1 div = 500 ms], (c) machine phase voltage $v_{AA'}$ and machine phase current $i_A$ during the balanced condition [$Y$-axis: (upper trace) 1 div = 33 V and (lower trace) 1 div = 2 A, $X$-axis: 1 div = 20 ms], and (d) the states of the controller.

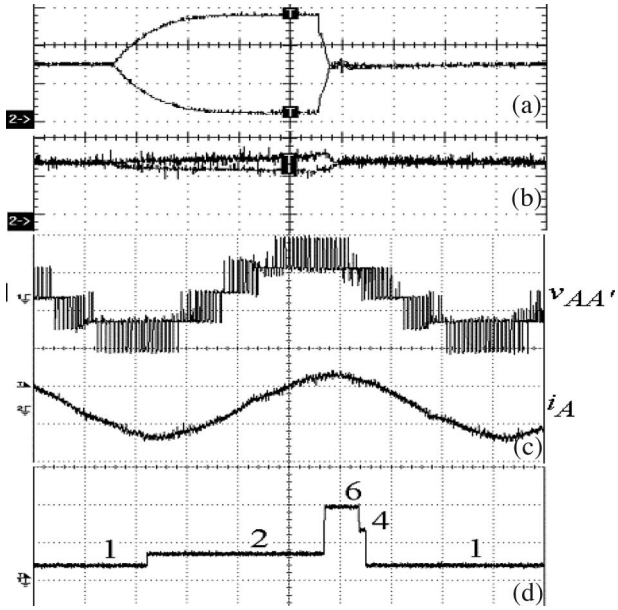



Fig. 7. With the controller disabled and enabled again in three-level operation: (a) capacitor voltages $v_{C2}$ and $v_{C3}$ [$Y$-axis: 1 div = 20 V, $X$-axis: 1 div = 500 ms], (b) capacitor voltages $v_{C1}$ and $v_{C4}$ [$Y$-axis: 1 div = 20 V, $X$-axis: 1 div = 500 ms], (c) machine phase voltage $v_{AA'}$ and machine phase current $i_A$ during balanced condition [$Y$-axis: (upper trace) 1 div = 33 V and (lower trace) 1 div = 2 A, $X$-axis: 1 div = 10 ms], and (d) the states of the controller.

The traces of dc-link-capacitor voltages ($v_{C2}$ and $v_{C3}$, and $v_{C1}$ and $v_{C4}$), machine phase voltage $(v_{AA'})$, machine phase current $(i_A)$, and states of the closed-loop controller are presented in Figs. 6–11, for different steady-state and transient operating conditions of the drive. The voltage control band for each comparator of Fig. 2(b) is set to 3 V. In two-level mode of operation, during the balanced condition of capacitor voltage [$v_{C2}$ and $v_{C3}$ in Fig. 6(a), and $v_{C1}$ and $v_{C4}$ in Fig. 6(b)], the controller outputs CS "1" [Fig. 6(d)]. When the closed-loop controller is disabled, a gradual divergence in voltages of the two inner capacitors ($v_{C2}$ and $v_{C3}$) is observed [Fig. 6(a)]. Now, the controller outputs CS "2" ($C_{1N}\ C_{2H}$, Table III). The corrective action taken by the controller is seen by the convergence of capacitor voltages $v_{C2}$ and $v_{C3}$, when the controller is enabled again [Fig. 6(a)]. This leads the system back to the balanced state of capacitor voltages (CS "1"), momentarily through CS "3," as shown in Fig. 6(d). Similar results of capacitor voltage balancing for higher speed range operations of the drive are shown in Figs. 7–10. Fig. 11 shows the transient performance of the proposed scheme during speed reversal of the drive. In Fig. 11(a), the waveforms of the machine phase voltage (upper trace) and the machine phase current (lower trace) show the smooth transitions of the operating levels of the inverter

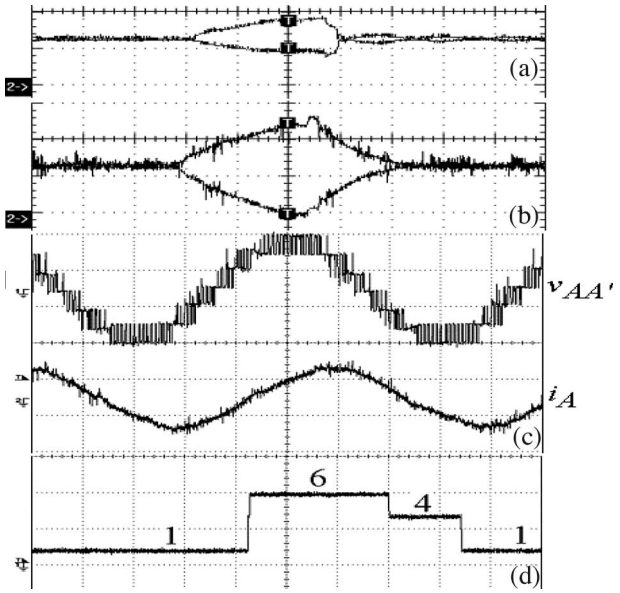



Fig. 8. With the controller disabled and enabled again in four-level operation: (a) capacitor voltages $v_{C2}$ and $v_{C3}$ [$Y$-axis: 1 div = 20 V, $X$-axis: 1 div = 500 ms], (b) capacitor voltages $v_{C1}$ and $v_{C4}$ [$Y$-axis: 1 div = 20 V, $X$-axis: 1 div = 500 ms], (c) machine phase voltage $v_{AA'}$ and machine phase current $i_A$ during balanced condition [$Y$-axis: (upper trace) 1 div = 50 V and (lower trace) 1 div = 2 A, $X$-axis: 1 div = 5 ms], and (d) the states of the controller.

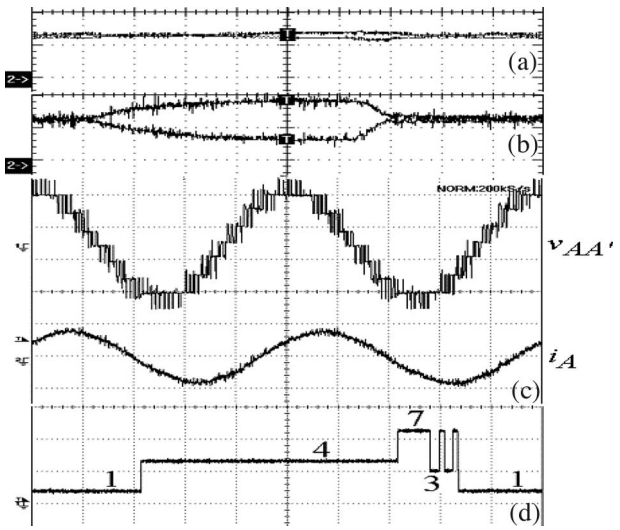



Fig. 9. With the controller disabled and enabled again in five-level operation: (a) capacitor voltages $v_{C2}$ and $v_{C3}$ [$Y$-axis: 1 div = 20 V, $X$-axis: 1 div = 500 ms], (b) capacitor voltages $v_{C1}$ and $v_{C4}$ [$Y$-axis: 1 div = 20 V, $X$-axis: 1 div = 500 ms], (c) machine phase voltage $v_{AA'}$ and machine phase current $i_A$ during balanced condition [$Y$-axis: (upper trace) 1 div = 50 V and (lower trace) 1 div = 2 A, $X$-axis: 1 div = 5 ms], and (d) the states of the controller.

during speed reversal. Fig. 11(b) shows that C2 and C3 [Fig. 1(a)] share the equal voltage, while equal sharing of voltage between C1 and C4 [Fig. 1(a)] is evident in Fig. 11(c). It is also clear from Fig. 11(b) and (c) that all the four capacitors of the dc-link share the equal voltage throughout the operating range of the drive. Hence, the closed-loop switching-state combinations (Table III) are able to keep the controller in its normal state, i.e., CS "1" [Fig. 11(d)] throughout the transient operations. It is quite evident from all the experimental results

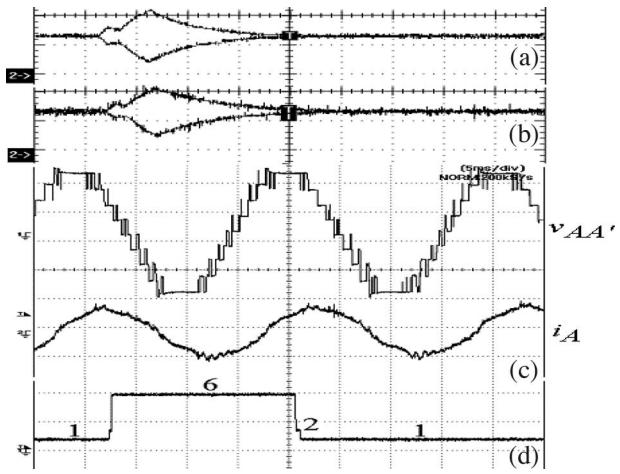



Fig. 10. With the controller disabled and enabled again in overmodulation operation: (a) capacitor voltages $v_{C2}$ and $v_{C3}$ [$Y$-axis: 1 div = 20 V, $X$-axis: 1 div = 1 s], (b) capacitor voltages $v_{C1}$ and $v_{C4}$ [$Y$-axis: 1 div = 20 V, $X$-axis: 1 div = 1 s], (c) machine phase voltage $v_{AA'}$ and machine phase current $i_A$ during balanced condition [$Y$-axis: (upper trace) 1 div = 50 V and (lower trace) 1 div = 2 A, $X$-axis: 1 div = 5 ms], and (d) the states of the controller.

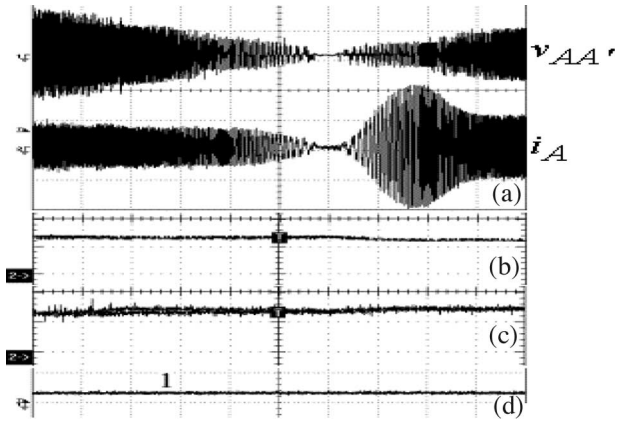



Fig. 11. Speed reversal in five-level operation: (a) machine phase voltage $v_{AA'}$ and machine phase current $i_A$ [$Y$-axis: (upper trace) 1 div = 50 V and (lower trace) 1 div = 2 A, $X$-axis: 1 div = 2 s], (b) capacitor voltages $v_{C2}$ and $v_{C3}$ [$Y$-axis: 1 div = 20 V, $X$-axis: 1 div = 2 s], (c) capacitor voltages $v_{C1}$ and $v_{C4}$ [$Y$-axis: 1 div = 20 V, $X$-axis: 1 div = 2 s], and (d) the states of the controller.

of Figs. 5–11 that the proposed closed-loop controller is able to maintain the dc-link capacitor voltage balancing in association with CMV elimination throughout the operating range of the drive in steady-state and transient operating conditions in both rotation directions of the machine.

## V. Conclusion

A dual five-level inverter-fed IM drive is proposed for the dual task of CMV elimination and dc-link capacitor voltage balancing for the entire modulation range. A simple closed-loop control scheme, based only on the switching-state redundancy, is proposed as a solution to the operating limitation of the open-loop control scheme, which was presented in part I of this paper. The present scheme has the capability of maintaining the capacitor-voltage balance and can also provide the corrective action, if there happens to be any unbalance in the capacitor

voltages during different dynamic operating conditions of the drive. Effective utilization of redundant switching-state combinations of the inverter voltage vectors eliminates the need for extra hardware to achieve capacitor voltage balancing, without affecting the fundamental output voltage of the inverter. Simulations and experimental results show the capability of the proposed scheme to provide the balancing of dc-link capacitor voltages and CMV elimination for the entire operating range of the drive.

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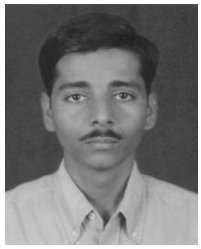
**P. N. Tekwani** (S'04) received the B.E. degree (Uni. First) in power electronics from Lukhdhirji Engineering College, Morbi, India, in 1995, and the M.E. degree in electrical engineering (First Rank) from the Maharaja Syajirao University of Baroda, Vadodara, India, in 2000. He is currently working toward the Ph.D. degree at the Centre for Electronics Design and Technology, Indian Institute of Science, Bangalore, India.

He was with Amtech Electronics Pvt. Ltd., Gandhinagar, India, from 1995 to 1996. From 1996 to 2001, he was with the Electrical Research and Development Association, Vadodara. Since 2001, he has been a member of the Faculty at the Nirma Institute of Technology, Ahmedabad, India.



**R. S. Kanchan** (S'04) received the B.E. degree in electrical engineering from Walchand College of Engineering, Sangali, India, in 1998, the M.Tech. degree in electrical engineering from the Indian Institute of Technology, Bombay, India, in 2000, and the Ph.D. degree from the Indian Institute of Science, Bangalore, India, in 2005.

He was with Tata Steel Company from 2000 to 2002. Currently, he is a Research Associate at the Centre for Electronics Design and Technology, Indian Institute of Science.

**K. Gopakumar** (M'94–SM'96) received the B.E., M.Sc.(Eng.), and Ph.D. degrees from the Indian Institute of Science, Bangalore, India, in 1980, 1984, and 1994, respectively.

He was with the Indian Space Research Organization from 1984 to 1987. He is currently an Associate Professor at the Centre for Electronics Design and Technology, Indian Institute of Science. His fields of interest include power converters, PWM techniques, and ac drives.

Dr. Gopakumar is an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS.