[12] Kelly, E. J. (1986)
An adaptive detection algorithm.
IEEE Transactions on Aerospace and Electronic Systems, **AES-22** (1986), 115–127.

[13] Horn, R. A., and Johnson, C. R. (1985)
Matrix Analysis.
New York: Cambridge University Press, 1985.

Analysis and Design of (LC)(LC)-Type Series-Parallel Resonant Converter

A series-parallel resonant converter employing (LC)(LC)-type tank circuit operating in lagging power factor (PF) mode is presented and analyzed using complex ac circuit analysis. Design curves are obtained and the converter is optimized under certain constraints. Detailed Space Integrated Control Experiment (SPICE) simulation results are presented to evaluate the performance of the designed converter under varying load conditions. Results obtained from an experimental converter are also presented. The results obtained from the theory, SPICE simulation, and the experimental converter are compared. The proposed converter has high efficiency from full load to very light load (< 10%). Switching frequency variation required for a wide change in the load (near load open circuit to full load) is narrow compared with the series resonant converter (SRC).

I. INTRODUCTION

A number of high-frequency (HF) resonant converter configurations have been reported in the literature [1–15]. Series resonant converter (SRC) is the simplest and most well documented configuration [1]. SRCs have high efficiency from full load to part load. But the major disadvantage of the SRC is the difficulty in regulating the converter output voltage at light loads, i.e., they require very wide variation in switching frequency for load regulation.

In an attempt to improve the performance of resonant converters, higher order resonant converters have been proposed (e.g. [3–15]). It has been shown by a number of authors that the LCC-type parallel resonant converter (also called as series-parallel resonant converter [3–6]) has a number of desirable features compared with other resonant converter configurations. Although this converter has good efficiency from full load to about 50% load, its efficiency falls for loads below about 50% of rated load since the converter takes the properties of the parallel resonant converter. This is because the peak current through the HF switches does not decrease in proportion to the load for load currents below about 50% of full load. A modified (LCL-type) SRC presented in [15] has very good characteristics (viz., high efficiency and narrow variation in switching frequency for load regulation), but has higher voltage stress on the output rectifier diodes.

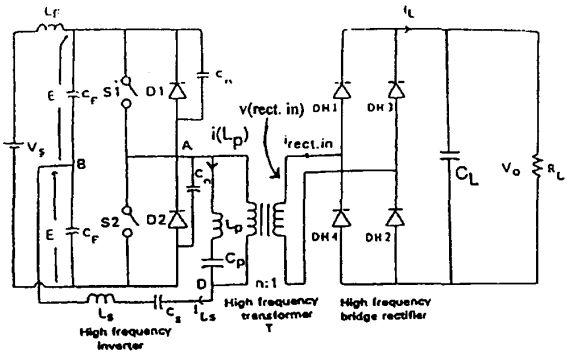

Fig. 1. Basic circuit diagram of (LC)(LC)-type series-parallel resonant converter suitable for operation in lagging PF mode. (Note: S1 and S2 are HF switches capable of base or gate turn-off capability).

Fig. 1 shows the circuit diagram of the proposed (LC)(LC)-type series-parallel converter. This converter was first proposed for telecommunication applications in [7] and the converter was operated below resonance (leading power factor (PF) mode). This type of operation resulted in audible noise and reduced efficiency. These problems can be overcome by operating the converter in above resonance (lagging PF) mode [5] and optimizing the converter design. Therefore, the objectives of this work are to present a detailed analysis, to obtain design curves for lagging PF mode of operation, to select the component values for an optimized converter, and to present detailed simulation and experimental results for the proposed converter.

The layout is as follows. Section II presents the operation of the converter. The converter is analyzed using complex ac circuit analysis in Section III. The design procedure is illustrated by a design example in Section IV. The converter is optimized under certain constraints. The converter designed in Section IV is simulated using the Space Integrated Circuit Experiment (SPICE) simulation program in Section V. Detailed experimental results obtained from a 100 W experimental converter are presented in Section VI to verify the theory.

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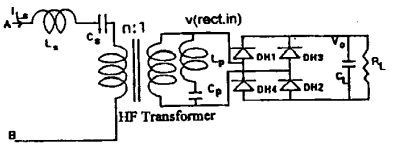
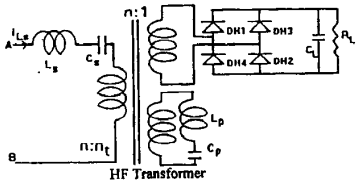


(a)



(b)

Fig. 2. Alternate possible connections of parallel resonant branch in Fig. 1. Parallel branch placed on (a) secondary-side of HF transformer, (b) on tertiary winding.

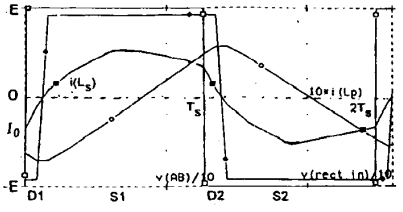


Fig. 3. Typical operating waveforms to illustrate lagging PF mode of operation for converter shown in Fig. 1.

II. OPERATING PRINCIPLE

Fig. 1 shows the basic circuit diagram of (LC)(LC)-type series-parallel resonant converter. Capacitive output filter is used. One can also place the parallel resonant circuit (L_pC_p) either on the secondary-side (Fig. 2(a)) of the HF transformer or on a tertiary-winding (Fig. 2(b)). With these arrangements, the leakage inductances of the HF transformer can be utilized as part of resonating inductor(s). The operating principle of the converter can be understood by referring to the typical operating waveforms (obtained from SPICE simulation) shown in Fig. 3. The converter is operated in the lagging PF mode (above resonance mode) with D1 (or D2) conducting prior to the turn-on of S1 (or S2) resulting in zero voltage turn-on of S1 and S2. The voltage input at the rectifier input terminals is nearly a square-wave with an amplitude nearly equal to the output load voltage.

III. STEADY-STATE ANALYSIS

In this section, the (LC)(LC)-type series-parallel resonant converter is analyzed using complex ac circuit analysis method [5, 9]. This approach gives good design values as verified in this work. Expressions for the converter gain and component ratings are derived in this section. Once the converter is designed at full load using this simple analysis, its performance can be evaluated using SPICE simulation as done in Section V.

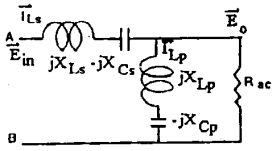


Fig. 4. Phasor circuit model used for analysis of (LC)(LC)-type converter shown in Fig. 1. (Note: X_{Ls}, X_{Cs}, X_{Lp}, X_{Cp} are reactances of L_s, C_s, L_p, and C_p, respectively.)

A. Assumptions Used

The following assumptions are made in the analysis presented in this work.

1) The switches, diodes, inductors, capacitors, and snubber components are ideal.
2) The effect of snubbers is neglected.
3) The HF transformer is ideal.
4) The input voltage to the resonant circuit is represented by the fundamental component of voltage across AB. Similarly, only fundamental component of the voltage at the input of the rectifier is taken into consideration.

B. Modeling of the Converter

The rectifier-filter-load block in Figs. 1 and 2 can be replaced by an equivalent ac resistance [5, 9], R_{ac}, considering the fundamental components of the waveforms (assumption 4). The value of R_{ac} is given by [5, 9]

$$R_{ac} = (8/\pi^2)R'_L\ \Omega \tag{1}$$

where R'_L is the primary-side reflected load resistance given by

$$R'_L = n^2R_L\ \Omega. \tag{2}$$

Fig. 4 shows the phasor circuit model used for the analysis. Based on this model, the steady-state analysis of the converter using complex ac circuit analysis is presented in the next section.

C. Analysis

All the equations presented are normalized using the base quantities:

$$V_B = E, \qquad Z_B = R'_L, \qquad I_B = V_B/Z_B. \tag{3}$$

The normalized quantities are represented by additional subscript "pu".

Following the procedure presented in [5, 9] and using complex circuit analysis in Fig. 4, it can be shown that the output voltage of the converter referred to the primary-side (i.e., converter gain) is given by

$$M = 1/[(X_{spu}/K)2 + (1 + X_{spu}/X_{ppu})^2]^{1/2} \text{ p.u.} \tag{4}$$

where

$$K = 8/\pi^2 \tag{5}$$

$$X_{spu} = Q_s f_{ssn} - Q_s/f_{ssn} \text{ p.u.} \tag{6}$$

$$X_{ppu} = Q_p f_{spn} - Q_p/f_{spn} \text{ p.u.} \tag{7}$$

$$Q_s = (L_s/C_s)^{1/2}/R'_L \tag{8}$$

$$f_{ssn} = \omega_s/\omega_{sr} = f_s/f_{sr} \tag{9}$$

$$\omega_{sr} = 1/(L_s C_s)^{1/2} \text{ rad/s} \tag{10}$$

$$Q_p = (L_p/C_p)^{1/2}/R'_L = Q_s(L_p/L_s)^{1/2}(C_s/C_p)^{1/2} \tag{11}$$

$$f_{spn} = f_s/f_{pr} = \omega_s/\omega_{pr} = f_{ssn}(L_p/L_s)^{1/2}(C_p/C_s)^{1/2} \tag{12}$$

$$\omega_{pr} = 1/(L_p C_p)^{1/2} \text{ rad/s} \tag{13}$$

and f_s is the switching frequency.

The equivalent impedance Z_{eq} (in per unit) looking into the terminals AB is given by

$$Z_{eqpu} = [B_1 + jB_2] \text{ p.u.} \tag{14}$$

where

$$B_1 = (1/K)(1/D) \tag{15}$$

$$B_2 = X_{spu} + (1/X_{ppu})(1/D) \tag{16}$$

$$D = (1/K^2) + (1/X_{ppu}^2). \tag{17}$$

The inverter output peak current (same as the switch peak current) is given by

$$I_{Lsppu} = 4/[\pi \mid Z_{eqpu}\mid] \text{ p.u.} \tag{18}$$

The per unit value of the initial current I_0 (at $t = 0$, Fig. 3) is given by

$$I_{0pu} = I_{Lsppu}\sin(-\phi) \text{ p.u.} \tag{19}$$

where

$$\phi = \tan^{-1}[B_2/B_1] \text{ rads.} \tag{20}$$

The peak voltage across the capacitor C_s, the peak current through the parallel branch (i.e., through inductor L_p and capacitor C_p), and the peak voltage across C_p are

$$V_{Csppu} = X_{Cspu} \cdot I_{Lsppu} \text{ p.u.} \tag{21}$$

$$I_{Lpppu} = I_{Lsppu}/[1 + (X_{ppu}/K)^2]^{1/2} \text{ p.u.} \tag{22}$$

$$V_{Cpppu} = X_{Cppu} \cdot I_{Lpppu} \text{ p.u.} \tag{23}$$

IV. DESIGN

Using the analysis presented in Section III, design curves are obtained for various ratios of L_s/L_p and C_s/C_p. This is illustrated by a design example. The specifications of the half-bridge converter design are: input supply voltage $2E = 100$ V, output power $P_0 = 100$ W, load voltage $V_0 = 48$ V, switching frequency $f_s = 100$ kHz.

The total kVA rating of the tank circuit per kW of output power, converter gain (M,p.u.), and inverter output peak current, with variation in f_{ssn} (ratio of switching frequency to series resonance frequency) are plotted in Figs. 5(a)–(c) for different ratios of L_s/L_p and C_s/C_p. These curves are obtained for maximum power output condition and for lagging PF mode of operation. I_0 (using (19)) must be negative for lagging PF mode of operation.

The converter is optimized for 1) minimum kVA rating of tank circuit per kW of output power, 2) minimum inverter output peak current, and 3) minimum variation in switching frequency for full load to no load voltage regulation.

It can be observed that for a given Q_s and f_{ssn}, as the value of L_s/L_p increases (Fig. 5(a1)–(a3)), kVA/kW rating of the tank circuit increases (i.e., tank circuit size increases). However, the switching frequency variation required for voltage regulation decreases (Fig. 5(b1)–(b3)). For low inverter output peak current (same as the switch peak current), switching frequency must be nearly equal to the series resonance frequency (with some margin for ensuring enough turn-off time for the switches), i.e., f_{ssn} must be nearly equal to 1 (Fig. 5(c1)–(c3)). Lower inverter output peak current increases the efficiency of the converter. In addition, it can be observed that the kVA/kW rating decreases with the value of Q_s. This also decreases the inverter output peak current at full load.

Based on the optimization constraints and the observations made from the design curves, the following values were selected in the design example:

$$L_s/L_p = 0.1, \qquad C_s/C_p = 2,$$
$$Q_s = 1, \qquad f_{ssn} = 1.05.$$

The normalized output voltage (using (4) or Fig. 5(b2)) at full load is

$$M = 0.9818 \text{ p.u.}$$

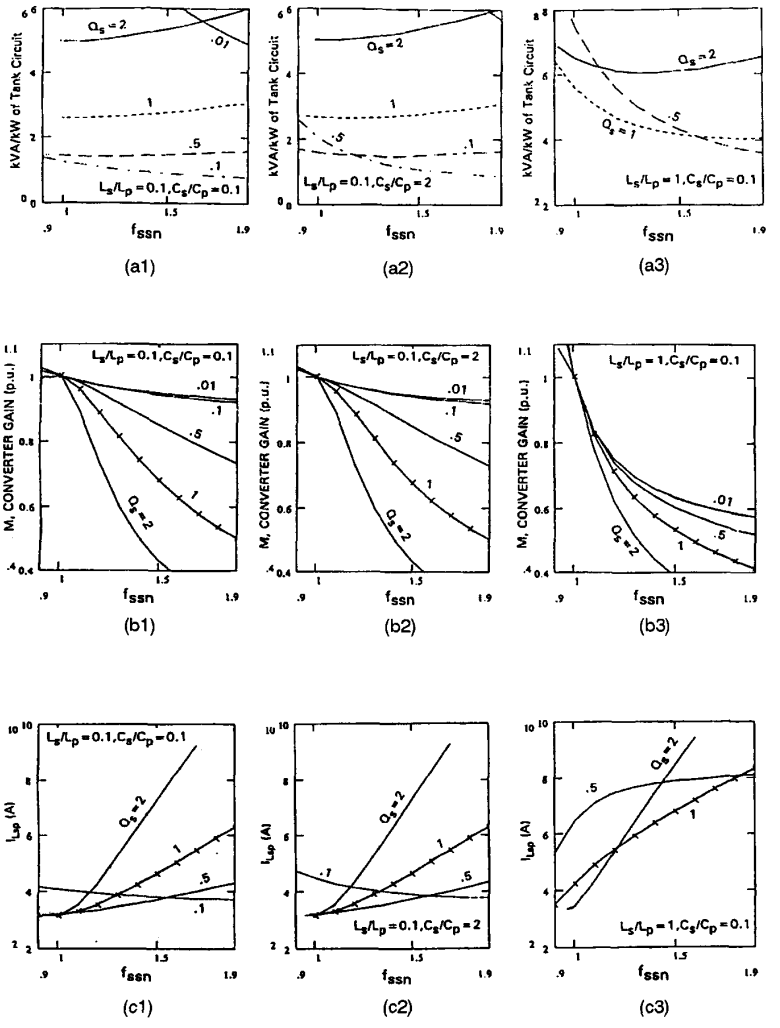


Fig. 5. Design curves obtained for the design example. (a) Total kVA rating of tank circuit per kW of output power for variation in normalized switching frequency, f_{ssn} (ratio of switching frequency to series resonance frequency) for various inductor and capacitor ratios, (a1) $L_s/L_p = 0.1$, $C_s/C_p = 0.1$, (a2) $L_s/L_p = 0.1$, $C_s/C_p = 2$, (a3) $L_s/L_p = 1$, $C_s/C_p = 0.1$. (b) Converter gain M (p.u.) versus f_{ssn} for various inductor and capacitor ratios. (c) Inverter output peak current (I_{Lsp},A) versus f_{ssn} for various inductor and capacitor ratios for designed 100 W converter.

The base values given by (3) are used. Then,

$$V_0' = 49.1 \text{ V} \quad \text{and} \quad R_L' = 24.1\ \Omega.$$

Therefore, the HF transformer turns ratio, $n \cong 1$.

The values of L_s and C_s are calculated by solving

$$(L_s/L_p)^{1/2} = Q_s \times R_L' = 1 \times 24.1\ \Omega$$

$$\omega_{sr} = 1/(L_sC_s)^{1/2} = 2\pi f_s/f_{ssn}$$

$$= 2\pi \times 100{,}000/1.05 \text{ rad/s}.$$

Solution of the above equations gives

$$L_s = 40{,}27\ \mu\text{H} \quad \text{and} \quad C_s = 0.069\ \mu\text{F}.$$

Since $L_s/L_p = 0.1$ and $C_s/C_p = 2$ are chosen,

$$L_p = 402.7\ \mu\text{H} \quad \text{and} \quad C_p = 0.0345\ \mu\text{F}.$$

The peak value of current to be carried by the switches, the inductor L_s, and the capacitor C_s at full load is given by (18),

$$I_{Lsp} = 3.21 \text{ A}.$$

The peak voltage across L_s, the peak current through L_p, and the peak voltage across C_p (using (21)–(23)) are approximately given by

$$V_{Csp} = 73.8 \text{ V}, \quad I_{Lpp} = 0.213 \text{ A}, \quad V_{Cpp} = 13.9 \text{ V}.$$

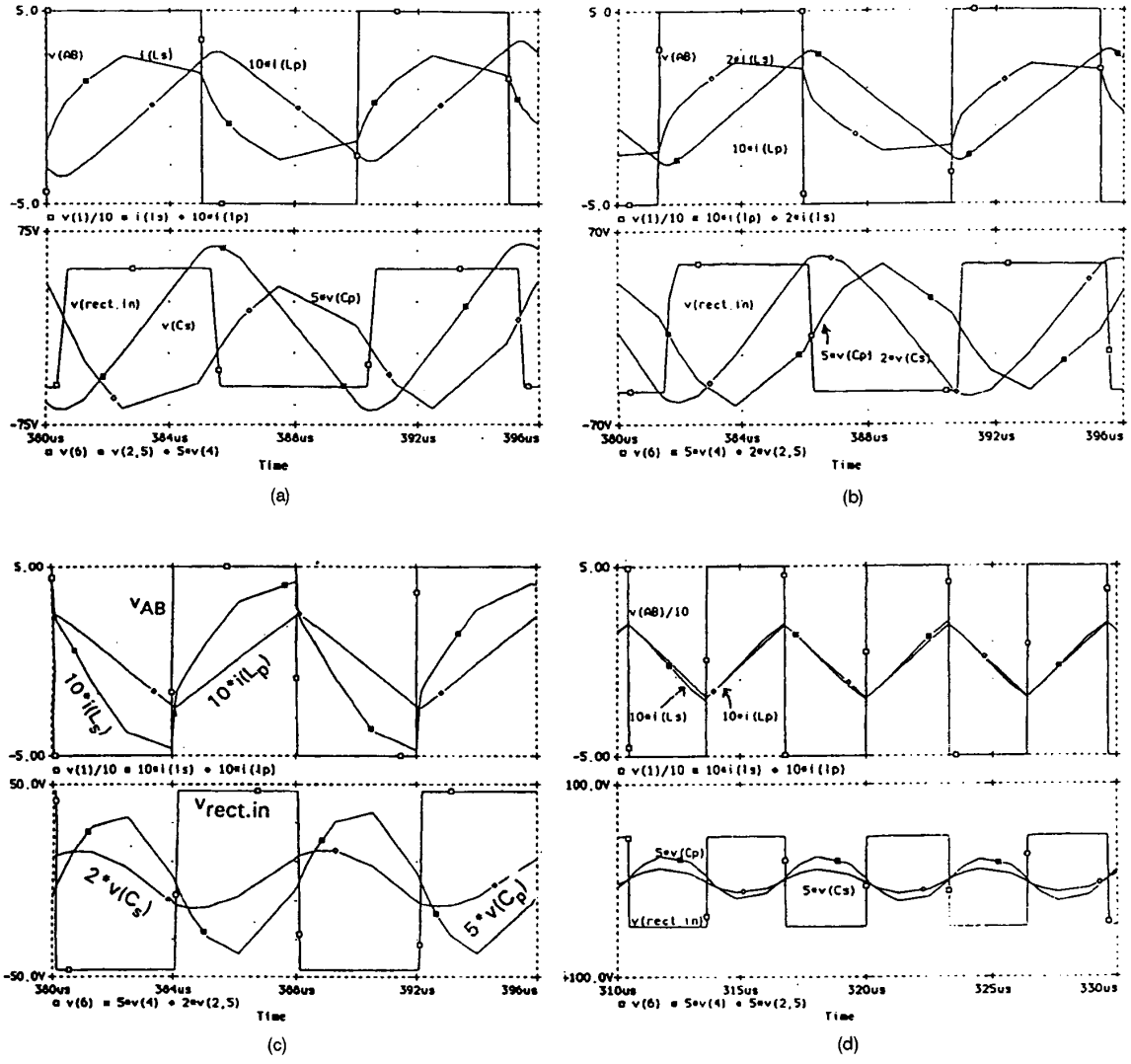


Fig. 6. Waveforms obtained from SPICE simulation for designed converter. Component values used in simulation correspond to design example. (a) Full-load, $R'_L = 24.1\ \Omega$. (b) Half-load, $R'_L = 48.2\ \Omega$. (c) 10% rated load, $R'_L = 241\ \Omega$. (d) Almost load open circuit, $R'_L = 241\ \text{M}\Omega$.

V. SPICE SIMULATION RESULTS

The converter designed in Section IV has been simulated using SPICE program for varying load conditions. Fig. 6 shows some of the waveforms obtained for full load to almost load open circuit condition. In all these waveforms, switching frequency was adjusted (after a number of simulation runs) such that load voltage remains the same as the value obtained at full load. It is clear from these waveforms that the variation in switching frequency required is narrow and the inverter output peak current reduces almost in proportional to the load. Under no load condition, current through L_s is the same as current through L_p. Table I summarizes the results obtained from the simulation.

VI. EXPERIMENTAL RESULTS

The results obtained from an experimental converter are presented in this section. The details of the 100 W experimental converter built using the metal-oxide semiconductor field-effect transistors (MOSFETs) as the switches are given in Fig. 7. Typical waveforms obtained from the experimental converter (operating in the lagging PF mode) are shown in Fig. 7 for variations in the load from full load value to very light load (approximately 10%) condition. In all

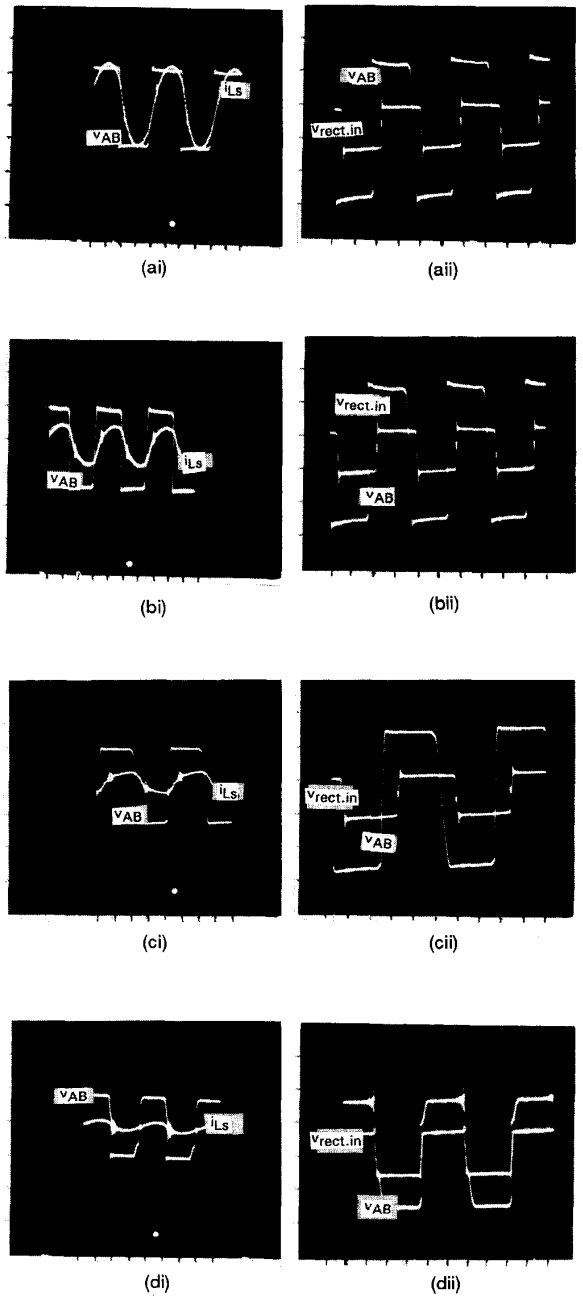


Fig. 7. Experimentally obtained waveforms. (a) Full load (R_L = 22 Ohms). (a1) ν_{AB} (40 V/div.) and inverter output current i_{Ls} (2.3 A/div.), (a2) ν_{AB} (25 V/div.), $\nu_{rect.in}$ (60 V/div.), switching frequency, $f_s \cong 100$ kHz. (b) 50% of full load. (b1) and (b2) same waveforms as (a1) and (a2), $f_s \cong 125$ kHz. (c) 25% of full load, (c1) and (c2) same waveforms as (a1) and (a2), $f_s \cong 165$ kHz. (d) Approximately 10% of full load, (d1) and (d2) same waveforms as (a1) and (a2), but ν_{AB} (50 V/div.) in (d1) and ν_{AB} (30 V/div.) in (d2), $f_s \cong 200$ kHz. (Details of converter. Switches used—IRFP250 MOSFETs, feedback diodes—internal to the MOSFETs, Input dc voltage, $2E$ = 100 V, L_s = 76.8 μH, C_s = 0.033 μF, L_p = 768 μH, C_p = 0.33 μF, rectifier bridge diodes—1N3891.)

TABLE I
Summary of Results Obtained From SPICE Simulation for Designed Converter of Section IV

Parameter	Full-load	50% of full-load	10% of full-load	Open circuit
R'_L (Ω)	24.1	48.2	241	241 MΩ
Switching frequency (f_s) (kHz)	100	107.5	125	156.25
Peak current through L_s (I_{Lsp})	2.7 A	1.1 A	0.46 A	0.21 A
Peak current through L_p (I_{Lpp})	0.32 A	0.29 A	0.26 A	0.21 A
Peak voltage across C_s (V_{Csp})	65 V	35 V	8.3 V	3.6 V
Peak voltage across C_p (V_{Cpp})	6.7 V	12.1 V	7.5 V	4.3 V

these waveforms, the output load voltage was held constant at 40 V (value obtained at the full load). The switching frequency was varied to regulate the output load voltage. It can be easily observed from Fig. 7 that the inverter output peak current decreases from about 3 A at full load to approximately 0.3 A at 10% load. Table II summarizes the experimental results. Table III compares the results obtained from the theory, SPICE simulation and experiment for the full load conditions (component values used correspond to the experimental converter). These results are in reasonably good agreement. It must be noted that component values used in the experimental setup are not the values corresponding to the optimized converter given in the design example. Due to this reason, the switching frequency required is wider than the design example. The above 100 W experimental converter was used only to illustrate the operating principle of the converter. This converter can be built at higher power levels switching at few hundreds of kHz with the same performance.

VII. CONCLUSIONS

In this paper, (LC)(LC)-type series-parallel resonant converter operating in the lagging PF mode has been proposed and analyzed using complex ac circuit analysis method. Analysis presented has been used to obtain design curves. A simple design procedure has been illustrated using a design example of 100 W converter. Detailed SPICE simulation results have been presented to evaluate the performance of the converter for varying load conditions. It can be observed from the results that the inverter output peak current (same as the switch peak current) reduces with the load current thus having high efficiency even at very light load conditions and, therefore maintains the advantages of the standard SRC. It has also been shown that the converter can operate with load open circuit condition without increasing the frequency to a very high value. It must be noted that

TABLE II
Summary of Experimental Results

Parameter	Full-load	50% of full-load	25% of full-load	10% of full-load
Switching frequency (f_s) (kHz)	100	125	165	200
Peak current through L_r (I_{Lrp})	3 A	1.5 A	0.7A	0.3 A
Peak current through L_p (I_{Lpp})	0.4 A	0.2 A	0.1 A	0.05 A
Peak voltage across C_r (V_{Crp})	150 V	60 V	24 V	12 V
Peak voltage across C_p (V_{Cpp})	2.5 V	2.5 V	2 V	2 V
Efficiency	90.8%	91.13%	88.6%	85.6%
Load current	1.82 A	0.92 A	0.45 A	0.2 A

Note: Details of converter are given in Fig. 7, $2E = 100$ V, load voltage, $V_0' = 40$ V.

TABLE III
Comparison of Analytical, Simulation and Experimental Results

Parameter	Calculated	Simulated	Measured
Peak current through L_r (I_{Lrp})	3.26A	3.278 A	3 A
Peak current through L_p (I_{Lpp})	0.2 A	0.317 A	0.4 A
Peak voltage across C_r (V_{Crp})	165 V	163.8 V	150 V
Peak voltage across C_p (V_{Cpp})	1.2 V	2 V	2 V
Load voltage, V_o	46.8 V	45 V	40 V

Note: Details of converter are given in Fig. 7, supply voltage $2E = 100$ V, full load $R_L' = 22$ Ohms, switching frequency $f_s = 100$ kHz.

the components used in the parallel branch draw very small current. By placing the parallel branch (L_pC_p) on the secondary-side, the leakage inductances of the HF transformer can also be used as part of resonating inductances. If (L_pC_p) is placed on a tertiary winding [16, Fig. 2(b)], then the leakage inductances can be used as part of L_s and L_p. The converter proposed in this paper is ideally suited for high voltage output applications due to the use of capacitive output filter. If the parallel inductor L_p is shorted, then the converter becomes LCC-type converter with capacitive output filter [18]. If the parallel capacitor C_p is shorted, then the converter becomes LCL-type converter with capacitive output filter [19–21]. The steady-state performance characteristics of the (LC)(LC)-type converter designed in this paper are very close to those of LCL-type converter with capacitive output filter. The transient performance of the converter has to be investigated in future work. But preliminary studies show that step changes in load causes a dc current in the parallel branch for the LCL-type converter, whereas (LC)(LC)-type converter does not have this dc component due to the presence of C_p.

The complex ac circuit analysis presented looses accuracy in predicting the results at reduced load currents due to deviation of the waveforms from sinusoidal approximation. However, designing the converter at full load using approximate analysis and then using SPICE simulation to predict the performance of the converter simplifies the design procedure. Further work is under progress to analyze the converter using exact method and to operate the converter in fixed-frequency mode.

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REFERENCES

[1] Sum, K. K. (1988)
Recent developments in resonant power conversion.
Intertech Comm. Inc., 1988.

[2] Ranganathan, V. T., et al. (1982)
A regulated dc-dc voltage source converter using a high-frequency link.
IEEE Transactions on Industry Applications, **IA-18**, 3 (May/June 1982), 279–287.

[3] Bhat, A. K. S., and Dewan, S. B. (1987)
Analysis and design of a high-frequency link resonant converter using LCC-type commutation.
IEEE Transactions on Power Electronics, **PE-2**, 4 (Oct. 1987), 291–301.

[4] Chen, J., and Bonert, R. (1983)
Load independent AC/DC power supply for high frequencies with sine-wave output.
IEEE Transactions on Industry Applications, **IA-19**, 2 (Mar./Apr. 1983), 223–227.

[5] Steigerwald, R. L. (1988)
A comparison of half-bridge resonant converter topologies.
IEEE Transactions on Power Electronics, **3**, 2 (Apr. 1988), 174–182.

[6] Johnson, S. D., Witulski, A. F., and Erickson, R. W. (1987)
A comparison of resonant converter topologies in high voltage DC applications.
In *IEEE Applied Power Electronics Conference Record*, (1987), 145–156.

[7] Muroyama, S., and Sakakibara, K. (1982)
Characteristics of a new series resonant converter.
In *Proceedings of IEEE International Telecommunications Energy Conference (INTELEC)*, (1982), 111–116.

[8] Kuwata, Y., Ohashi, Y., and Yotsumoto, K. (1987)
Characteristics of a new series resonant converter with a parallel resonant circuit.
In *Proceedings of IEEE International Telecommunications Energy Conference* (INTELEC), (1987), 204–210.

[9] Bhat, A. K. S. (1991)
A unified approach for the steady-state analysis of resonant converters.
IEEE Transactions on Industrial Electronics, **38**, 4 (Aug. 1991), 251–259.

[10] Jain, P. (1989)
A 20 kHz hybrid resonant power source for the space station.
IEEE Transactions on Aerospace and Electronic Systems, **25**, 4 (July 1989), 491–496.

[11] Jain, P., Bannard, D., and Cardella, M. (1992)
A phase-shift modulated double tuned resonant DC/DC converter: Analysis and experimental results.
In *Proceedings of IEEE Applied Power Electronics Conference*, (1992), 90–97.

[12] Rosenberg, S. A., and Dewan, S. B. (1977)
An inverter/cycloconverter system for variable frequency, variable voltage, ac power supplies.
In *Proceedings of IEEE IAS International Semiconductor Power Conference*, (1977), 247–255.

[13] Baterseh, I., and Lee, C. Q. (1991)
Steady-state analysis of the parallel resonant converter with LLCC-type commutation network.
IEEE Transactions on Power Electronics, **6**, 3 (July 1991), 525–538.

[14] Bhat, A. K. S., and Dewan, S. B. (1989)
A generalized approach for the steady-state analysis of resonant inverters.
IEEE Transactions on Industry Applications, **25**, 2 (Mar./Apr. 1989), 326–338.

[15] Bhat, A. K. S. (1990)
Analysis and design of a modified series resonant converter.
In *IEEE Applied Power Electronics Conference Record*, (1990), 594–600.

[16] Bhat, A. K. S. (1991)
Analysis and design of a parallel resonant converter with the resonating capacitor placed on a tertiary winding.
In *IEEE Industry Application Society Conference Record*, (Oct. 1991), 990–995.

[17] Biswas, A. (1993)
Analysis and design of (LC)(LC)-type series-parallel resonant converter.
M.E. project report, Department of Electrical Engineering, Indian Institute of Science, Bangalore, Feb. 1993.

[18] Bhat, A. K. S. (1991)
Analysis and design of a series-parallel resonant converter with capacitive output filter.
IEEE Transactions on Industry Applications, **27**, 3 (May/June 1991), 523–530.

[19] Severns, R. (1990)
Topologies for three element resonant converters.
In *IEEE Applied Power Electronics Conference Record*, (Mar. 1990), 712–722.

[20] Schmidtner, E. G. (1988)
A new high frequency resonant converter topology.
In *High Frequency Power Conversion Conference Record*, (1988), 390–403.

[21] Bhat, A. K. S. (1990)
Analysis and design of LCL-type series resonant converter.
In *Proceedings of IEEE International Telecommunications Energy Conference* (INTELEC), (1990), 172–178.

Improving Performance in Pulse Radar Detection Using Neural Networks

A new approach using a multilayered feed forward neural network for pulse compression is presented. The 13 element Barker code was used as the signal code. In training this network, the extended Kalman filtering (EKF)-based learning algorithm which has faster convergence speed than the conventional backpropagation (BP) algorithm was used. This approach has yielded output peak signal to sidelobe ratios which are much superior to those obtained with the BP algorithm. Further, for use of this neural network for real time processing, parallel implementation of the EKF-based learning algorithm is indispensable. Therefore, parallel implementation of the EKF-based learning algorithm on a network of three transputers also has been developed.

I. INTRODUCTION

Pulse compression technique [1] is always used to improve the performance in pulse radar detection. In practice, two different approaches are used to obtain the pulse compression. The first one is to use a matched filter, in which codes with small sidelobes in their autocorrelation functions are used. The second approach is to use inverse filters of two kinds, viz., nonrecursive time invariant causal filter [2] and recursive time variant filter [3].

A new approach using a multilayered neural network that yields much better signal-to-sidelobe ratio (the ratio of peak signal to maximum sidelobe) than the traditional approaches has been reported in [4]. This approach also has an advantage of robustness that is typical of multilayered neural networks. In this approach, the 13 element Barker code [1] which has the sequence $[1,1,1,1,1,-1,-1,1,1,-1,1,-1,1]$ and the maximum length sequences (m-sequences) of lengths 15, 31, and 63 (all of them are single period) [1] were used as the signal codes, and four networks were implemented, respectively. Each of the networks used had n input nodes (where n is the code length), three hidden nodes, and a single output node.

The BP algorithm, which is the most popular learning algorithm for training neural networks, was used for training the network. The training set for each network comprised of just the time-shifted sequences with magnitudes ± 1 of the code adopted. The desired

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