A Single-Phase Boost Rectifier System for Wide Range of Load Variations

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***Abstract*—Converters operated in discontinuous-conduction-mode (DCM) and in continuous-conduction-mode (CCM) are suitable for lighter and higher loads, respectively. A new, constant switching frequency based single-phase rectifier system is proposed, which operates in DCM and in CCM for outputs less than and greater than 50% rated load, respectively, covering a wide range of load variation. The power circuit and the control circuit of the proposed rectifier are easily configurable for DCM and CCM operations. The measured load current is used to select the desired operating mode. The peak device current under DCM is limited to rated device current under CCM without using a device of higher current rating. The input current shaping under CCM and DCM are based on the comparison of measured input current with linear and nonlinear carriers, respectively. A load current feedforward scheme is presented to improve the system dynamic performance and also to ensure a smooth transition between the two operating modes. All the necessary control operations are performed without using multiplication, division and square-root operation. The proposed rectifier shows improved input current characteristics over the existing CCM converters for the above load range. This is validated on a 600-W rectifier prototype. Simulation and experimental results are presented.**

***Index Terms*—Continuous-conduction-mode (CCM), discontinuous-conduction-mode (DCM).**

I. Introduction

SINGLE-PHASE diode bridge rectifiers are gradually being replaced by pulsewidth modulation (PWM) rectifiers to maintain a sinusoidal input current at near unity power factor and to satisfy the necessary harmonic standards [1], [2]. A single-phase, single-switch boost rectifier (Fig. 1) is a well-established topology in the field of ac–dc power conversion to comply with the above harmonic standards. The rectifier system may be operated in the continuous conduction mode (CCM), or in the discontinuous conduction mode (DCM) [3]–[5].

The CCM is preferred over DCM because of continuous input current and low conducted electromagnetic interference (EMI) [6]. However, it is reported to have high input current distortion at light load [7]. For a particular switching frequency and boost inductance, the amount of current distortion increases as the load decreases [7]. A high valued boost inductor is necessary at light load to limit the input current distortion [7]. This increases the size, weight, and cost of the converter and results in poor system dynamic response. Hence, CCM is preferred at higher loads [7], [8].

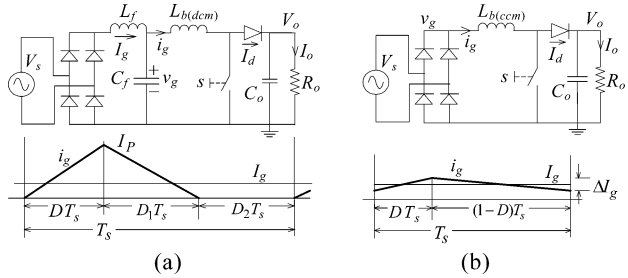

Fig. 1. Single-phase, single-switch boost rectifier: (a) topology based on DCM and (b) topology based on CCM.

The above issues are not seen, when the converter is operated in DCM. However, DCM is always associated with high device current stress and conducted EMI [6]. Therefore, a high current rated device and a costly EMI filter are necessary at higher loads. Thus, DCM is preferred for light loads.

The present work deals with a constant output voltage application, where the load current varies over a wide range (10% to 110% of rated load current) and the converter is required to comply with the necessary harmonic standards [1], [2]. It can be seen from the above discussion that neither of the operating modes (CCM and DCM) alone is suitable and economical for the above application. Therefore, the optimum choice is to operate the converter in DCM during light loads and in CCM for higher loads [9]. The load boundary between DCM and CCM operations can be set at a suitable level (say 50%) to limit the peak device current stress under DCM up to the rated device current under CCM without using a higher current rated device. Similarly, the minimum load under CCM, for which the converter is required to comply [1], [2] is 50% rated load. This permits us to use a low valued boost inductor compared to the entire CCM case without any degradation in the performance of the converter [9].

The main challenge associated with such a mixed-mode operation [9] is to realize the two distinct operating modes (DCM and CCM) into a single converter system without introducing any appreciable dynamics during transition between the two operating modes. There are two possible ways to achieve this. The first method suggests a single-valued boost inductor with constant but two different switching frequencies (a low switching frequency for DCM and a high switching frequency for CCM) for the above operation. The second method requires two different boost inductors (a high valued inductor for CCM and a low valued inductor for DCM) with a constant switching frequency for above application. The first method is simpler than the second method, as it only requires the switching frequency

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of the converter to be changed. However, the second method requires the physical inductors to be changed.

A converter system, using two different switching frequencies (2.56 kHz for DCM and 25.6 kHz for CCM) and a single valued boost inductor has been reported in [9]. The use of two different switching frequencies introduces difficulties in designing the EMI filter. The controller works in the principle of voltage mode control without using any input current sensor. A current sensor is however required for over-current protection of the converter. The input current distortion under DCM is high as there is no lowpass filter connected at the input to the converter. The implementation of the above control scheme involves complex mathematic operations, such as multiplications, divisions and square root operations. It also requires the peak value and the zero crossing instants of the input voltage to compute the unit vectors ($\sin\theta$ and $\cos\theta$). These increase the complexity and cost of the controller.

Addressing the above-mentioned issues and using two different boost inductors (a high valued inductor for CCM and a low valued inductor for DCM) a new, constant-switching-frequency based rectifier system is proposed in this paper. The power circuit of the proposed converter system can be configured either for CCM or for DCM by performing a simple on-off control of an auxiliary switch. A DCM power topology, with an input side lowpass filter is obtained, when the auxiliary switch is on. Again, a CCM power topology (without any input filter) is realized, when the auxiliary switch is off.

A simple, input voltage sensorless, current-mode controller [10] is proposed for the above rectifier system. The controller works in the principle of one-cycle control [7] or the nonlinear carrier control [4], [11] without using any of the above-mentioned complex mathematical operations. The required gating pulses for the converter switch are generated by comparing the measured input current with one of the two periodic carriers in a modulator. A linear carrier is used under CCM, while a nonlinear carrier is selected under DCM. The measured load current is used to select the desired operating mode (CCM or DCM). A simple load current feedforward scheme is used to improve the dynamic response of the converter system, which also ensures a smooth transition from one operating mode to the other. The proposed concept has been simulated on MATLAB/SIMULINK platform and experimentally validated on a 600-W prototype. The simulation and experimental results are presented.

II. Proposed Single-Phase Rectifier System

A single-phase, single-switch boost rectifier is shown in Fig. 1, where Fig. 1(a) and (b) represent the DCM and the CCM boost rectifier topologies, respectively. A lowpass filter (L_fC_f) is used in the DCM topology for filtering the switching current harmonics, which is absent in the CCM topology. Further, it can be shown that for the same switching frequency, the value of boost inductor $L_{b(dcm)}$ is much lower than $L_{b(ccm)}$. Thus, for the same switching frequency, the DCM topology is not suitable for CCM operation and vice versa. Similarly, it can be shown that the control scheme, suitable for CCM application [4] may not be useful in DCM operation and vice versa. Therefore, a common rectifier system (power circuit topology and control scheme) is required to be developed, which is suitable for both CCM and DCM. Such a rectifier system is developed in this section.

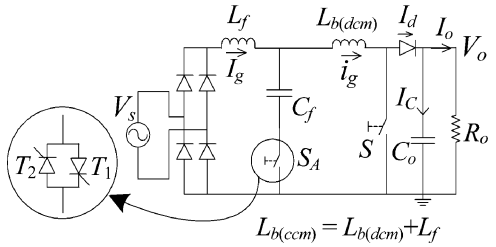

Fig. 2. Proposed power circuit topology.

A. Proposed Power Circuit Topology

The proposed power circuit topology is shown in Fig. 2, which is originally derived from the DCM topology shown in Fig. 1(a). There are two separate inductors L_f and $L_{b(dcm)}$ and a filter capacitor C_f used in the power circuit as shown. The auxiliary switch S_A may be turned on to realize the DCM power topology same as Fig. 1(a). The combination L_fC_f serves the purpose of the input lowpass filter, while the inductor $L_{b(dcm)}$ acts as the effective low valued boost inductor.

The switch S_A can be turned off, when the CCM topology is to be realized. The filter capacitor C_f remains ineffective in the power circuit, while the series combination of L_f and $L_{b(dcm)}$ acts as the effective high valued boost inductor $L_{b(ccm)}$. A detailed design method for selecting L_f, $L_{b(dcm)}$, $L_{b(ccm)}$ and C_f is presented in Section III.

It is shown that by simple on-off control of the switch S_A, we can realize two different power topologies [Fig. 1(a) and (b)] using a single converter system, while maintaining a constant switching frequency throughout. Now it is required to understand the various issues associated with turn-on and turn-off instants of the switch S_A and to propose a suitable semiconductor switch for its realization.

Let us consider a case, when the converter system is required to be driven into DCM from its original CCM operation. This means that the switch S_A, which was originally off is now required to be closed. When the converter is operated under CCM, the inductors $L_{b(dcm)}$ and L_f carry the same instantaneous current $i_g = I_g$, while the filter capacitor C_f does not carry any current. Under this condition S_A can be closed at any instant with zero current switching to drive the converter system into DCM.

Now, let us consider the other possibility, i.e., the converter system, which was initially operating under DCM and is required to be driven into CCM. It can be seen from Fig. 1(a) that, under DCM the instantaneous currents carried by the inductors $L_{b(dcm)}$ and L_f are different. Nevertheless, it can be shown that the current $(I_g - i_g)$, through the switch S_A passes through zero twice in a switching cycle. Now, if we try to open S_A at an instant $i_g \neq I_g$, the difference current $(I_g - i_g)$ will flow momentarily through S_A. This can cause over-voltage across S_A, which can damage the switch. In order to avoid this situation, we propose two anti-parallel thyristors, each conducting during one half cycle of the switching frequency current components, for the realization of S_A as in Fig. 2. Now both turn on and turn

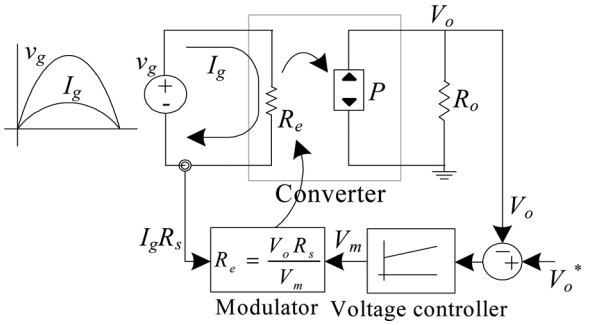

Fig. 3. Resistor emulator [10].

off of the thyristors are at zero current (i.e. at $i_g = I_g$) ensuring a smooth transition from DCM to CCM and vice versa.

It should be noted that it is also possible to use a single thyristor and an anti-parallel diode to realize S_A. In that case, the thyristor T_2 (Fig. 2) may be replaced by a diode of same polarity. The advantage of this method is that no isolated gate drive is required to drive the switch S_A.

Now, it is required to develop a suitable controller for controlling the proposed power topology, which is suitable for both CCM and DCM operations. Such a controller is developed in the following section.

B. Proposed Controller

The proposed controller works on the principle of resistor emulator [7] as shown in Fig. 3. One of the control objectives is to shape the averaged input current I_g follow the input voltage v_g as shown in (1), where R_e is the desired input port resistance of the proposed converter

$$I_g = v_g/R_e. \tag{1}$$

The next objective is to maintain the output voltage V_o at the desired reference level against all possible input voltage and load variations. This is achieved by regulating the input power to the converter through R_e by closed loop control as shown in Fig. 3. The output V_m of the voltage controller is used to regulate R_e as shown in (2), where R_s is the gain in the current sensing path [4], [7]

$$V_m = (V_o.R_s)/R_e. \tag{2}$$

Equations (1), (2) and the quasi steady state approach [7] are used to establish the necessary control equations for the DCM and CCM operations. A constant but high switching frequency $f_{sw} = 1/T_s$ is assumed throughout.

1) Control Equation for CCM: The converter is assumed to be operated in CCM with switch duty ratio D as shown in Fig. 1(b). The input voltage v_g may be related to the output voltage V_o and the duty ratio D as shown in (3). Equations (1)–(3) may be used to obtain the required control equation for CCM operation as shown in (4) [7]

$$v_g = (1 - D)V_o \tag{3}$$

$$I_gR_s = V_m - DV_m. \tag{4}$$

2) Control Equation for DCM: The converter is assumed to be operated in DCM as shown in Fig. 1(a). In each switching interval T_s the switch S is turned on for duration DT_s. The peak inductor current I_P and the switching-cycle averaged inductor current I_g can be expressed as in (5) and (6), respectively. Eliminating D_1 and I_P from (5) and (6), the expression for the switch duty ratio D is obtained as shown in (7) [5], [12]. The duty ratio D, shown in (7) depends on I_g, $L_{b(dcm)}$, V_o, v_g and T_s. Equations (1), (2), and (7) are used to obtain the control equation for the DCM operation as shown in the following [12]:

$$I_P = \frac{v_gDT_S}{L_{b(dcm)}} = \frac{(V_o - v_g)D_1T_S}{L_{b(dcm)}} \tag{5}$$

$$I_g = \frac{(D + D_1)I_P}{2} \tag{6}$$

$$D = \sqrt{\frac{2I_g(V_o - v_g)L_{b(dcm)}}{V_ov_gT_S}} \tag{7}$$

$$I_gR_s = V_m - D^2\left(\frac{R_sT_s}{2L_{b(dcm)}}\right)V_o. \tag{8}$$

3) The Carrier Waves: The control equations (4) and (8) may be solved for D and accordingly the required gating pulses for the switch S under CCM and DCM operations may be generated. This, however, involves complex mathematic operations such as multiplications, divisions and square root operations, which increase the cost and complexity of controller. In order to avoid such complex operations a carrier-based approach is followed in this paper [4], [5], [12].

The right hand sides of (4) and (8) may be considered for the generation of two carriers $v_{c(ccm)}$ and $v_{c(dcm)}$ as shown in (9) and (10), respectively, where D is replaced by t/T_s [4], [5]. The carriers (9) and (10) represent a linear and a nonlinear carriers for CCM and DCM operations, respectively

$$v_{c(ccm)}(t) = V_m - \left(\frac{V_m}{T_s}\right)t; \quad 0 < t < T \tag{9}$$

$$v_{c(dcm)}(t) = V_m - \left(\frac{R_sV_o}{2L_{b(dcm)}T_s}\right)t^2; \quad 0 < t < T. \tag{10}$$

4) Gating Pulse Generation Under DCM and CCM: The process of gate pulse generation under DCM and CCM operations are shown in Fig. 4(a) and (b), respectively. The carriers $v_{c(dcm)}$ and $v_{c(ccm)}$ can be generated using simple op-amp based integrator and amplifier circuits as shown. The integrators are reset at the beginning of each switching cycle by a constant-frequency clock of negligible pulse width. At the beginning of each switching cycle ($t = 0$), each of the above carriers start from the same initial value V_m. At $t = DT_s$, the carrier $v_{c(ccm)}$ equals the RHS of (4), while the carrier $v_{c(dcm)}$ equals the RHS of (8). Further, at $t = DT_s$, the RHS of (9) and that of (10) equal the measured input current I_gR_s [see (4) and (8)]. Thus, the required gating pulses for the switch S can be generated by comparing the measured input current I_gR_s with either of the above carriers in a comparator. The linear carrier (9) may be used during CCM, while the nonlinear carrier (10) may be selected during DCM.

The converter system is required to be operated in DCM during lighter load and in CCM for higher load. The measured load current I_oR_s may be compared with a reference load

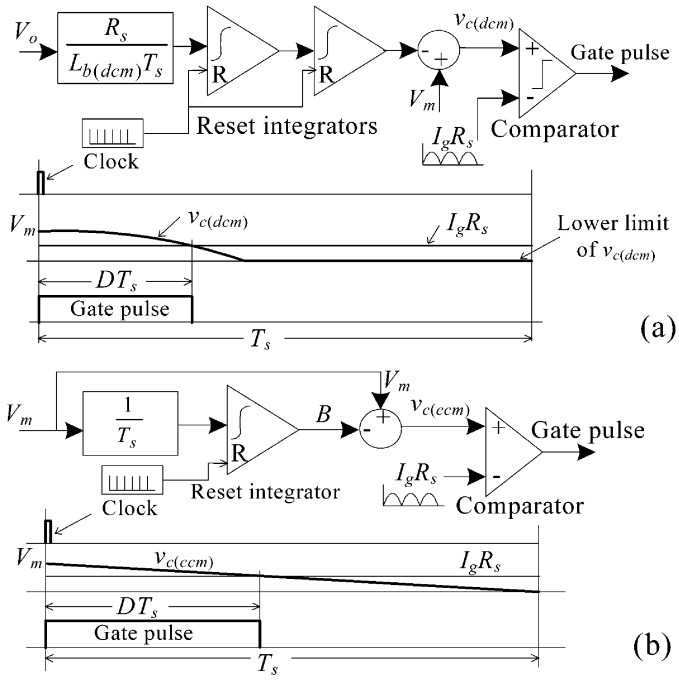

Fig. 4. Gating pulse generation under (a) DCM and (b) CCM.

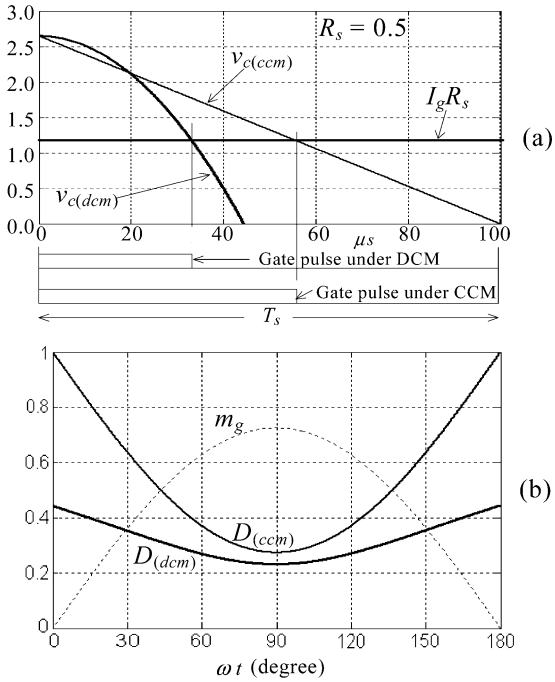

Fig. 5. Comparison of CCM and DCM modes for the same output power of 300 W: (a) variation of carriers over a switching cycle and (b) variation of duty ratio over a half line cycle.

current $I_{o(\mathrm{ref})}$ [set at a level corresponding to the load boundary between CCM and DCM operations (discussed in Section III)] in a hysteresis comparator to select the desired operating mode (CCM or DCM).

It can be seen that the process of gating pulse generation under CCM is different from the process under DCM. Further, the DCM operation is effective only during lighter loads, while the CCM is during higher loads. A one-to-one comparison of the carriers and the duty ratios under CCM and DCM for an output power of 300 W is given below.

5) Comparison of the Carriers and the Duty Ratios: Let us define the voltage ratio m_g as shown in (11), where ω is the supply angular frequency, v_g and V_{gm} are the instantaneous and the peak input voltages, respectively, and $M_g = V_{gm}/V_o$

$$m_g = \frac{v_g}{V_o} = \frac{V_{gm}\sin(\omega t)}{V_o} = M_g \sin(\omega t). \tag{11}$$

Equations (1) and (11) may be used to modify (3) and (7) as in (12) and (13), respectively, where $K = 2L_{b(dcm)}f_{sw}/R_e$. It can be seen that the duty ratio under CCM depends only on m_g. However, in addition to m_g, the duty ratio under DCM depends on the output power through parameter K

$$D_{(\mathrm{ccm})} = 1 - \frac{v_g}{V_o} = (1 - m_g) \tag{12}$$

$$D_{(\mathrm{dcm})} = \sqrt{K(1 - m_g)}. \tag{13}$$

The variations of the carriers (9) and (10) in a particular switching cycle T_s are shown in Fig. 5(a). The variations of $D_{(\mathrm{ccm})}$ and $D_{(\mathrm{dcm})}$ over a half fundamental cycle are shown in Fig. 5(b). The output power in all the above cases is 300 W (see parameters in Section III-G).

6) Load Current Feedforward: The voltage loop of the proposed converter system is required to be designed for low bandwidth (see Section III-F) to limit the input current distortion caused by the output voltage ripple [5]. This results in poor system dynamic response with significant undershoot and overshoot in the output voltage V_o during sudden changes in the load. A typical settling time of the voltage loop for a step change in load is reported to be around 250 ms [5]. A simple load current feedforward scheme is used in this paper to improve the dynamic response of the converter system and also to ensure a smooth transition from one operating mode to the other.

It can be seen from (2) that the output V_m of the voltage controller controls the input power to the converter through R_e. However, the output power of the converter is controlled by the load current I_o. At steady state, the input power equals the output power (internal losses are neglected) as shown in (14). Equation (14) may be used to express the steady state value of V_m in terms of I_o as shown in

$$P_o = V_o I_o = \frac{V_o^2}{R_o} = \frac{V_{gm}I_{gm}}{2} = \frac{V_{gm}^2}{2R_e} \tag{14}$$

$$V_m = \left(\frac{2R_s V_o^2}{V_{gm}^2}\right) I_o = \left(\frac{2R_s}{M_g^2}\right) I_o. \tag{15}$$

Though the steady state value of V_m is proportional to I_o, it is not so during transients. When the load changes suddenly, the voltage loop acts slowly to adjust V_m from its original value to a new steady state value depending on its bandwidth. During this time, the input-output power balance gets disturbed. This appears as overshoot or undershoot in the output voltage V_o.

In order to avoid this issue, the control parameter V_m is reconstituted from two control inputs as shown in (16), where $V_{m(VC)}$ is the output of the voltage controller and the RHS of (15) is used as the feedforward input $V_{m(FF)}$. The measured load current $I_o R_s$ is used to obtain the feedforward input $V_{m(FF)}$

$$V_m = V_{m(VC)} + V_{m(FF)} = V_{m(VC)} + \left(2/M_g^2\right) I_o R_s. \tag{16}$$

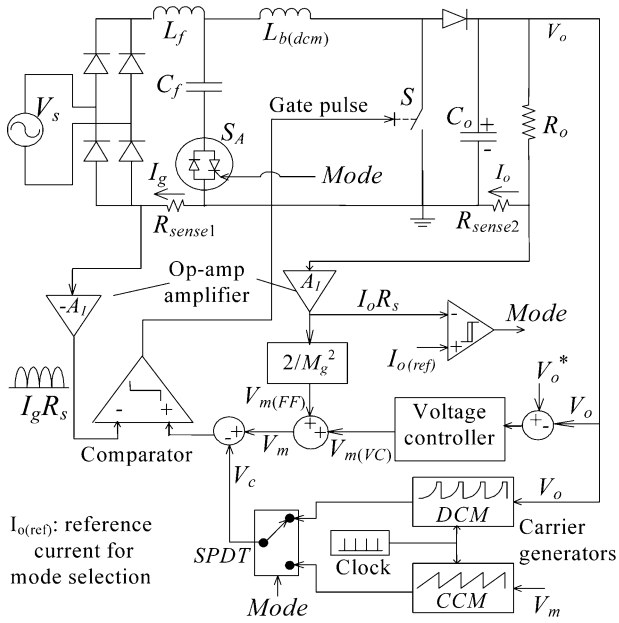

Fig. 6. Proposed controller.

The feedforward input $V_{m(FF)}$ helps the control parameter V_m settle immediately to the neighborhood of its final value during above transients. The fine adjustment of V_m is performed slowly through $V_{m(VC)}$.

The rated value of M_g may be used to derive the feedforward input $V_{m(FF)}$. It can be shown that at rated input voltage, $V_{m(VC)}$ is zero. However, the output $V_{m(VC)}$ takes a non-zero value, when the input voltage deviates from its rated value.

The complete block diagram of the proposed control scheme is shown in Fig. 6. All measurements can be performed with respect to the negative terminal of the output capacitor C_o. It can be seen that no electrical isolation is required for the measurements as well as for gate drive.

III. Design

This section explains a detailed design method for selecting different passive components such as $L_{b(dcm)}$, L_f, C_f and C_o, and the parameters of the voltage controller.

A. Load Boundary Between CCM and DCM Operations

For the same output power, the peak device current in DCM is much higher than in CCM. Therefore, it is required to set the load boundary between CCM and DCM operations to a level, where the maximum device current under DCM is less than or equal to the rated device current under CCM.

Equations (5), (7), and (14) may be used to express the peak device current $I_{P(\mathrm{dcm})}$ under DCM as in (17), where K_1 is defined in (18), $I_g = I_{gm}\sin(\omega t)$ and $P_{o(dcm(max))}$ is the desired maximum output power under DCM. Equation (17) has a maximum value $I_{P(dcm(max))}$ at $\omega t = \sin^{-1}[2/(3M_g)]$ as in

$$I_{P(\mathrm{dcm})} = K_1 m_g \sqrt{(1-m_g)} \tag{17}$$

$$K_1 = \frac{2}{M_g}\sqrt{\frac{P_{o(\mathrm{dcm(max)})}}{L_{b(\mathrm{dcm})} f_{sw}}} \tag{18}$$

$$I_{P(\mathrm{dcm(max)})} = \left(\frac{2}{3\sqrt{3}}\right) K_1. \tag{19}$$

Using (14), the peak device current $I_{P(\mathrm{ccm(max)})}$ under CCM is shown in (20), where $P_{o(\mathrm{ccm(max)})}$ is the maximum output power under CCM, which decides the current rating of the device. It should be noted that in (20) the effect of ripple current in the inductor has been neglected. In order to keep the peak device current under DCM within $I_{P(\mathrm{ccm(max)})}$, we have the constraints

$$I_{P(\mathrm{ccm(max)})} = \frac{2P_{o(\mathrm{ccm(max)})}}{V_{gm}} \tag{20}$$

$$I_{P(\mathrm{dcm(max)})} \le I_{P(\mathrm{ccm(max)})} \tag{21}$$

$$P_{o(\mathrm{dcm(max)})} \le \left(\frac{27 L_{b(\mathrm{dcm})} f_{sw}}{4V_o^2}\right) P_{o(\mathrm{ccm(max)})}^2. \tag{22}$$

It is seen in (22) that for a given V_o, f_{sw} and $P_{o(\mathrm{ccm(max)})}$, the selection of the load boundary between CCM and DCM operations depends on $L_{b(\mathrm{dcm})}$.

B. Boost Inductor $L_{b(\mathrm{dcm})}$

In Fig. 1(a), the interval D_2T_s becomes zero, when the converter operates at CCM–DCM boundary (note that the CCM–DCM boundary is different from the load boundary between CCM and DCM operations). The corresponding average inductor current I_g is shown in (23). Equations (1) and (23) are used to obtain the corresponding duty ratio as in

$$I_g = \frac{I_P}{2} = \frac{v_g D T_s}{2L_{b(\mathrm{dcm})}} \tag{23}$$

$$D_{(\mathrm{ccm-dcm})} = K = \frac{2L_{b(\mathrm{dcm})} f_{sw}}{R_e}. \tag{24}$$

Using (13) and (24), the condition for operation at CCM-DCM boundary is shown in (25). The RHS of (25) has a minimum value of $(1 - M_g)$ at the peak of the input voltage ($m_g = M_g$). The inductor $L_{b(\mathrm{dcm})}$ is selected such a way that for an output power $P_{o(\mathrm{dcm(max)})}$, the operation of the converter is on the CCM–DCM boundary at the peak of the input voltage in a half line cycle as in (26). Equations (22) and (26) are used to determine the load boundary between CCM and DCM operations as in (27)

$$K = (1 - m_g) \tag{25}$$

$$L_{b(\mathrm{dcm})} = \frac{(1-M_g)V_{gm}^2}{4P_{o(dcm(max))} f_{sw}} \tag{26}$$

$$P_{o(\mathrm{dcm(max)})} = \left(\frac{3\sqrt{3}M_g\sqrt{(1-M_g)}}{4}\right) P_{o(\mathrm{ccm(max)})}. \tag{27}$$

C. Boost Inductor $L_{b(\mathrm{ccm})}$

Under CCM [Fig. 1(b)], the peak-to-peak ripple ΔI_g in the inductor current i_g as a per unit of the peak averaged inductor current I_{gm} is shown in (28), where $D_{(\mathrm{ccm})}$ is defined in (12).

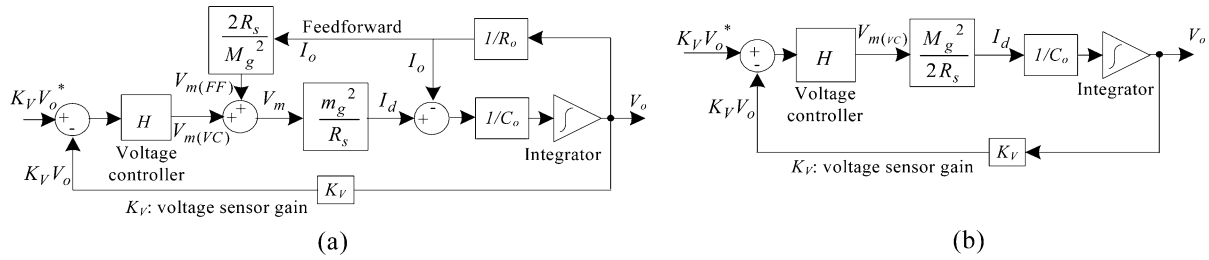

Fig. 7. (a) Averaged model of the converter and (b) voltage loop.

The value of $L_{b(\mathrm{ccm})}$ is selected based on the maximum value of $\Delta I_g/I_{gm}$ at minimum output power under CCM (i.e. $P_o = P_{o(\mathrm{dcm(max)})}$) as in (29), which occurs at $\omega t = \sin^{-1}(0.5/M_g)$

$$\frac{\Delta I_g}{I_{gm}} = \frac{v_g D_{(\mathrm{ccm})} T_s}{L_{b(\mathrm{ccm})} I_{gm}} = \left(\frac{M_g V_o^2}{2L_{b(\mathrm{ccm})} f_{sw} P_o}\right) m_g(1-m_g) \tag{28}$$

$$L_{b(\mathrm{ccm})} = \frac{M_g V_o^2}{8P_{o(\mathrm{dcm(max)})} f_{sw} (\Delta I_{g\max}/I_{gm})}. \tag{29}$$

D. Input Filter L_f and C_f

The value of $L_f = L_{b(\mathrm{ccm})} - L_{b(\mathrm{dcm})}$ can be obtained from (26) and (29). The parameter C_f may be expressed in terms of L_f and the filter corner frequency f_c as in (30), where $n = f_{sw}/f_c$. The value of C_f may be obtained by selecting a suitable value for n. A detailed design procedure is given in [13]

$$C_f = \frac{1}{L_f(2\pi f_c)^2} \approx \frac{0.025n^2}{L_f f_{sw}^2}. \tag{30}$$

E. DC Bus Capacitor C_o

The capacitor C_o (Fig. 2) carries low frequency as well as high frequency current components. For selecting the value of C_o, the high frequency current components may be neglected. The low frequency current components may be obtained from the switching-cycle averaged capacitor current I_C as in (31), where I_d is the averaged diode current, shown in (32) and $I_g = I_{gm}\sin(\omega t)$. It can be shown that (32) is valid for both CCM and DCM

$$I_C = I_d - I_o = -I_o.\cos(2\omega t) \tag{31}$$

$$I_d = m_g I_g. \tag{32}$$

The peak-to-peak ripple ΔV_o in V_o is shown in (33). Using (14) and (33), the capacitor C_o is designed for the maximum possible peak-to-peak ripple $\Delta V_{o(max)}$ as in (34), where f is the fundamental frequency

$$\Delta V_o = \frac{1}{\omega C_o}\int_{\pi/4}^{3\pi/4} I_c d\omega t = \frac{I_o}{\omega C_o} \tag{33}$$

$$C_o = \frac{P_{o(\mathrm{ccm(max)})}}{2\pi f V_o^2\left(\Delta V_{o(max)}/V_o\right)}. \tag{34}$$

F. Voltage Loop

Equations (1), (2), and (11) may be used to modify (32) as in (35). It can be seen from (35) that I_d has a dc component and an ac component. The dc component of I_d equals the load current I_o, while its ac component causes the voltage ripple $\tilde{v}_o$ in V_o as in

$$I_d = \left(\frac{m_g^2}{R_s}\right)V_m = \left(\frac{M_g^2}{2R_s}\right)V_m - \left(\frac{M_g^2 V_m}{2R_s}\right)\cos(2\omega t) \tag{35}$$

$$\tilde{v}_o = \frac{1}{\omega C_o}\int I_{d(ac)} d\omega t = \left(\frac{-V_o}{2\omega C_o R_o}\right)\sin(2\omega t). \tag{36}$$

The averaged model of the converter system, including the load current feedforward scheme, is shown in Fig. 7(a). The feedforward scheme makes the voltage loop insensitive to load current as seen in Fig. 7(b).

A simple PI type voltage controller, shown in (37), is used to control the above system. Equation (38) shows the steady state output $V_{m(VC)}$ of the voltage controller. At steady state, the dc component of the output voltage V_o equals the reference voltage V_o^*, while its ripple component (36) is processed by the voltage controller as in (39). The parameters K_{PI} and T_{PI} of the voltage controller are selected in such a way that the voltage loop does not respond to the dc bus voltage ripple [5]. Compared to the proportional term, the effect of the integral term in (39) may be ignored, when the zero of the voltage controller is placed well below the twice-line frequency $2f$ (i.e., 100 Hz) [5]

$$H(s) = \frac{K_{PI}(1+sT_{PI})}{sT_{PI}} \tag{37}$$

$$V_{m(VC)} = K_{PI}K_V\left(V_o^* - V_o\right) + \frac{K_{PI}K_V}{T_{PI}}\int\left(V_o^* - V_o\right)dt \tag{38}$$

$$\tilde{v}_{m(VC)} = -K_{PI}K_V\tilde{v}_o - \frac{K_{PI}K_V}{T_{PI}}\int\tilde{v}_o dt \approx -K_{PI}K_V\tilde{v}_o. \tag{39}$$

An ideal condition is when there is no ripple in V_o and V_m. Equations (1) and (2) may be used to express the steady state input current I_g as in (40). Now, considering the ripple in V_o and in V_m, the steady state input current (40) is modified as in (41), whose parameters are shown in

$$I_g = \frac{V_m v_g}{V_o R_s} \tag{40}$$

$$I_g = \frac{v_g}{R_e}\left(\frac{1 - A(\tilde{v}_o/V_o)}{1 + (\tilde{v}_o/V_o)}\right) \approx \frac{v_g}{R_e}\left[1 + AB\sin(2\omega t)\right]$$
$$= I_{gm}\left[\sin(\omega t) + I_2\cos(\omega t) - I_2\cos(3\omega t)\right] \quad (41)$$
$$A = \frac{K_{PI}K_V R_e}{R_s}; \quad B = \frac{1}{2\omega C_o R_o}; \quad \frac{\tilde{v}_o}{V_o} \ll 1;$$
$$I_{gm} = \frac{V_{gm}}{R_e}; \quad I_2 = \frac{AB}{2}. \quad (42)$$

It can be seen from (41) that in absence of output voltage ripple, the average inductor current I_g equals the desired current v_g/R_e. However, the presence of ripple in V_o introduces an unwanted displacement term $I_{gm}I_2\cos(\omega t)$ and a third-harmonic distortion term $I_{gm}I_2\cos(3\omega t)$ in I_g. Both of these could be controlled through K_{PI}. A low valued K_{PI} is required to maintain a low input current distortion and displacement. However, a high valued K_{PI} is required for good voltage loop response. Hence, there is a tradeoff between the fastness of response and quality of input current.

G. Design Example

This subsection presents a design example of the above converter. The specifications are as follows: i) maximum output power: $P_{o(\mathrm{ccm(max)})} = 660$ W (110% rated load), ii) peak input voltage: $V_{gm} = 156$ V, iii) line frequency: $f = 50$ Hz, iv) rated output voltage: $V_o = 215$ V, v) maximum peak-to-peak ripple in the output voltage: $\Delta V_{o(\max)} = 0.04 * V_o$, vi) maximum peak-to-peak ripple in the input current (under CCM): $\Delta I_{g(\max)} = 0.2 * I_{gm}$, vii) switching frequency: $f_{sw} = 10$ kHz, viii) voltage sensor gain: $K_v = 1/35$, and ix) current sensing gain: $R_s = 0.5\ \Omega$.

1) Energy storage elements: Equations (26), (27), (29), (30), and (34), may be used to obtain the values of the different energy storage elements. The converter is required to be operated in DCM up to 50% of the maximum load (i.e., 330 W), and in CCM between 330 Wand 660 W as seen in (43), where $M_g = V_{gm}/V_o = 0.726$

$$P_{o(\mathrm{dcm(max)})} \le \left(\frac{3\sqrt{3}M_g\sqrt{(1 - M_g)}}{4}\right) P_{o(\mathrm{ccm(max)})}$$
$$= 330\ \mathrm{W}. \quad (43)$$

The boost inductors required for the DCM and CCM operations are obtained as shown in (44) and (45), respectively. The required input filter inductance is shown in (46)

$$L_{b(\mathrm{dcm})} = \frac{(1 - M_g)V_{gm}^2}{4P_{o(\mathrm{dcm(max)})}f_{sw}} \approx 500\ \mu\mathrm{H} \quad (44)$$
$$L_{b(\mathrm{ccm})} = \frac{M_g V_o^2}{8P_{o(\mathrm{dcm(max)})}f_{sw}\left(\Delta I_{g\max}/I_{gm}\right)}$$
$$\approx 6.4\ \mathrm{mH} \quad (45)$$
$$L_f = L_{b(\mathrm{ccm})} - L_{b(\mathrm{dcm})} = 5.9\ \mathrm{mH}. \quad (46)$$

Fig. 8 shows the input filter capacitance C_f plotted against the ratio of switching frequency to filter corner frequency (n) for $L_f = 5.9$ mH as per (30). Considering $n = 10$, the filter capacitor C_f is computed in (47). Further, the dc bus capacitance is obtained as in (48)

$$C_f = \frac{0.025n^2}{L_f f_{sw}^2} \approx 4\ \mu\mathrm{F} \quad (47)$$

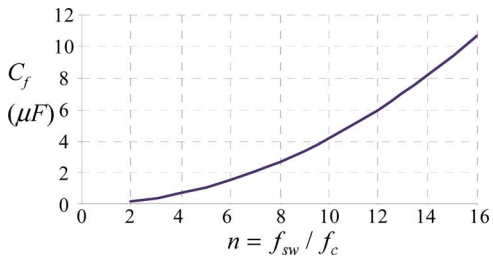

Fig. 8. Variation of C_f with n.

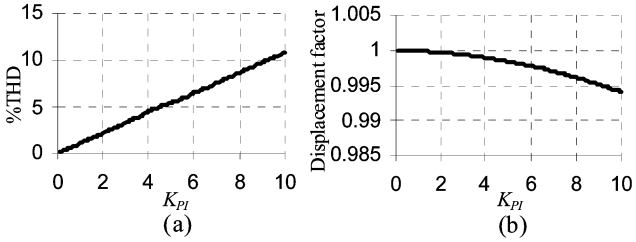

Fig. 9. (a) Variations of %THD with K_{PI} and (b) variation of displacement factor with K_{PI}.

$$C_o = \frac{P_{o(\mathrm{ccm(max)})}}{2\pi f V_o^2\left(\Delta V_{o(\max)}/V_o\right)} \approx 1100\ \mu\mathrm{F}. \quad (48)$$

2) Parameters of the voltage controller: The zero of the PI controller is placed at 7.5 Hz, which is well below $2f = 100$ Hz [5]. The corresponding time constant $T_{PI} = 20$ ms. This ensures sufficient attenuation of 100 Hz ripple in the output voltage due to the integral part of (39).

In order to select K_{PI}, the distortion and the displacement terms in (41) are plotted against K_{PI} in Fig. 9(a) and (b), respectively, where I_2 is the total harmonic distortion factor (THD) and $\left[\cos(\tan^{-1}(I_2)\right]$ is the displacement factor. It is seen that compared to distortion factor, the displacement factor is less affected by K_{PI}. The parameter K_{PI} is set at 1 to keep the input current THD within 1%.

The parameters determined as above are used for simulation and also in the prototype presented in the following section.

IV. Simulation and Experimental Results

The proposed control concept is verified through simulation using MATLAB/SIMULINK and also experimentally on a 600-W prototype shown in Fig. 10. Due to availability, inductors $L_f = 6$ mH and $L_{b(dcm)} = 0.4$ mH are used in the experimental setup. The control circuit shown in Fig. 10 is implemented using discrete integrated circuits (ICs). The op-amp full-wave rectifier, amplifiers, voltage controller, comparators, summers and subtractors are implemented using op-amp (TL084) based analog circuits [14]. The input lowpass filter, when connected in the ac side (Fig. 10) handles fundamental current along with switching frequency current components. However, when it is placed in the dc side (as in Fig. 6), it carries dc, twice the line frequency and switching frequency current components. It is found that the placement of the filter in the ac side gives better input current waveform than its placement in the dc side. However, no such significant change is noticed for the inductor $L_{b(\mathrm{dcm})}$. In experimental setup, the inductors $L_{b(\mathrm{dcm})}$ and L_f and the filter capacitor C_f are connected in the

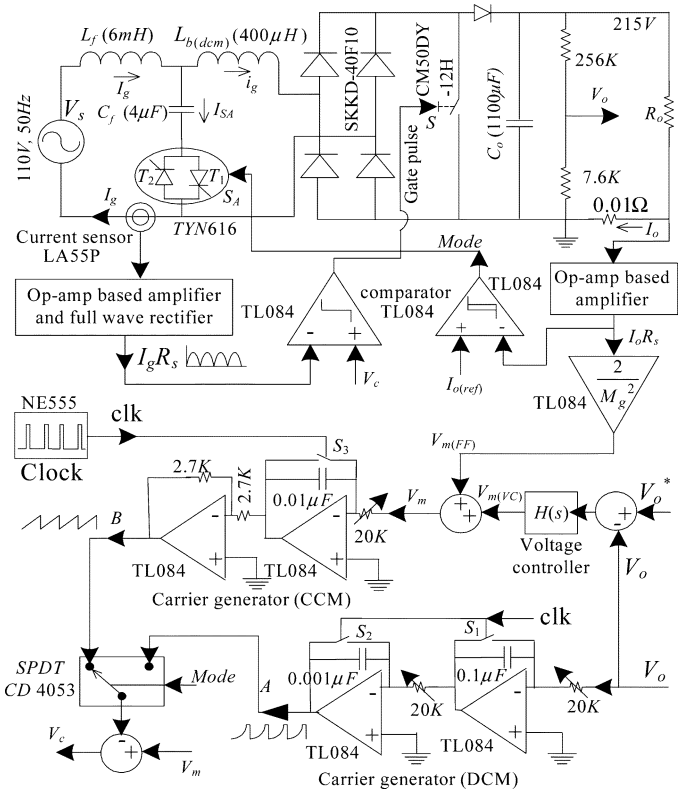

Fig. 10. Experimental setup.

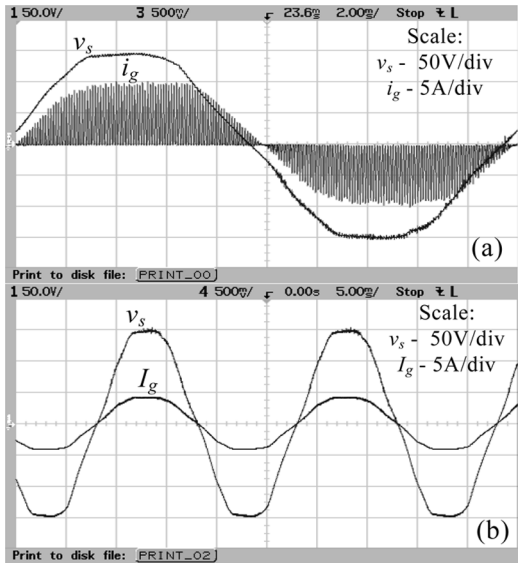

Fig. 11. (a) Input voltage and current through $L_{b(dcm)}$ (DCM) and (b) input voltage and input current (DCM).

ac side as seen in Fig. 10. The auxiliary switch S_A is realized by two anti-parallel thyristors T_1 and T_2 as shown. The input current I_g is measured using an isolated current sensor, while the output voltage and the load current are measured using resistor based sensors as shown.

A. Steady State Input Voltage and Current Under DCM

The steady state input voltage and input current waveforms, corresponding to 250 W output power are shown in Fig. 11. The converter is operated in DCM, where the auxiliary switch S_A is turned on and the nonlinear carrier A is selected. The input voltage and the current through the boost inductor $L_{b(\mathrm{dcm})}$ are shown in Fig. 11(a), while the input voltage and the input current are shown in Fig. 11(b). The input current THD and the input power factor are found to be 3.1% and 0.988, respectively.

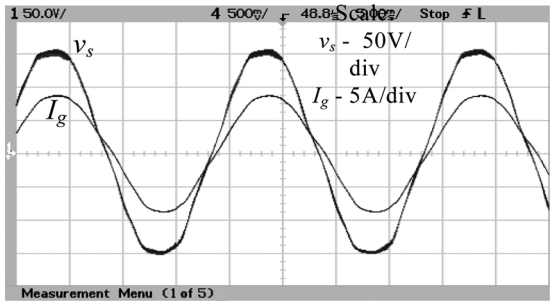

Fig. 12. Input voltage and input current (CCM).

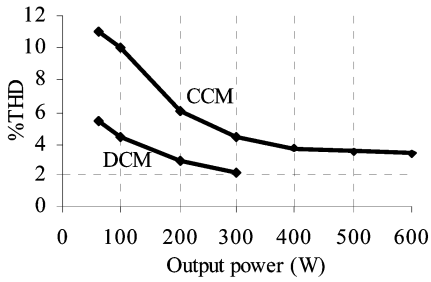

Fig. 13. Variation of input current THD (simulation).

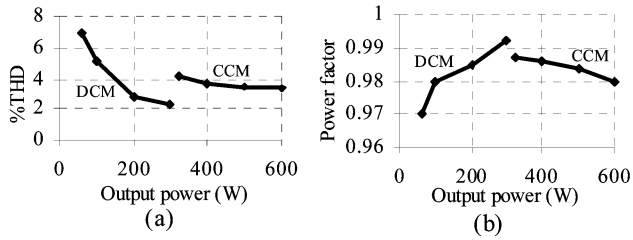

Fig. 14. (a) Variation of input current THD (experimental) and (b) variation of input power factor (experimental).

B. Steady State Input Voltage and Current Under CCM

The steady state input voltage and input current waveforms, corresponding to 600-W output power, are shown in Fig. 12. The converter is operated in CCM, where the auxiliary switch S_A is turned off and the linear carrier B is selected. The input current THD and the input power factor are found to be 3.3% and 0.98, respectively.

C. Variation of Input Power Factor and Input Current THD With Load

In order to observe the above performances, the output power of the converter is varied between 60 W and 600 W. Fig. 13 shows the variation of input current total harmonic distortion factor (THD) with load as obtained through simulation. The plot CCM in Fig. 13 is obtained with the converter operating in CCM at different loads over the entire load range with a 6.4 mH boost inductor. This may be compared against the plot DCM in

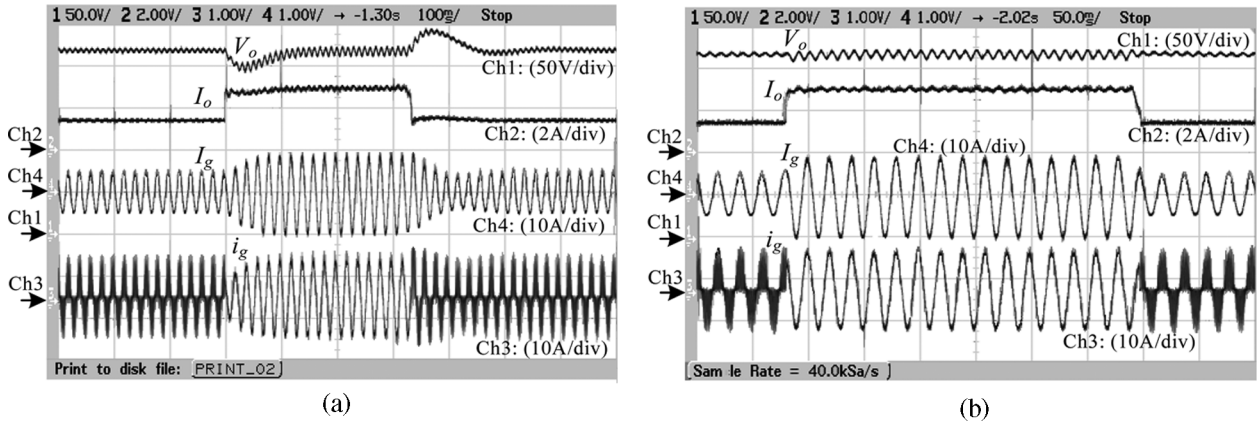

Fig. 15. Transient performance during step change in load: (a) without load current feedforward scheme and (b) with load current feedforward scheme.

the same figure. As seen the DCM operation leads to less input current distortion between 60-W and 300-W output power. The maximum input current THD under DCM operation is 5.5% (at 60 W). To obtain the same input current THD at 60-W load under CCM, the value of boost inductance required is 20 mH (as seen from simulation results).

The experimental variations of the measured input current THD and the input power factor for different loads are shown in Fig. 14(a) and (b), respectively. The THD increases as the load decreases. It can be seen that the proposed converter system is able to maintain a high power factor and low input current THD over the entire load range.

D. Dynamic Response of the Converter System

In order to test the dynamic response of the converter system, the output load is suddenly varied from 250 to 600 W and vice versa. Initially the converter is tested without using the load current feedforward scheme. The corresponding experimental results are shown in Fig. 15(a). The settling time of the output voltage response is found to be around 160 ms.

Now, the converter is tested with load current feedforward scheme. The corresponding experimental results are presented in Fig. 15(b). It can be seen that, compared to the previous case (i.e., without load current feedforward), there is no overshoot or undershoot found in the output voltage V_o. The response of the input current I_g as well as the inductor current i_g are also faster during the load changes.

It can be seen in Fig. 15(b) that the transitions between CCM and DCM modes are always smooth without any appreciable dynamics in the output voltage as well as in the input current I_g and the boost inductor current i_g. The peak device current stress under DCM operation is restricted to be close to the rated device current under CCM operation.

E. Voltage and Current Stress in the Auxiliary Switch S_A

The voltage V_{SA} across the auxiliary switch S_A and the current I_{SA} through the switch S_A are shown in Fig. 16. This may be required to select the proper voltage and current rating of the auxiliary switch S_A. The maximum possible voltage stress across S_A is $(V_{gm} + V_o)$. This can appear across S_A for a short duration, if the filter capacitor C_f is charged at the peak input voltage, just before the switch S_A is turned off. The maximum current stress in the switch S_A is same as the rated device current.

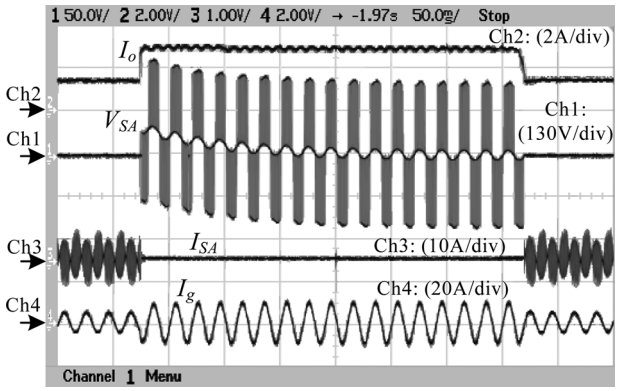

Fig. 16. Voltage stress V_{SA} and current stress I_{SA} in the auxiliary switch S_A.

V. Conclusion

A single-phase, constant-switching-frequency based rectifier system is presented for maintaining sinusoidal input current at near unity power factor under wide range of load variations. The above rectifier system is operated under DCM for output less than 330 W and in CCM for output greater than 330 W, exploiting the best features of both the operating modes.

The power circuit of the proposed converter can be configured either for DCM or for CCM by simple on–off control of an auxiliary switch. Similarly, the proposed control circuit can also be configured either for CCM or for DCM simply by choosing the appropriate carriers (a linear carrier for CCM and a nonlinear carrier for DCM). The measured load current is used to select the desired operating mode. The required switching instants are generated by comparing the measured input current with one of the above carriers in a modulator without using any multiplication, division, square root operation, and input voltage sensing.

All the necessary design equations are provided to select the passive components. The averaged model of the proposed rectifier system is presented. Using such model, a design guideline for selecting the parameters of the voltage controller is presented. A simple load current feedforward scheme is presented to improve the dynamic response of the system against sudden

change in loads. This also ensures a smooth transition from one operating mode to the other. The simulation and the experimental results show that the proposed rectifier system with mixed-mode operation gives better input current characteristics for a wide range of load variation compared to the case, when it is operated completely in CCM for the given load range.

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