A Method to Improve PLL Performance Under Abnormal Grid Conditions

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Abstract— Phase tracking system or phase locked loop (PLL) is an important part of the control unit of a grid connected power converter. Popular methods such as zero crossing detection (ZCD) and synchronous reference frame (SRF) PLL do not produce accurate phase information when grid is non-ideal. In this work a method to obtain accurate phase information when the grid voltages are unbalanced by adding a moving average filter to a SRF PLL has been proposed. The performances of the PLL have been experimentally verified for abnormal grid conditions such as unbalance, harmonics, voltage sag and swell, faults etc. Generally, during a fault phase voltages become unbalanced so this method can give better fault ride through capability to a power converter.

Index Terms— Phase locked loop (PLL), Grid connected converters, Synchronous reference frame (SRF), Moving average filter

I. INTRODUCTION

A phase locked loop is used in applications where tracking of phase and frequency of the incoming signal is necessary. For grid connected applications of power converters such as distributed generation and power quality improvement, a PLL is used to generate unit sine and cosine signals synchronized to system frequency from utility voltage. Closed loop control of power converters in synchronous reference frame method needs these unit sine and cosine signals to compute feedback and modulating signals. Generation of unit vectors face problems when undesirable conditions like unbalance, frequency variation, presence of harmonics, voltage sag and swell, faults, phase jump, line notching exist in the grid. The PLL has to track phase information accurately under non-ideal grid voltage condition also . So the job of a PLL can be stated as to track phase angle of the fundamental component of the positive sequence utility voltage.

PLL structures can be broadly classified into following three categories.

1) Zero crossing detection (ZCD) based PLL
2) Stationary reference frame based PLL
3) Synchronously rotating reference frame (SRF) based PLL

ZCD based PLL [1] is the simplest among all but it's performance becomes poorer if frequency variation or line notching is present. Stationary reference frame based PLL structure [2] is not capable of accurate phase tracking during unbalanced voltage condition. The well known SRF PLL [3],[4] works well under most abnormal grid conditions but during unbalance it's performance becomes poorer. Additional information of system frequency and voltage magnitude are obtained from this method. For accurate phase angle tracking under unbalanced condition many methods have already been proposed in literature. Extraction of phase angle using instantaneous pq theory [5] , through positive and negative sequence separation [6] and FIR filter based approach [7] are notable among them. Here in this work a simple method based on FIR digital filter to improve performance of SRF PLL under unbalanced phase voltage condition has been proposed. Performance of this PLL structure under single phase line to ground fault and other abnormal grid conditions have been investigated. Experimental results indicate a better performance of the proposed approach compared to the SRF PLL.

II. BASIC OPERATION OF THREE PHASE SRF PLL

Operation of a three phase SRF based PLL can be schematically shown in the Fig. 1. To obtain the phase information the
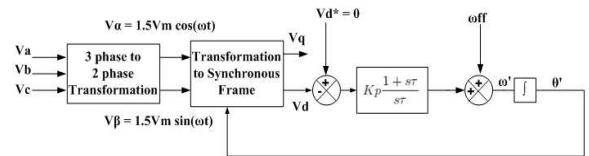

Fig. 1.   Basic structure of SRF PLL

three phase voltage signals (V_a, V_b and V_c) are transferred into stationary two phase system (V_α and V_β). Where,

$$V_a = V_m \cos(\omega t) \tag{1}$$

$$V_b = V_m \cos(\omega t - \frac{2\pi}{3}) \tag{2}$$

$$V_c = V_m \cos(\omega t - \frac{4\pi}{3}) \tag{3}$$

Now phase angle (θ) can be obtained by either synchronizing the voltage space vector(**V**, Fig. 2) along q axis or along d axis of synchronously rotating reference frame. Let us assume

that the voltage space vector is to be aligned with q axis (Fig. 2). Then position of d axis (θ) is related to ωt by

$$\theta = \omega t - \frac{\pi}{2} \qquad (4)$$

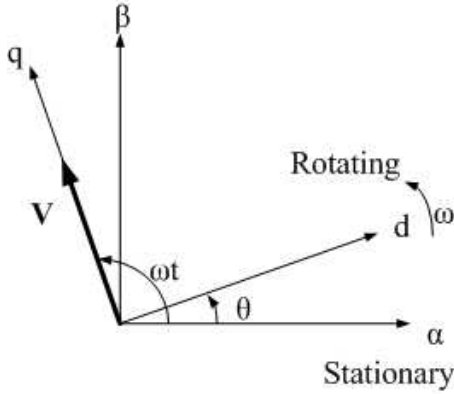In the PLL structure (Fig. 1) θ gets estimated as θ' by

Fig. 2.   Reference frames

integrating estimated frequency (ω') which is the summation of output of PI controller ($Kp\dfrac{1+s\tau}{s\tau}$) and the feedforward frequency (ω_{ff}). The voltage vectors in synchronously rotating reference frame can be found out using θ' from following equations.

$$V_d = -\frac{3}{2} V_m \, sin(\theta - \theta') \qquad (5)$$

$$V_q = \frac{3}{2} V_m \, cos(\theta - \theta') \qquad (6)$$

The controller gains are designed such that V_d follows reference value which will result in estimated frequency (ω') to lock to system frequency (ω) and estimated phase angle (θ') to be equal to the phase angle θ. Now if $\theta \approx \theta'$ then space vector of voltage gets aligned to q axis. The voltage vector along synchronously rotating d-axis (eqn. 5) can be expressed as follows.

$$V_d = -\frac{3}{2} V_m \, (\theta - \theta') \qquad (7)$$

So, overall system in Fig. 1 can be simplified to that shown in Fig 3. Detailed analysis and design of PI controller gains
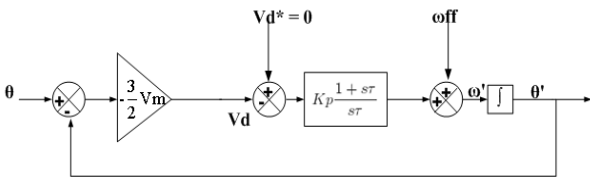

Fig. 3.   Simplified block diagram of SRF PLL

can be found in references [3] and [4].

III.   A SOLUTION TO THE PROBLEM DUE TO UNBALANCE

If phase voltages are unbalanced in a 50 Hz system then a ripple of 100 Hz will appear in d and q axis along with the DC quantities and this results in erroneous estimation of θ. If a low pass filter is used to filter the ripple then the system response becomes slower but with a moving average filter comaparatively faster system response and better attenuation is achievable which is shown next. A 1st order low pass filter has a transfer function of the form $\dfrac{1}{1 + \dfrac{s}{a}}$, where 'a' is the corner frequency. If a 100 Hz (628 rad/sec) component has to be filtered then for $a = 62.8$ rad/sec i.e. a corner frequency at 10 Hz would give 20 dB attenuation. A moving average filter is a simple FIR filter. If the signal containing 100 Hz component is sampled at a rate 1KHz and at every computational instant average of 10 samples (which includes the previous 9 samples) is calculated then output would not contain 100 Hz and it's integral harmonics upto 500 Hz (decided by Nyquist criteria). Transfer function of such a filter in discrete domain is given by

$$\begin{aligned} H(z) &= 0.1(1 + z^{-1} + z^{-2} + z^{-3} \\ &\quad + z^{-4} + z^{-5} + z^{-6} \\ &\quad + z^{-7} + z^{-8} + z^{-9}) \end{aligned} \qquad (8)$$

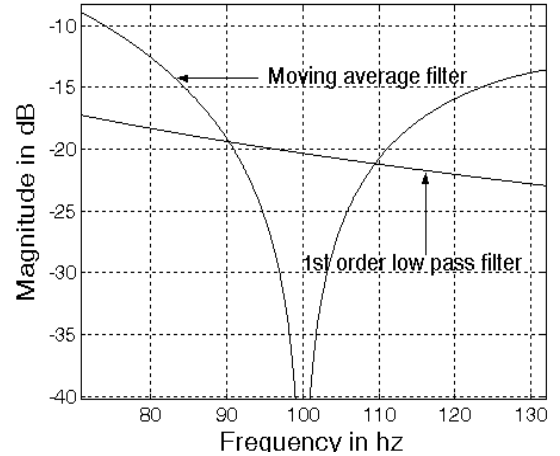Fig 4 shows the magnitude response of the two filters

Fig. 4.   Frequency responses of the filters around 100 Hz

around 100 Hz. It can be observed that for a wide range of frequency this moving average filter is capable of giving better attenuation. So even if there is a frequency variation in the grid side the performance of a moving average filter would not deteriorate. Fig 5 shows the frequency responses of the two filters. From the phase response plots it can be seen that this moving average filter is capable of giving higher phase margin (between frequencies of 10 rad/sec to 300 rad/sec) when coupled with the plant. Therefore with a moving average filter it is possible to design a PLL with more accuracy and higher bandwidth. The final simplified control block diagram is given
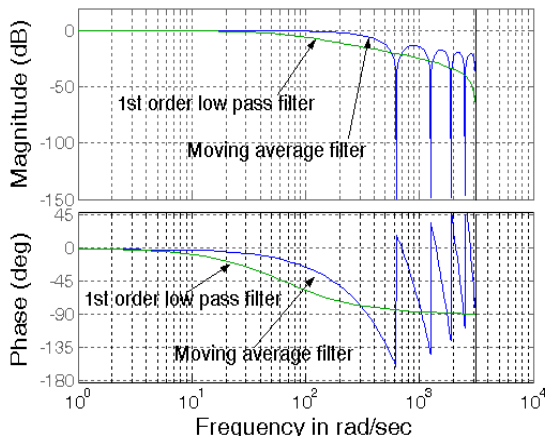
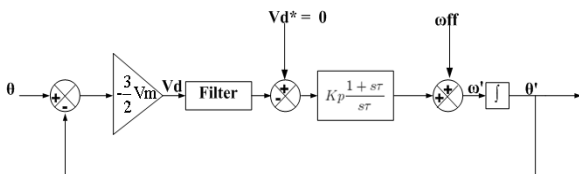Fig. 5. Frequency responses of the filters

Fig. 6. Final block diagram with filter

Fig. 7. Approximation of moving average filter with a 1st order system

Fig. 8. Bode plots of loop gain

in Fig. 6. Problem due to unbalance can also be avoided by using a notch filter whose notch frequency is around 100 Hz. Such a filter provides high attenuation around notch frequency and unity gain at other frequencies. Fig. 5 shows that the moving average filter is capable of providing high attenuation to 300 Hz (if 5th or 7th harmonic voltage is present in phase voltage 300Hz component will be present in d axis voltage). For such a situation accurate phase tracking is possible if the moving average filter is used. For switching frequency and other high frequency noises the loop gain provides enough high attenuation.

IV. DESIGN OF PI CONTROLLER GAINS

System chosen : 3 phase, 415 V, 50 Hz.
The following method was adopted to design the filter and PI controller.

1) First the moving average filter is approximated as a 1st order low pass filter. Here the lowest frequency to be filterd is 100 Hz. Sampling frequency for the filter is chosen as 1KHz (Time period = 10 ms). The time constant for the approximated 1st order low pass filter is taken as 10ms. Fig. 7 shows the comparative response between the two filters for a step input.
2) Using symmetrical optimum method [8] suitable value of Kp and τ can be calculated. The obtained values are approximate and are required for finding more exact values of Kp and τ. $Kp = 0.101$; $\tau = 0.04sec$;
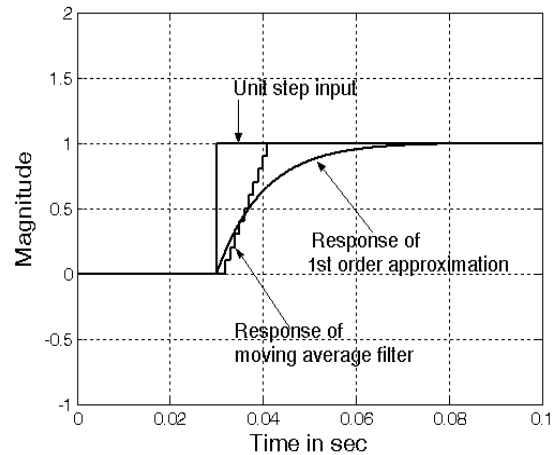3) The transfer function of the moving average filter is now
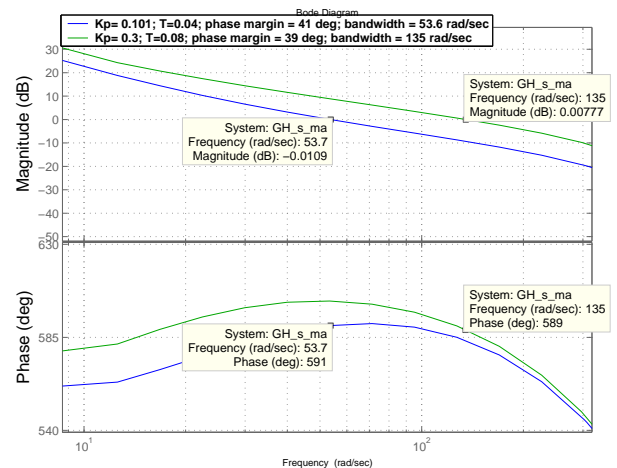
converted into 's' domain using bilinear transformation with prewraping at 100Hz (628 rad/sec).
4) With values of Kp and τ obtained in step 2 the loop gain (GH) of Fig. 6 is calculated. The frequency response of GH is plotted using MATLAB for both 1st order approximation and with moving average filter (Fig. 8).
5) From frequency response the bandwidth and phase margin is observed.
6) Now to achieve sufficient phase margin and higher bandwidth, value of Kp and τ is adjusted. During this fine tuning following things were considered

   - Lower value of τ ensures fast tracking.
   - Lower phase margin results in oscillatory response.
   - Value of Kp influences phase margin and changes bandwidth.

   Final values of controller parameters are $Kp = 0.3$ and $\tau = 0.08sec$ also $Phase margin = 39 deg$ and $Bandwidth = 135 rad/sec$.
7) By choosing a higher τ it is possible to achieve higher

bandwidth but settling time will increase.

V. EXPERIMENTAL RESULTS

The above discussed method has been implemented and tested for different conditions through MATLAB simulation as well as using a cyclone FPGA board. For experiments the required three phase voltage signals with controllable magnitude, phase and frequency have been generated using this board. The experimental results are given below.
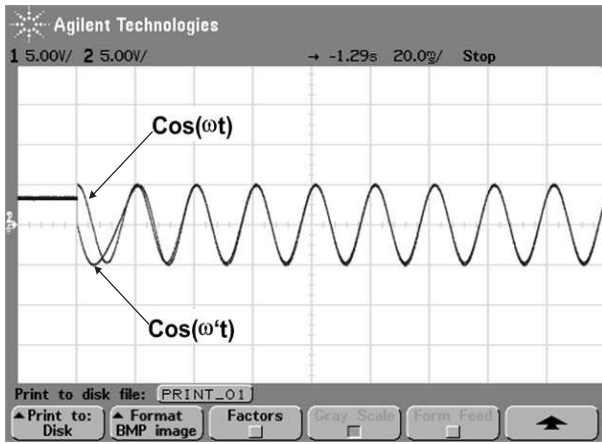
A. Balanced condition :

Fig. 9. Tracking of reference voltage under balanced condition (Scale: X-axis 20ms/div amd Y-axis 5V/div)

Fig. 9 shows operation of the moving average filter based PLL under balanced operating condition. Here Cos(ωt) is the R phase voltage signal and Cos(ω't) is genetrated from estimated value of θ using eqn. 4 and a look up table. In Fig. 10 the grid phase angle (ωt) and estimated phase angle (ω't) have been shown. The estimation of d and q axis voltages are shown in Fig. 11. It can be seen that during start up the tracking of phase angle is achieved within 60 ms. The controller parameters used here are $Kp = 0.3 \ and \ \tau = 0.08sec$.
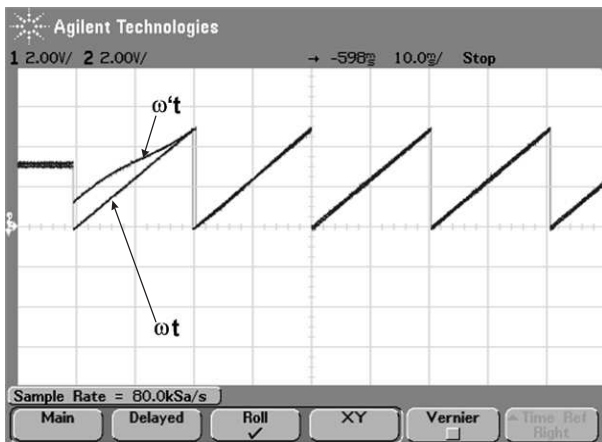

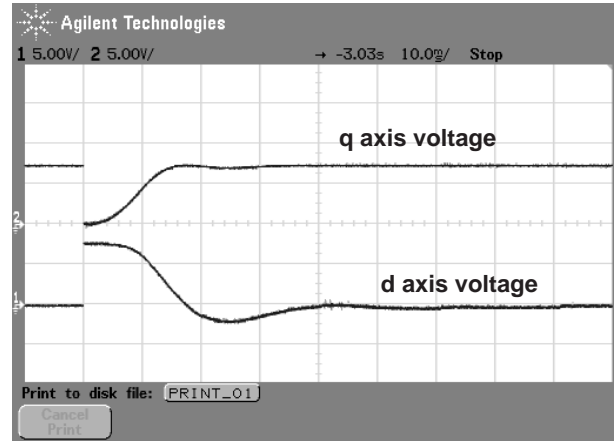Fig. 10. Tracking of grid phase angle (Scale: X-axis 10ms/div amd Y-axis 2V/div)

Fig. 11. Estimation of d and q axis voltages (Scale: X-axis 10ms/div amd Y-axis 5V/div)

B. Unbalanced condition :

Fig. 12 shows the 3 phase unbalanced voltage signals under which performance of the proposed PLL structure has been examined. Performances of this PLL have been compared with a SRF PLL under this condition also. The controller parameters are $Kp = 0.3 \ and \ \tau = 0.08sec$. The bandwidth of SRF PLL is 43 rad/sec whereas the bandwidth of the proposed PLL is 135 rad/sec.
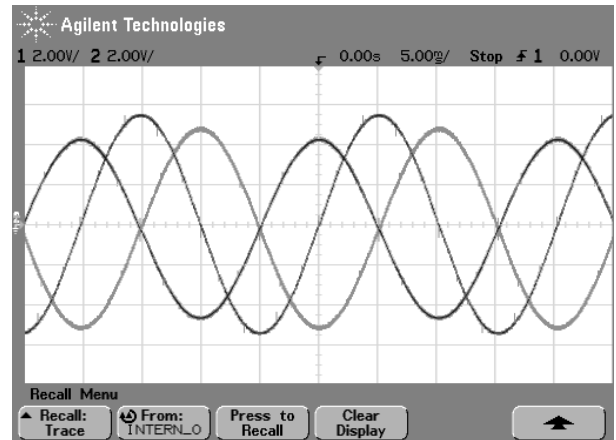

Fig. 12. Applied unbalanced voltages (Scale: X-axis 5ms/div amd Y-axis 2V/div)

Fig. 13 shows tracking of R phase voltage which is obatained within 3 fundamental cycles. In Fig. 14 the d axis voltage (Vd) which contains 100 Hz component and the output of moving average filter giving very high attenuation are shown under unbalanced situation.

The source frequency was kept at 50 Hz. Fig. 15 shows the estimation of the source frequency with moving average filter based SRF PLL and Fig. 16 shows frequency estimation with SRF PLL. The estimation in case of SRF PLL is erroneous as it contains 100 Hz ripple where in the proposed method Frequency is estimated accurately.
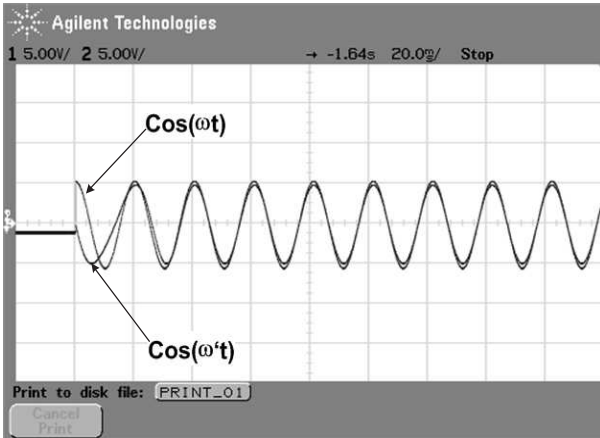
Fig. 13. Tracking of reference voltage under unbalanced condition (Scale: X-axis 20ms/div amd Y-axis 5V/div)
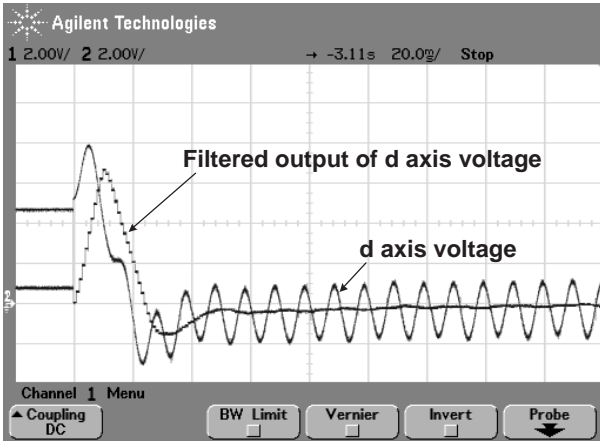

Fig. 14. Estimation of d axis voltage under unbalanced condition (Scale: X-axis 20ms/div amd Y-axis 2V/div)
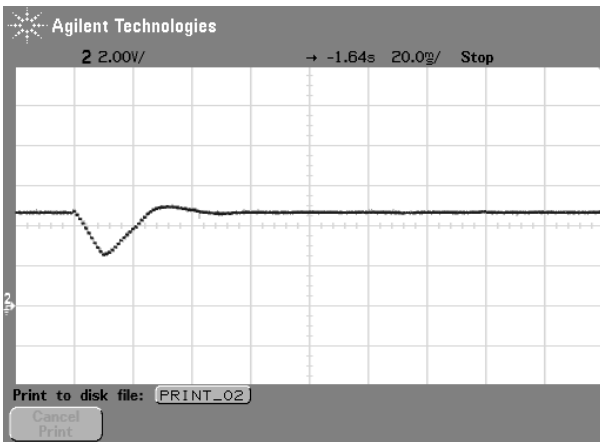

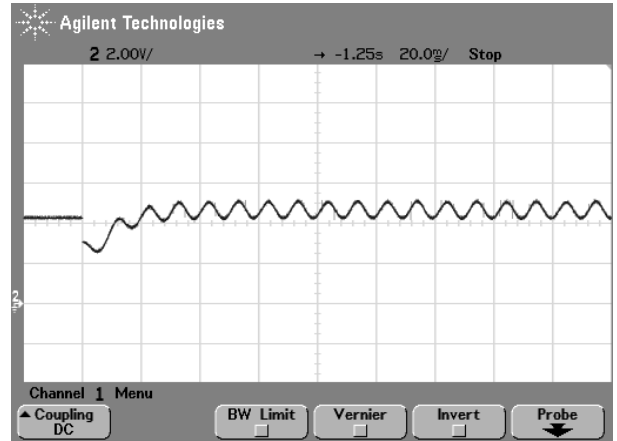Fig. 15. Estimation of frequency with proposed PLL (Scale: X-axis 20ms/div amd Y-axis 2V/div)

Fig. 16. Estimation of frequency with SRF PLL (Scale: X-axis 20ms/div amd Y-axis 2V/div)

though there would be attenuation provided by the integrator for estimating θ but as the estimated frequency in SRF PLL contains 100 Hz so the estimated θ will not be accurate (Fig. 18) . However in case of the proposed PLL, estimation of θ would be accurate (Fig. 17).
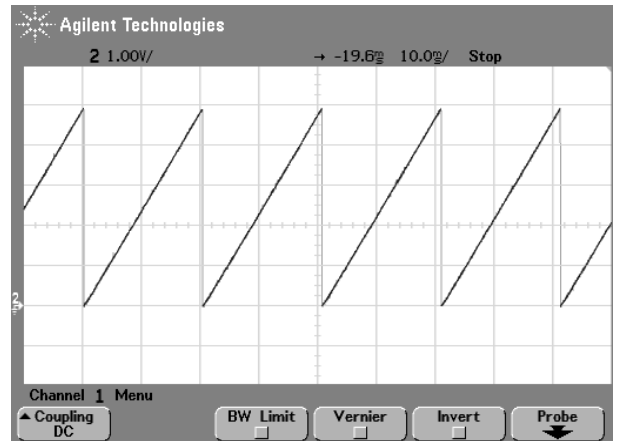

Fig. 17. Estimation of grid phase angle at steady state with proposed PLL (Scale: X-axis 10ms/div amd Y-axis 1V/div)

C. Presence of harmonics :

Because of transformation into synchronously rotating reference frame 5th and 7th harmonic voltages would create a ripple voltage of 300 Hz. As this moving average filter gives very high attenuation at 300 Hz or 1884 rad/sec (Fig. 5) so phase tracking would not get affected.

D. Frequency variation :

To test, performance of the proposed PLL during frequency variation supply frequency was given a step change from 50 hz to 40 Hz. The settling time was found to be 60 ms (Fig. 19). Experiment on SRF PLL with the same PI controller parameters shows similar result.
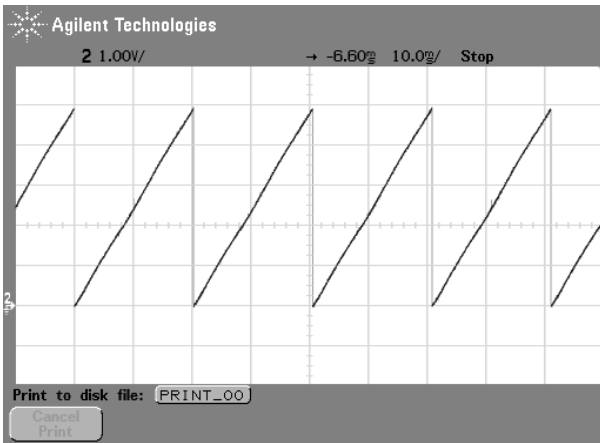
Fig. 18. Estimation of grid phase angle at steady state with SRF PLL (Scale: X-axis 10ms/div amd Y-axis 1V/div)
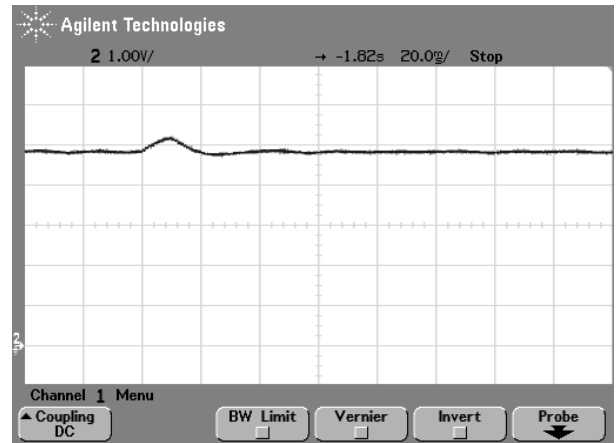

Fig. 20. Frequency tracking for a phase jump of 10 degree (Scale: X-axis 20ms/div amd Y-axis 1V/div)
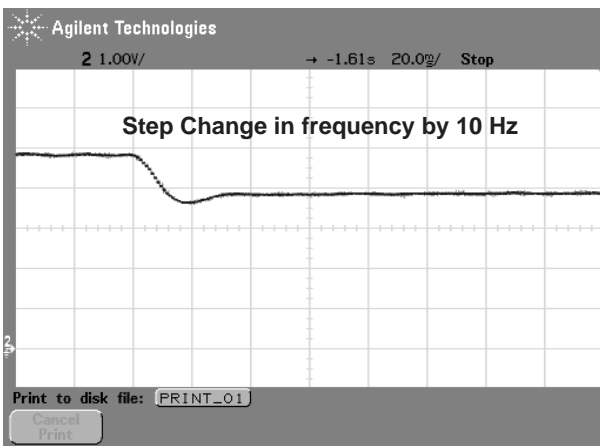

Fig. 19. Frequency tracking for a step change of 10 Hz (Scale: X-axis 20ms/div amd Y-axis 1V/div)
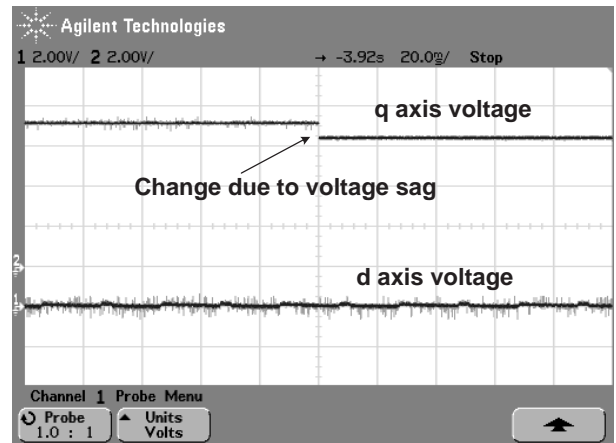

Fig. 21. D and q axis voltages during voltage sag (Scale: X-axis 20ms/div amd Y-axis 2V/div)

E. Phase jump :

Sudden phase change in load terminal voltage may occur if a large load is withdrawn from the supply system or due to faults in the grid [2]. To find performance of the proposed PLL under this situation a step change of 10 degree in system phase has been applied. The settling time was observed to be 0.06 sec (Fig. 20). Similar result was obtained for a SRF PLL with the same controller parameters.

F. Voltage sag :

Voltage sag or swell may occur in a supply system and generally they last for a few cycles. In experiment a sudden drop of voltage magnitude by 10% in all three phases were applied. As the PLL is already phase locked with the system so there was no change in d axis voltage and the q axis voltage accurately tracks the system voltage magnitude(Fig. 21). So no disturbance was observed in phase tracking. Also during voltage swell same result would be seen.

G. Single phase LG fault :

During single phase LG fault, voltage of the faulty phase becomes almost zero. The voltage is restored after the fault is cleared. During experiment Y phase voltage was made zero and the d axis voltage and it's filtered output are observed (Fig. 22). The filtered output reaches zero within 10 ms which indicates that it is able to track grid phase angle at this condition. Accurate tracking of grid phase angle under a neighbouring fault condition can enhance fault ride through capability of a power converter.

VI. CONCLUSION

In applications of grid connected power converter phase tracking is important. A PLL can be used to obtain magnitude, frequency and phase information of positive sequence fundamental component of grid voltage. Accurate and fast estimation of these quantities can be used for control and protection of power converter. Though frequency variation in grid is a slow process but fast estimation of frequency gives the option for a power converter to decide the necessary
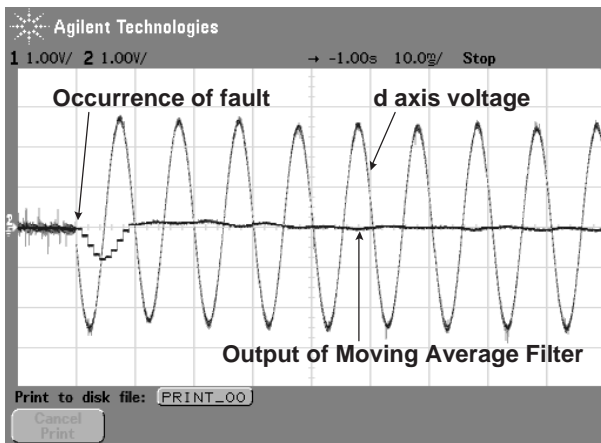
Fig. 22. Estimation of d axis voltages during single phase LG fault (Scale: X-axis 20ms/div amd Y-axis 2V/div)

course of action. Present technique of three phase SRF PLL has limitations in abnormal grid conditions. In this work a moving average based SRF PLL technique and it's design of PI controller gains have been discussed. It has been shown that under unbalanced situation this technique can give better results compared to a SRF PLL. It can be concluded that a moving average filtering method applied in a three phase SRF PLL structure would give a better performance under abnormal grid conditions.

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