High Precision 16-bit Readout Gas Sensor Interface in 0.13µm CMOS

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***Abstract*— A high precision 16-bit readout circuit for gas sensor interface is realized in 0.13µm CMOS technology. The front end signal conditioning circuit comprises a low power resistance – to – time period converter with subthreshold operation of transistors. The time-period proportional to the transducer output is digitized using a counter based frequency – to – digital conversion (FDC) technique. In order to handle the sensor signal with a dynamic range of 160dB, subranging technique is employed to provide feedback to front end circuit interfacing the sensor. While the 3 MSBs of 16-bit word restrict the input frequency to FDC between 1MHz and 10MHz, the 13-bit counter operates on this signal to provide a worst case resolution of 0.4%. The power consumption of the readout circuit is 366µW from a 1.2V supply.**

I. INTRODUCTION

Integrated CMOS sensors offer several advantages such as low cost, low power, small form factor, and high reliability. Sensor signals typically have low signal bandwidth (few Hz) [1], but may exhibit very wide dynamic range [2],[3]. Front end signal conditioning circuitry (FEC) must support the precision and dynamic range that is expected of the sensors. It is convenient to have frequency or time period of an RC relaxation oscillator as the analog output signal from such sensors for better linearity and ease of processing. The analog-to-digital conversion, which enables further signal processing in the digital domain, should not result in the degradation of the precision, but at the same time, support the wide dynamic range. A counter based frequency-to-digital converter (FDC) suits this purpose.

There have been reports on resistive gas sensor interface circuits [2],[4],[5]. In [2], a resistance – to – time period converter is used as the FEC where the frequency output, which is calibrated using a digital control, is readout through an external microcontroller. A logarithmic converter forms the FEC in [4]. Though this supports the wide dynamic range, it loses out on high precision. In [5], a trans-resistance amplifier followed by an ADC is used as the interface circuit. This results in significant area and power overhead. In this paper we report on a 16-bit readout gas sensor interface realized in 0.13µm UMC technology, with 0.4% resolution over a wide dynamic range of 160dB. FEC is realized as resistance – to – time period converter with subthreshold operation of transistors. The digital output is obtained from an on-chip FDC employing subranging technique. The circuit consumes 366µW.

The paper is organized as follows. The design of FEC is presented in section II. Section III deals with the FDC design. Signal – to – noise ratio of the FDC is analyzed in section IV. Concluding remarks are provided in section V.

II. FEC ARCHITECTURE

Resistance – to – time period conversion circuit is used for gas sensing (fig 1). The circuit has a current mirror charging/discharging a capacitor at its core. The current through the sensor film is mirrored onto the capacitor (C_1 or

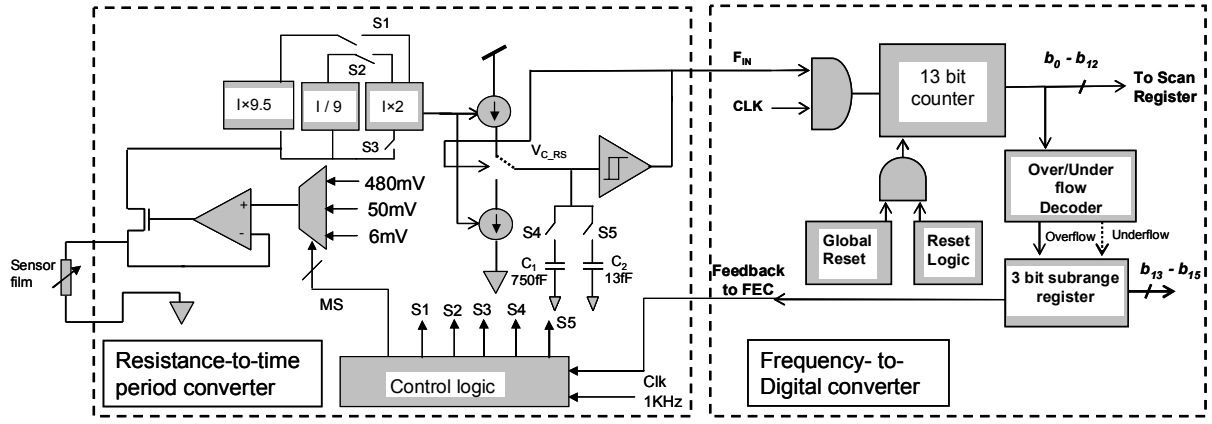

Figure 1. Block diagram of the readout circuit for gas sensor interface

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C_2). The current mirror operates for a large range of resistance in the subthreshold region, leading to low power consumption. The capacitor voltage is fed to a Schmitt trigger, which controls the charging/discharging paths. The resultant square wave output of the Schmitt trigger has its time-period proportional to the sensor resistance. The sensor resistance varies from 150Ω to 85MΩ with a resolution of 0.4% of the base value. Subranging technique is employed in this case, limiting the frequency of the sensor circuit to a band of 1MHz to 10MHz. The frequency feedback information is provided by the digital readout of the FDC to the control logic to select one of the three current scaling paths, one of the two capacitors (13fF and 750fF), and one of the three analog voltages (V_R = 480mV, 50mV and 6mV) such that the output frequency always lies in the designed band. For stability considerations, a slight overlap is used in the different bands.

The gas sensor readout circuit is shown in fig 2. The current through the sensor film is given as $I_{sensor} = V_{sensor} / R_{sensor}$. This current is mirrored onto the capacitor. Reverse body bias of -1V is applied to the NMOS transistors in the current mirror to enhance the subthreshold region. NMOS transistor in current mirror operates in subthreshold region over 99.4% of the entire resistance range. Cascode transistors are used to increase the output impedance. The current through the capacitor C is given as $I_c = C\,\Delta V / \Delta T$ where ΔV is the change in voltage across the capacitor, which is set by the Schmitt trigger threshold voltages (0.3V and 0.9V). ΔT is half the time-period of the Schmitt trigger output. I_c is limited to the range of 100nA to 10μA. As shown in fig 2, once the I_{sensor} crosses this band, the current is folded back to the designed band using the two current mirror circuits. S1, S2 and S3 are mutually exclusive switches, with S3 initially on. As shown in fig 2(a) and 2(b), if I_c exceeds 10μA, then S2 is turned on. Conversely, if I_c falls below 100nA, S1 is turned on. S5 and S4 are on for I_c ranges of 100nA to 1μA, and 1μA to 10μA respectively. The switches MS are simultaneously operated to set an appropriate V_R so that the output frequency always lies in the designed band.

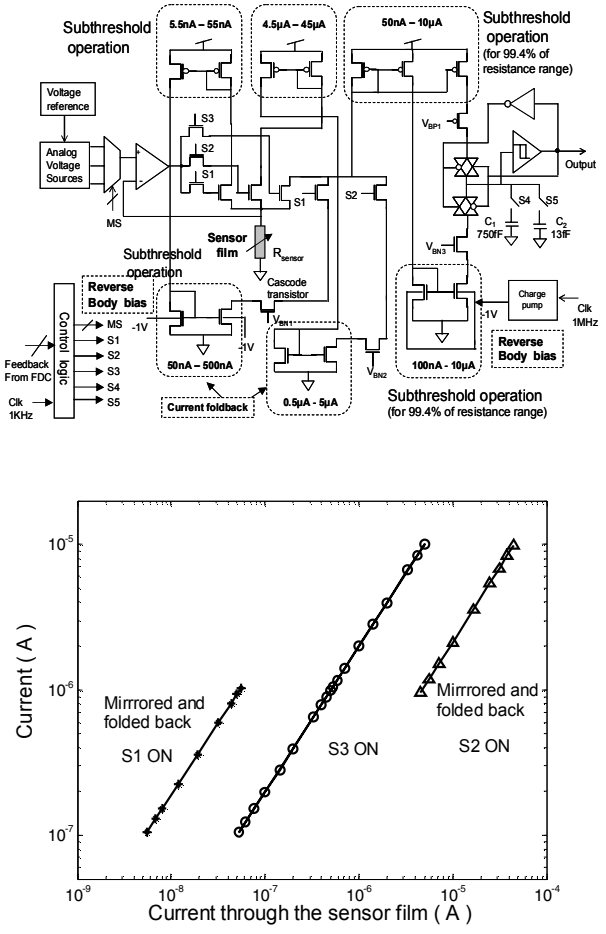

Figure 2. (a) Gas sensor readout circuit. (b) Mirrored and folded back current from the three scaling paths.

III. FDC ARCHITECTURE

The frequency output of FEC is digitized by the FDC block. The 16-bit FDC is implemented with 3 MSBs providing the subrange information and the 13 LSBs of the counter providing the required resolution (fig 1). The 13-bit synchronous counter is constructed with a clock frequency of 1KHz. Since the signal bandwidth (i.e. the rate of change of the input signal frequency) is low (few hundreds of mHz to a few Hz), a reference clock of 1KHz is acceptable. This corresponds to a worst case resolution of 0.2% (excluding the one-cycle count error). Whenever 13-bit counter overflows (underflows), the subrange register is incremented (decremented). Thus the 3-bit subrange register will take every decade range of frequencies and fold it back to a range between 1MHz and 10MHz, by providing feedback to FEC.

Fig 3. shows the control logic, which is implemented as a finite state machine, running on 1KHz clock. The subrange register bits are fed to two combinational logic blocks - an incrementer and a decrementer. Based on the overflow/ underflow information, outputs of one of the blocks form the D-inputs to the subrange register. If there is neither overflow

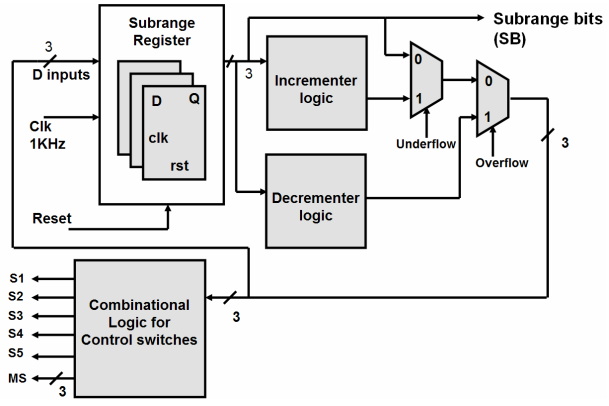

Figure 3. Control logic for the FEC signal conditioning.

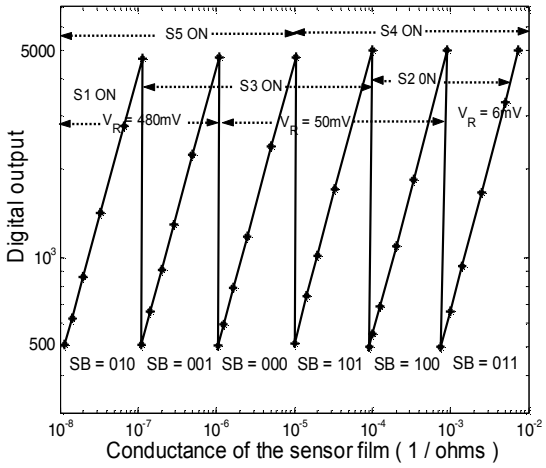

Figure 4. Digital code versus the conductance of the sensor film

nor underflow, then the present outputs (Q) are fedback as D-inputs. Thus the same state will be retained till there is either an underflow or an overflow. The combinational logic for the control switches is obtained from the D-inputs of the register.

The digital output, showing the subranging, is plotted against the conductance of the sensor film in fig 4. The maximum DNL is ±1LSB (1 LSB corresponds to 2KHz). This is due to the one cycle count error. The integral nonlinearity (INL) is observed to be ± 1 LSB (in a subrange). Thus the FDC provides a worst case resolution of 0.4% over the resistance range of 150Ω to 85MΩ, corresponding to 163dB dynamic range ($20\log_{10}$ (85M/(0.4% of 150)) = 163dB).

Fig 5 shows the micrograph of the chip realized in 0.13µm CMOS 1P8M technology. The total area consumed (FEC + FDC) is 30215µm^2. The power consumption is 366µW from a 1.2V supply.

IV. Signal to Noise And Distortion Ratio (SNDR)

The input signal range to FDC is from 1MHz to 10MHz (in a subrange). The resolution or step size in this band is

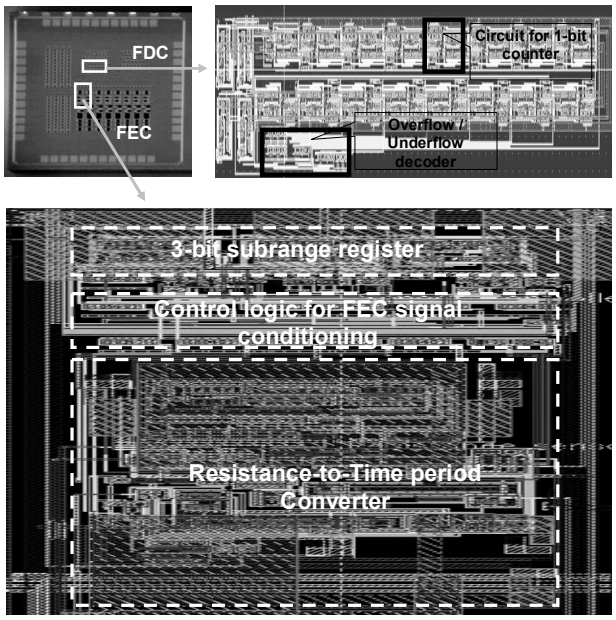

Figure 5. Chip micrograph with layout details of FEC and FDC. The chip has 8 readout channels for interfacing with a sensor array.

4KHz. Considering only the quantization noise, the signal to noise ratio is given as

$$SNR = 10\log_{10}\left(\frac{\left(9M/2\sqrt{2}\right)^2}{(4K)^2/12}\right) = 68.8\ dB \quad (1)$$

The effective number of bits (ENOB) is calculated to be 14.13 bits for the 16-bit FDC.

MATLAB simulations were performed to validate the above result. The input signal is a pulse waveform whose frequency varies by 0.5MHz about the mean value of 1.5MHz at the rate of 50 Hz. Mathematically, the frequency of the pulse waveform is given as

$$f_{in} = (1.5MHz) + (0.5MHz)\sin(2\pi.50.t) \quad (2)$$

TABLE I

PERFORMANCE COMPARISON OF RECENT RESISTANCE READOUT CIRCUITS

Parameter	Value			
	This work	***M.Malfatti et al 2006 [2]***	***D.Barrettino et al 2004 [4]***	***M.Grassi et al. 2005 [5]***
Sensing scheme	R → T conversion	R → T conversion	(Log R) → V conversion	R → V conversion + ADC
Input range	150Ω – 85MΩ	500KΩ – 1GΩ	1KΩ - 10MΩ	100Ω - 10MΩ
Dynamic range	163 dB	115dB	-	-
Supply voltage	1.2V	3.3V	5V	3.3V
Power dissipation	326µW	3.1mW	-	< 5mW
Area Consumed	12000µm^2	-	-	1.625mm^2
CMOS Technology	0.13µm	0.35µm	0.8µm	0.35µm

TABLE II

PERFORMANCE AND COMPARISON OF RECENT TIME-TO-DIGITAL CONVERTERS

Parameter	Value				
	This work	***P. Chen et al. 2005 [1]***	***K.Karadamoglou et al. 2004 [6]***	***C.Hwang et al 2004 [7]***	***E.R.Ruotsalainen et al. 2000 [8]***
Input range	150Ω - 85MΩ (converted to time : 0.1μs - 1μs)	0^0C - 100^0C (converted to time)	50 ps - 2.048μs	-	10ns – 2.5 μs
Dynamic range	163dB	55. 91dB	92.2 dB	-	97.86dB
Precision	4KHz in 1MHz – 10 MHz band	0.16^0C	50ps – 1ns	-	32ps
No. of bits	16-bit	10-bit	11-bit	-	-
DNL	±1 LSB (2KHz)	-	-	± 0.55 LSB	-
INL	±1 LSB (2KHz)	-	±1 LSB	+1 to -1.5 LSB	± 0.156 LSB
Estimated SNDR	68.8 dB (in a subrange)	-	-	-	-
SFDR	> 55.85 dB	-	-	-	-
Estimated ENOB	14.13	-	-	-	-
Supply voltage	1.2V	3.3V	5V	3.3V	5V
Power dissipation	40μW	490μW	< 10mW	< 50mW	350mW
Refresh time	1ms	1ms	-	-	< 6.3 μs
Area Consumed	18215μm^2	0.175mm^2	-	0.6mm^2	11.9mm^2 (including pads)
CMOS Technology	0.13μm	0.35μm	0.8μm	0.35μm	0.8μm

The counter output data is collected at the rate of 1KHz. 1K points are collected for FFT computation. Equation (1) is valid under the condition that the time resolution is infinite. The computation time increases exponentially with the increase in time resolution. Hence, in Matlab, input sampling frequency of 150MHz was used, corresponding to time step of 6.67ns. This discretization in time leads to clipping of the signal at higher frequencies leading to a saturated count value. This results in harmonic distortion. It is observed that both SNDR and Spurious Free Dynamic Range (SFDR) improve with the increase in sampling rate used in Matlab. The SNDR obtained for 1MHz swing is 46.1dB and the SFDR obtained is 55.85dB. The SNDR for full scale input (9MHz amplitude) is calculated to be 65dB. It is expected that with further increase in the sampling rate, the SNDR would approach the ideal value of 68.8dB. The chip testing is under progress to validate this.

The performance of the designed FEC (obtained through SPICE simulations) is benchmarked against some of the recent reports in the literature (Table I). There is a significant reduction in power consumption due to subthreshold operation of transistors. Considering the power and area metrics, the FDC performance is superior to other published reports, as seen in Table II.

V. CONCLUSION

The design and implementation of readout circuit with a dynamic range of 160dB is presented for gas sensor interface. The subthreshold operation of the transistors in the front end signal conditioning circuit results in a low power implementation. Subranging technique is employed to cover the wide dynamic range with high linearity. The 16-bit FDC has an accuracy of 0.4% in the subrange of 1MHz – 10MHz. ENOB is estimated to be 14.13 bits. The designed FDC can also be used in low power, low bandwidth, wide dynamic range and high precision sensor applications.

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