Design of High Performance Two Stage CMOS Cascode Op-Amps with Stable Biasing

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Abstract

The technique of mirror biasing is introduced and applied to a very high gain two stage CMOS cascode op-amp, in order to desensitize its output voltage to bias variations. Various performance metrics like low frequency common mode and power supply rejection ratios, slew rate and the sensitivity of the systematic offset are substantially improved. The improved performance is theoretically predicted and substantiated through circuit simulations.

1 Introduction

In a wide variety of CMOS analog circuits such as switched capacitor filters and A/D and D/A converters, accuracy is determined by the d.c. gain of the op-amps [1], [2]. Cascoding and the use of more than one gain stage are well-known techniques for boosting the gain of a CMOS op-amp [3]. Thus, for very high gain applications, a two stage cascode op-amp is an appropriate topology.

In a two stage cascode op-amp a number of transistors are externally biased and the operating point of the op-amp is very sensitive to these biases and the transistor sizes. Because of this, the sensitivity of the systematic offset of the op-amp is high. Since the output voltage is sensitive to common mode signals and the supply voltages, the common mode rejection ratio (CMRR) and the power supply rejection ratio (PSRR) of a two stage op-amp are low.

In this paper we introduce the notion of mirror biasing and apply it to two stage CMOS cascode op-amps in order to desensitize its operating point to bias and parameter variations. The idea is adapted from [4] and [5] which deal with folded cascode op-amps which is the topology of choice for moderate gain and high speed. The basic idea of mirror biasing is to avoid external biasing of the transistors but instead creating self-biased mirror pairs in which the mirror transistor is diode connected. This reduces the sensitivity of

the operating point to the bias variations by rejecting common mode signals while maintaining the high differential mode gain of an externally biased transistor. As a result the sensitivity of the systematic offset is reduced and the PSRR and CMRR are increased. An additional advantage of mirror biasing is that it increases the slew rate and hence, settling time of the op-amp. While the technique has been applied here for a two stage cascode op-amp it is easily applied to the large class of two stage op-amps of which the circuit dealt with in this paper is a super circuit [6] and comparator circuits.

The paper is organized as follows. In section 2 we discuss about mirror biasing of cascode second stage of a two stage op-amp. Small signal analysis is used to quantify the degree of operating point stability and improvement of CMRR and PSRR provided by mirror biasing. In section 3 the topology of the new mirror biased two stage cascode op-amp is synthesized. Simulation results to support the qualitative arguments are given in section 4, while section 5 summarizes the work.

2 Mirror Biasing of Cascode Second Stage

In this section we first highlight the high sensitivity of the node voltages of a standard cascode op-amp. Next we describe desensitization of the quiescent values of node voltages by the use of mirror biasing. We also discuss how mirror biasing reduces common mode gain and power supply gain and hence, improves CMRR and PSRR.

Throughout this paper transconductance, drain conductance and the aspect ratio of the gate area of transistor M_i are denoted by g_{mi} , g_{di} and $r_i (= \frac{W_i}{L_i})$ respectively.

In fig-1(a) the cascode second stage of a two stage op-amp is shown. In this circuit the transistors M_{12}

Figure 1: Cascode second stage: (a) with external bias, (b) with mirror bias.

and M_{13} form a cascode load circuit and the transistors M_{14} and M_{15} form a cascode gain circuit. The input of this circuit is fed at the gate of the transistor M_{15} from the positive output of the input stage of the op-amp. Traditionally, the transistors M_{12} , M_{13} and M_{14} are externally biased [6]. Using small signal analysis [3] (with the valid assumption $g_{mi} \gg g_{di}$), we get the sensitivity of the quiescent output voltage to the the gate to source voltage of the transistor M_{15} as,

$$\left| \frac{\partial V_O}{\partial (V_{dd} - V_{in})} \right| = \frac{g_{m15}}{\left(g_{d15} \cdot \frac{g_{d14}}{g_{m14}} + g_{d12} \cdot \frac{g_{d13}}{g_{m13}} \right)}$$

For equal g_{mi} and equal g_{di} of all the four transistors,

$$\left| \frac{\partial V_O}{\partial (V_{dd} - V_{in})} \right| = \frac{1}{2} \left(\frac{g_m}{g_d} \right)^2 \quad (1)$$

This equation shows the high sensitivity of the output voltage to V_{in} which is important to get high differential mode gain of the op-amp. Similarly, V_O is highly sensitive to V_{b1} , V_{b2} , V_{b3} and the transistor sizes.

It is important to note that the same equation (1) gives the positive power supply gain and the common mode gain of the second stage. Since, these two gains are equal to the differential mode gain of the second stage, this stage has no contribution in CMRR and PSRR and hence, CMRR and PSRR of the two stage op-amp are low.

Mirror biasing involves the creation of mirror pairs in which one of the transistors is diode connected. In such a configuration the diode connected transistor

provides the low impedance necessary for low sensitivity of the operating point to common mode variation while the other transistor maintain high differential mode gain. To bias the transistors M_{14} , M_{13} and M_{12} a dummy output stage is constructed and mirrored with the actual output stage (ref. fig 1(b)). In the dummy output stage the transistors $M_{12a} - M_{15a}$ are respectively matched with the transistors $M_{12} - M_{15}$ with the same ratio, say $1 : m$. Typically m will be greater than 1 since the actual output stage has to drive a load but the dummy output stage does not. In the dummy output stage the transistor M_{18} is introduced to get sufficient output swing. The input of the dummy output stage is connected to the negative output of the input stage of the op-amp. The relationship that is maintained between the actual and dummy inputs is depicted by a buffer/inverter [5] in the figure. This block is a buffer for quiescent voltage and common mode signals and is an inverter for differential inputs. Using small signal analysis of the mirror biased second stage, the sensitivity of the output voltage to the common mode variation in $(V_{dd} - V_{in})$ can be obtained. With the same simplifying assumption $g_{mi} \gg g_{di}$, the sensitivity is

$$\begin{aligned} \frac{\partial V_O}{\partial (V_{dd} - V_{in})} &= \frac{g_{m15} (g_{m12} + g_{m13})}{g_{m12} g_{m13}} \\ &+ \frac{g_{m15}}{g_{m18}} \cdot \frac{g_{d14} g_{d15} / g_{m14}}{\left(g_{d15} \cdot \frac{g_{d14}}{g_{m14}} + g_{d12} \cdot \frac{g_{d13}}{g_{m13}} \right)}. \end{aligned}$$

For equal g_{mi} and g_{di} of all the transistors,

$$\frac{\partial V_O}{\partial (V_{dd} - V_{in})} = \frac{5}{2} \quad (2)$$

This sensitivity is a factor of $5 \left(\frac{g_d}{g_m} \right)^2$ less than the corresponding sensitivities for the externally biased op-amp. Because of the low sensitivity of the output quiescent voltage, the sensitivity of the systematic offset of the mirror biased op-amp is much smaller than that of the externally biased op-amp. Further, equations (1) and (2) show that the low frequency common mode gain and power supply gain of the mirror biased op-amp is less than those of the externally biased op-amp by a factor of $5 \left(\frac{g_d}{g_m} \right)^2$.

3 Mirror Biased Two Stage Cascode Op-amp

The mirror biased two stage cascode op-amp circuit is shown in fig-2. In the circuit the transistors M_{16a} and M_{17a} form the dummy level shifter. The

Figure 2: Mirror biased cascode op-amp.

two transistors M_{16a} and M_{17a} are matched, respectively, with the transistors M_{16} and M_{17} in the actual level shifter. This dummy level shifter helps to provide equal quiescent voltages and differential signals of opposite phase to the inputs of the two output stages (the actual and the dummy). In the input stage of the op-amp, transistors M_5 and M_7 in the negative half are diode connected. So for differential inputs the gain of this negative half is much less (by a factor of $\left(\frac{g_d}{g_m}\right)^2$) than that of the positive half of the input stage and, hence, the amplitude of the signal at node 4 is much smaller than that at node 3. Hence, with this implementation, the buffer/inverter (ref. fig-1(b)) is an inverter with high attenuation factor for differential inputs. Due to the high attenuation factor of the buffer/inverter effectively no signal is coming to the gates of the transistors M_{14} , M_{13} and M_{12} through the dummy output stage. Hence, over a large frequency range the differential a.c. characteristics of the externally biased and mirror biased op-amps are the same. As previously discussed, the common mode gain and power supply gain are substantially reduced. Further, the slew rate of the op-amp is also improved. This is because the current in the dummy output stage is mirrored into the actual output stage and increases the load current.

4 Simulation Results

In the previous sections we have given qualitative arguments about the improvement of the op-amp per-

formance by the use of mirror biasing. Here we give Spice3 simulation results to support these arguments. Through simulation, the mirror biased op-amp is compared with the standard topology [6] biased with a standard bias circuit [3]. The operating point and the transistor sizes of the two circuits are taken to be the same. In the simulation, Spice BISM transistor model with hp 1.2μ CMOS process parameters (available through MOSIS) are used.

We did not do any rigorous parametric design to pick the design point for simulation comparison. We took the lengths of all of the transistors at the minimum possible value for the used technology (i.e. 1.2μ). To get high gain and slew rate we took $r_i (= \frac{W_i}{L_i})$ equal to 50 for all of the transistors in the circuit with some exceptions. The ratio of the dummy and actual output stages is 1:4. The size r_{15} was taken to be 70 to satisfy the balance equation which reduces the systematic offset of the standard topology and the size r_{18} was taken to be 2.5 to get a reasonable output swing. In the bias circuit we took $r_{b1} = 1.5$ and $I_{bias} = 10\mu A$. The supply voltages are $\pm 5V$. The load capacitor and the compensating capacitor are 10pf and 6pf respectively.

The simulation results are given in Table-1. Note that the low frequency gain ($A(0)$) and the phase margin (PM) are equal for both circuits while the unity gain frequency (UGF) is better in the mirror biased op-amp. The common mode range (CMR) and the output swing (OS) are equal. At low frequency the common mode rejection ratio (CMRR) and the power

Responses	Mirror Bias	Stand. Bias
A(0)(db)	94	94
PM (deg.)	72	72
UGF (Mhz)	38	26
CMRR @ 0Hz (db)	120	79
CMRR @ 10kHz (db)	98	79
PSRR @ 0Hz (db)	102	74
PSRR @ 10kHz (db)	78	72
PD (mW)	25.5	22.4
CMR (V)	-4.3, 3.1	-4.3, 3.1
OS (V)	-4.3, 4.2	-4.3, 4.2
SR (V/ μ sec.)	-71, 158	-48, 102
0.1% ST (nsec.) (1V step)	80, 44	90, 60

Table 1: Comparison of the mirror biased and the standard externally biased two stage cascode op-amps.

supply rejection ratio (PSRR) of the mirror biased op-amp are much better than that of the standard externally biased op-amp, though, in the high frequency range the CMRR and the PSRR of the two circuits are equal. The mirror biased op-amp has 48% higher negative slew rate (SR) and 55% higher positive slew rate than that of the externally biased op-amp. Due to the higher slew rate of the mirror biased op-amp its settling time (ST) is less.

In order to highlight the desensitization of the systematic offset to bias and parameter variations, its sensitivity to the bias current was measured for both circuits. For the mirror biased op-amp the sensitivity is 1.65 V/A while for the standard topology it is 45 times larger. While the mirror biased op-amp provides the above mentioned performance improvements, its power dissipation is 14% more than that in the externally biased op-amp.

5 Summary

We have introduced the technique of mirror biasing and applied it to a two stage CMOS cascode op-amp in order to desensitize its operating point to bias variations. As a result, the sensitivity of the systematic offset of the op-amp is drastically reduced.

Mirror biasing is based on the use of self-biased mirror pairs in which one transistor provides the high impedance necessary for good a.c. performance while the other transistor provides the low impedance which is necessary for operating point desensitization and reduction of common mode gain and power supply gain. The large degree of desensitization provided by mir-

ror biasing has been quantified through small signal analysis.

The technique of mirror biasing has been applied to a two-stage cascode op-amp by creating dummy level shifter and output stages. The use of these dummy stages contributes to improved slew rate and settling time in comparison with standard externally biased cascode op-amps. These performance improvements have been achieved at the cost of a small increase in the power dissipation.

Since matched transistors are crucial to the successful application of mirror biasing, it is clear that mismatches created by process variations will reduce the gains documented in this work. Mismatch is however a well known problem in op-amp design and the numerous techniques that are available to minimize it are equally applicable to this work.

While the technique of mirror biasing has been applied in this work to a two stage cascode op-amp, it is equally applicable to all two stage op-amps and comparator circuits.

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