A Simple Analog Controller for Single-Phase Half-Bridge Rectifier

Rajesh Ghosh and G. Narayanan, *Member, IEEE*

***Abstract*—A simple analog controller is proposed for the single-phase half-bridge pulsewidth modulation rectifier to maintain near unity power factor at the input and balance the voltages across each half of the dc bus. The controller works in the principle of constant-frequency current programmed control. The required gating pulses are generated by comparing the input current with a linear and bipolar carrier without sensing the input voltage. Two voltage controllers and a single reset-integrator are used to generate the carrier. All the necessary control operations are performed without using any phase locked loop, multiplier, and/or divider circuits. Resistor based sensors are used to measure the voltages across two halves of the dc bus and the input current. The controller can be fabricated as a single integrated circuit. The averaged small signal models and all the necessary design equations are provided. The condition of stability against subharmonic oscillation is analyzed. Calculation of switching and conduction losses is presented. The control concept is validated through simulation and also experimentally on an 800-W half-bridge rectifier. Experimental results are presented for ac–dc application, and also for ac–dc–ac application with both linear and nonlinear loads at two different output fundamental frequencies (50 and 60 Hz).**

***Index Terms*—AC–DC conversion, current mode control, half-bridge converter, nonlinear carrier control, one-cycle control, power factor correction (PFC), single-phase uninterruptible power supply (UPS), transformerless UPS.**

I. Introduction

SINGLE-PHASE, ac–dc pulsewidth modulation (PWM) converters are increasingly replacing diode-bridge rectifiers in many power electronic applications to meet the necessary harmonic standards such as IEEE-519 [1] and IEC 1000-3-2 [2]. Some of the applications are ac–dc power supply, battery charger, uninterruptible power supply (UPS) systems, static frequency conversion, high input power factor ac line conditioning and single-phase to three-phase power conversion.

A number of PWM converter topologies such as half-bridge and full-bridge with power factor correction (PFC) feature have been reported [3], [4]. Compared to full-bridge topology, a half-bridge topology Fig. 1(a) has simpler power conversion circuit and fewer switching devices [4]. The converter efficiency may be expected to be higher because of a single semiconductor voltage drop at any instant of time [4].

A half-bridge topology behaves as a voltage-doubling rectifier [5] and is well suited in applications requiring a high dc bus voltage as shown in Fig. 1. Fig. 1(b) shows a single-phase transformerless UPS system. The back-to-back connection of two half-bridge topologies makes the input-output neutral connection easier without using a bulky isolation transformer [6], [7]. The same topology Fig. 1(b), (except for the battery interface) is extensively used in single-phase ac line conditioner and frequency changer applications [8]. Similarly, single-phase power can be converted into three-phase power using an eight-switch topology as shown in Fig. 1(c) for motor drives applications [9]. The main challenges associated with the half-bridge rectifier control are 1) to maintain sinusoidal input current at near unity power factor, 2) to hold the dc bus voltage at the desired reference value, and 3) to maintain balance between the voltages across each half of the dc bus [4], [5].

Compared to voltage mode control [8], a current mode control offers inherent overcurrent protection capability [4]–[7]. In current mode control there is an outer voltage loop, which sets the current reference for the inner current loop. A current controller is used to force the input current to follow the reference current. Some of the reported current mode control techniques are 1) fixed-frequency current mode control [10] and 2) fixed-band hysteresis current control [4], [5]. Hysteresis control results in a wide variation of switching frequency (e.g., 9–40 kHz.) [4], which makes the electromagnetic interference (EMI) filter design difficult [8]. Both of the above techniques use input and output voltage sensing along with input current sensing. These also use complex mathematic operations like division and/or multiplications to determine the converter switching instants. Some techniques involve a phase locked loop (PLL), generation of unit vectors and linear transformation [11], adding to the complexity of the controller. Programmable logic devices [12] and digital signal processor (DSP) based controller have been used [6] for control implementation in digital domain.

The main issues associated with the control of converter are a) control structure, b) complex mathematic operation, c) number of sensing points, d) generation of unit vectors, e) variable switching frequency, and f) overcurrent protection, and g) the controller cost. As the single-phase converters are used in low power applications, a low-cost controller solution is preferred.

A new variation of the constant frequency current programmed control is the one-cycle control or the nonlinear carrier control [13]–[15]. It has solved many of the above-mentioned issues such as cost, complexities, sensing points andovercurrent protection. Instead of a current controller a modulator is used in the controller, where the measured input current is compared with a suitable carrier to derive the required

Manuscript received September 13, 2005; revised February 14, 2006. Recommended for publication by Associate Editor J. Espinoza.

The authors are with the Department of Electrical Engineering, Indian Institute of Science, Bangalore 560012, India (e-mail: rajesh@ee.iisc.ernet.in; gnar@ee.iisc.ernet.in).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2006.886621

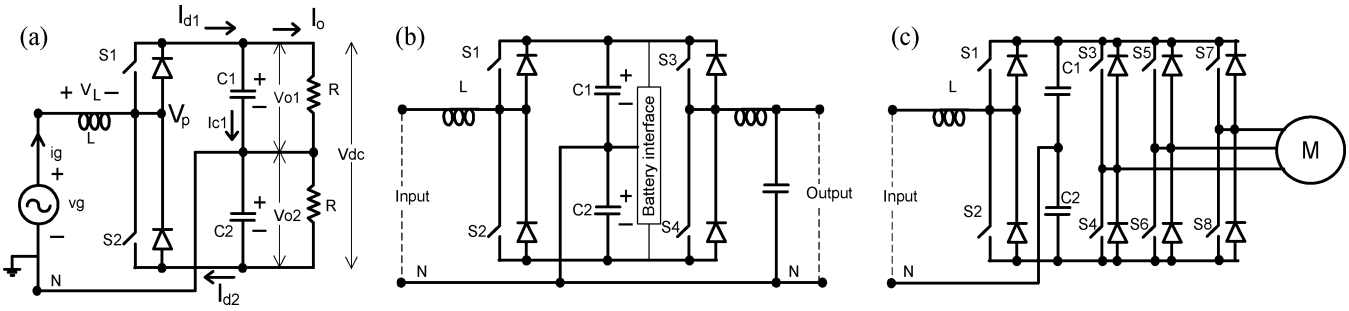

Fig. 1. Single-phase half-bridge rectifier applications; (a) ac–dc, (b) transformerless UPS, and (c) single-phase to three-phase.

gating pulses for the converter switches. The controller does not use input voltage sensing and offers comparable performance over the existing ones [3]–[12]. It can be realized using simple integrated circuits without any expensive multiplier and/or divider circuits. Such a controller is proposed in [13] for the three-phase boost rectifier and in [14], [15] for the single-phase, single-switch boost rectifier.

This paper extends the above-mentioned control concept to single-phase half-bridge rectifier and proposes a simple, low-cost controller solution. The control methods reported in [13]–[15] is applied to converter topologies with a single dc bus voltage $V_{\rm dc}$ to be controlled. However a half-bridge rectifier has a split dc bus as shown in Fig. 1(a). Under normal operating condition there exists an unbalance in the voltages V_{o1} and V_{o2} as discussed in [4], [5], and [16]. An additional voltage-balancing loop is used to mitigate the unbalance [4], [5], and [7]. Considering the above issues, the control scheme is proposed in Section II. The method of unbalance correction is explained.

Effort has been made to provide complete set of design equations. The selection of the passive components (L and C) is discussed in Section III. The averaged small signal model with the proposed control is developed in Section IV. A detailed analysis is presented for designing the voltage controllers. The effect of dc bus voltage ripple on the input current distortion is explained. The controllers proposed in [13]–[15] use a modulator in place of a current controller. However no further analysis has been reported for the modulator. In the present work it is shown that the modulator can be analyzed to be an equivalent current loop. An estimation of current loop bandwidth is also given.

A current programmed controller is reported to have subharmonic instability for duty ratio $D >$0.5 [17], [18]. This must be expected in ac–dc PFC applications as well since the converter duty ratio varies over a wide range in a line cycle. A detailed analysis is provided in Section V to determine the condition of subharmonic instability.

An estimation of the converter switching loss and conduction loss is given in Section VI.

In order to validate the control concept an 800-W prototype is built. The converter is tested for two applications namely 1) single-phase ac–dc rectification and 2) single-phase ac–dc–ac power conversion. Under ac–dc–ac application the possibilities of both linear and nonlinear loads are considered at two different output fundamental frequencies (50 and 60 Hz), while the input side frequency is 50 Hz. The experimental results are discussed in Section VII. Finally, the conclusion is given in Section VIII.

II. Control Scheme

A single-phase half-bridge rectifier is shown in Fig. 1(a). In each switching cycle T_s the converter switches S_1 and S_2 are turned on and turned off by complementary gating pulses. S_2 is turned on for a duration of DT_s and S_1 for $(1-D)T_s$, where D is the duty ratio of the converter. With S_2 on and S_1 off, the voltage applied across the inductor L is $(V_g + V_{o2})$. Again, with S_1 on and S_2 off, the same is $(v_g - V_{o1})$. Assuming a constant and high switching frequency $(f_{\rm sw} = 1/T_s)$ the duty ratio D can be determined by the volt–second balance across the inductor L as shown in [4]

$$v_g = V_{o1} - D(V_{o1} + V_{o2}). \tag{1}$$

A. Control Equation

One control objective is to modulate the duty ratio D such that the converter operates at unity power factor and the input current i_g is proportional to the input voltage v_g as per (2), where R_e is the emulated resistance of the converter [14]. The second objective is to hold the dc bus voltage $V_{\rm dc}$ at the reference level irrespective of the input voltage and load variations. This can be achieved by regulating the effective input side resistance R_e in closed loop control. In [13]–[15], the output of the dc bus voltage controller V_m is used to realize R_e as shown in (3), where R_s is the gain in the current sensing path [14]

$$i_g = v_g/R_e \tag{2}$$

$$V_m = (V_{\rm dc}R_s)/R_e. \tag{3}$$

Since a half-bridge converter has a split dc bus, both the output voltages V_{o1} and V_{o2} must be regulated [4], [5], [7]. These two voltages must also be balanced. Addressing the above-mentioned objectives the present work proposes a PI controller each for controlling V_{o1} and V_{o2} independently as shown in Fig. 2. The outputs of the two controllers V_{m1} and V_{m2} are used to control the emulated resistance R_e of the whole converter. Similar to (3), V_{m1} and V_{m2} are related to R_e and also to the respective output voltages as shown in

$$V_{m1} = (V_{o1}.R_s)/R_e \tag{4}$$

$$V_{m2} = (V_{o2}.R_s)/R_e. \tag{5}$$

Using (1), (2), (4), and (5) the control equation (6) for the proposed controller is obtained. Note that the left hand side of

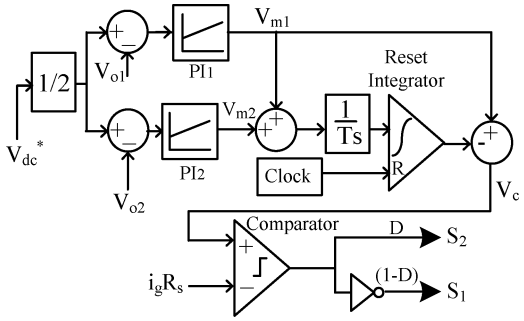

Fig. 2. Proposed control scheme.

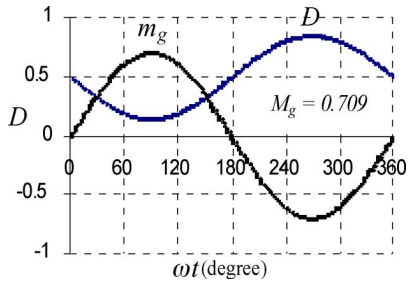

Fig. 3. Variation of duty ratio over a line cycle.

(6) is the output of the input current sensor with gain R_s

$$i_g.R_s = V_{m1} - D(V_{m1} + V_{m2}). \tag{6}$$

Equation (6) can be solved for D as shown in (7) and accordingly the required gating pulses can be generated. At steady state $V_{o1} = V_{o2} = V_o$. The required variation of D over a line cycle is shown in (8) and also in Fig. 3, where $v_g = V_{\rm gm}\sin(\omega t) = m_g V_o$, $M_g = V_{\rm gm}/V_o$ and ω is the supply angular frequency

$$D = \frac{V_{m1} - i_g R_s}{V_{m1} + V_{m2}} = \frac{V_{o1} - i_g R_e}{V_{o1} + V_{o2}} \tag{7}$$

$$\begin{aligned} D &= 0.5(1 - v_g/V_o) = 0.5(1 - m_g) \\ &= 0.5(1 - M_g \sin \omega t). \end{aligned} \tag{8}$$

The analytical solution of (7) however requires a division operation to be performed, which increases the controller cost. In order to avoid the division a carrier-based approach as in [13]–[15] is followed.

B. Carrier

In order to solve (6) for the duty ratio D, in any switching interval T_s consider a carrier $V_c(t)$ as defined in (9). Note that the carrier is obtained by replacing D with t/T_s in the right hand side of (6) [14]. The carrier can be generated by simple integration as shown in (10) and its shape is shown in Fig. 4(a)

$$V_c(t) = V_{m1} - (V_{m1} + V_{m2})t/T_s; \;\; (0 < t < T_s) \tag{9}$$

$$V_c(t) = V_{m1} - \frac{(V_{m1} + V_{m2})}{T_s} \int_0^t 1.dt; \;\; (0 < t < T_s). \tag{10}$$

In the beginning of any interval T_s (i.e., at $t = 0$), $V_c(t)$ is equal to V_{m1}. It is $(-V_{m2})$ at the end of the interval $t = T_s$.

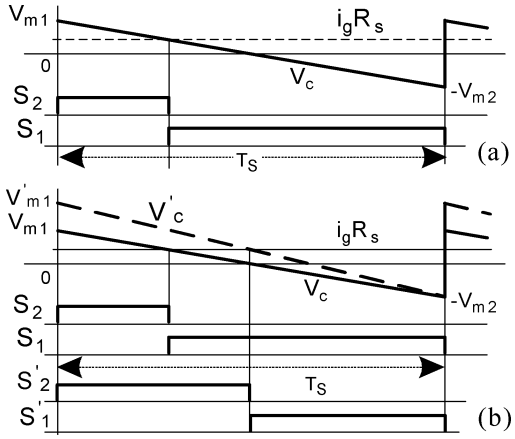

Fig. 4. (a) Gate pulse generation and (b) voltage balancing.

Observe that $V_c(t)$ equals $I_g R_s$ at the instant $t = DT_s$ as in (6). Thus the switching instants can be determined by comparing the input current $i_g R_s$ with $V_c(t)$ in a comparator as shown in Fig. 2.

C. Generation of Gating Pulses

In each switching cycle T_s, the carrier V_c is generated using a simple analog circuit containing a reset-integrator as shown in Fig. 2. The integrator is reset by the rising edge of a constant frequency clock. The measured input current $I_g R_s$ is compared with the carrier V_c in the comparator as shown in Figs. 2 and 4(a). The comparator output directly drives the switch S_2. The complementary pulses drive S_1. It can be seen that unlike [13]–[15] the use of S–R flip-flop based structure is avoided. Such structures are sensitive to the noise in the measured input current $(i_g R_s)$, which causes unwanted flip-flop resets [18].

D. Balancing the Output Voltages V_{o1} and V_{o2}

The mechanism of output voltage balancing is explained with the help of Fig. 4(b). Consider V_c is the carrier (in solid line) and S_1 and S_2 are the corresponding gating pulses under balanced condition (i.e., $V_{o1} = V_{o2}$). The positive and the negative peaks of V_c are V_{m1} and $-V_{m2}$, respectively, where $V_{m1} = V_{m2}$.

A particular case of unbalance, where $V_{o1} < V_{\rm dc}^*/2$ (reference voltage) and $V_{o2} = V_{\rm dc}^*/2$, increases the output of the controller for V_{o1} and also the positive peak of the carrier to a new value V'_{m1} $(> V_{m2})$ as shown. The modified carrier V'_c is shown in dashed line. The corresponding gating pulses S'_1 and S'_2 show that compared to the balanced case the bottom device remains on for a longer duration and the top device for a shorter duration. This results in transfer of excess energy from C_2 to C_1 to balance both V_{o1} and V_{o2}. The control action during other cases of voltage unbalance can also be explained qualitatively in a similar fashion. A detailed mathematical analysis is presented in Section IV.

A variable-frequency, hysteresis current control technique with a single PI controller controlling the entire dc bus voltage $V_{\rm dc}$ and a voltage-balancing controller for balancing V_{o1} and V_{o2} is proposed in [4] and [5]. Using two such controllers an alternative fixed-frequency, one-cycle control scheme is

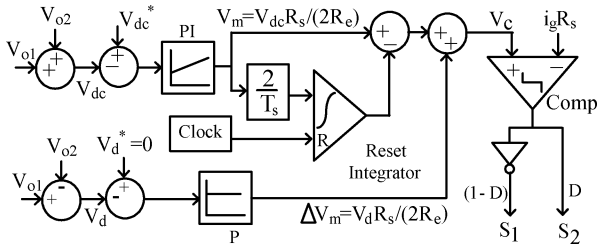

Fig. 5. Alternative control scheme.

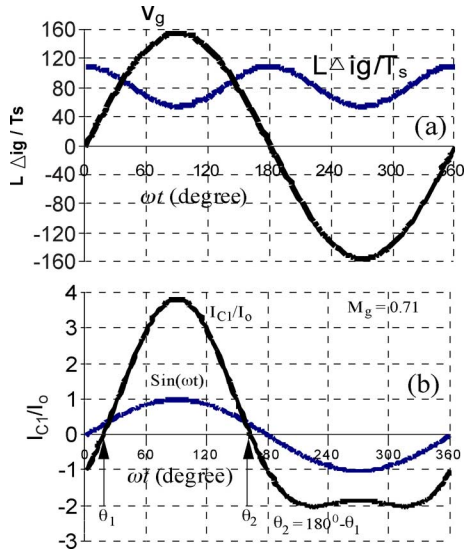

Fig. 6. (a) Variation of $(L\Delta i_g/T_s)$ and (b) variation of I_{C1}/I_o over a fundamental cycle.

proposed in Fig. 5. All the necessary equations are shown in Fig. 5. It can be shown that any one of the control schemes mentioned in Figs. 2 and 5 may be used to generate the required gating pulses. However in the present work the scheme shown in Fig. 2 is considered for detailed investigation. The control scheme developed in this section can be extended to three-phase, four-wire PWM rectifier [10].

III. Selection of Passive Components

Selection of the input inductor L and the output capacitors C_1 and C_2 are discussed in this section.

A. Input Side Inductor L

The peak-to-peak ripple in the inductor current i_g in a switching interval T_s is given in (11), where D is defined in (8). The variation of $(L\Delta i_g/T_s)$ over a fundamental cycle is shown in Fig. 6(a). It can be seen that Δi_g has a maximum value of $\Delta i_{g\max}$ at v_g equals zero, as shown in

$$\Delta i_g = \left(\frac{v_g + V_o}{L}\right) DT_s = \frac{V_o T_s}{2L}\left[1 - \{M_g \sin(\omega t)\}^2\right] \quad (11)$$

$$\Delta i_{g\max} = V_o T_s/(2L). \quad (12)$$

The inductor value L is determined using the highest permissible $\Delta i_{g\max}$ as shown in (13), where $I_{\rm gm}$ is the peak input current and P_o is the output power. Using the parameters given in Table I and for $(\Delta i_{g\max}/I_{\rm gm})$ =0.1, the required inductance is found to be 10.7 mH

$$L = \frac{V_o T_s}{2I_{\rm gm}(\Delta i_{g\max}/I_{\rm gm})} = \frac{V_o^2 M_g}{4P_o f_{\rm sw}(\Delta i_{g\max}/I_{\rm gm})}. \quad (13)$$

TABLE I
Parameters and Components of the System

P_o	800W		C_3	0.01μF
V_{gm}	156V		C_4	1μF
V_o	220V		C_5	0.01μF
f_{sw}	10kHz		Op-amps	TL084
ω	2π*50 rad/s		Comparator	TL084
L	10mH		Inverter	CD4069
R_L	0.2Ω		Clock	555
C_1, C_2	2200μF		K_V	0.03
S_1- S_4 (IGBT)	CM50DY-12H 50A, 600V		R_s	0.5Ω
R_1	1MΩ		V_{ce}	2.1V
R_2	22KΩ		V_{dd}	2.7V
R_3 - R_7	10KΩ		t_{on} + t_{off}	0.75μs
R_{s1}	0.01Ω			

B. DC Bus Capacitors C_1 and C_2

The capacitor current consists of switching frequency components and low frequency components. For selection of the output capacitance (C_1 and C_2), only the low frequency components are considered. The switching cycle average capacitor current I_{c1} Fig. 1(a), which includes the sum of all low frequency components is shown in (14). Assuming unity power factor operation, the variation of (I_{c1}/I_o) over a fundamental cycle is shown in Fig. 6(b). The zero crossing instants, namely θ_1 and θ_2, are given in (15). The peak-to-peak voltage ripple in V_{o1} is shown in (16). With this, an expression for C_1 can be obtained as shown in (17), where f is the fundamental frequency in Hz

$$I_{c1} = (1-D)i_g - I_o = I_o\left[(2/M_g)\sin(\omega t) - \cos(2\omega t)\right] \quad (14)$$

$$\theta_1 = \sin^{-1}\left[\frac{1}{2M_g}\left(\sqrt{(1+2M_g^2)} - 1\right)\right]$$

$$\theta_2 = (180^\circ - \theta_1) \quad (15)$$

$$\Delta V_{o1} = \frac{1}{\omega C_1}\int_{\theta_1}^{\theta_2} I_{c1}\, d\omega t \quad (16)$$

$$C_1 = \frac{P_o}{4\pi V_o^2 f(\Delta V_o/V_o)}\left[\frac{4}{M_g}\cos(\theta_1) + \sin(2\theta_1)\right]. \quad (17)$$

Considering an input voltage regulation of ±15% around the nominal value (110 V rms) and using the parameters of Table I, the effective range of operation is found to be $0.6 < M_g < 0.82$.

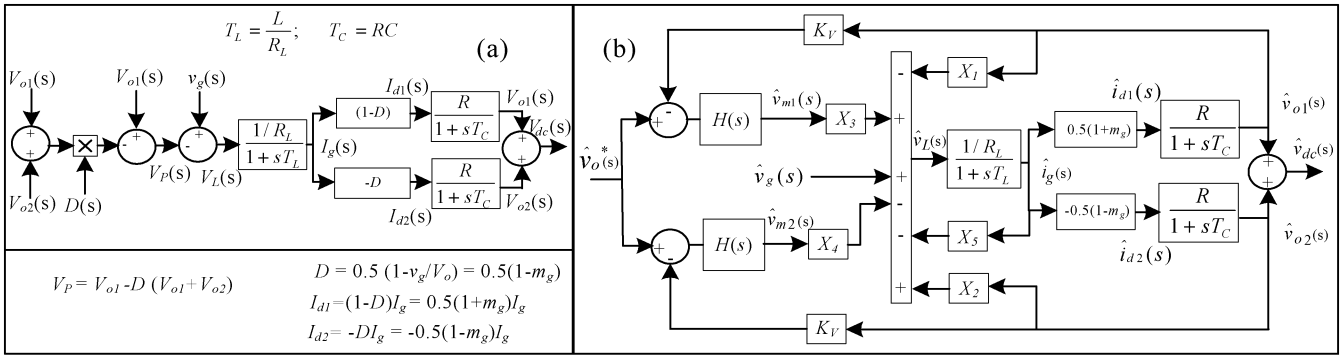

Fig. 7. (a) Average model of the converter at steady state and (b) small signal model of the converter and controller.

For this range, (17) can be approximated as in (18). For $(\Delta V_o/V_o) = 0.07$, the required capacitance is found to be 2270 μF

$$C_1 = C_2 = \frac{0.876P_o(1 - 0.636M_g)}{V_o^2 f(\Delta V_o/V_o)}. \tag{18}$$

IV. Small Signal Analysis

Assuming a high switching frequency compared to the fundamental frequency, the switching cycle average model of the half-bridge rectifier Fig. 1(a) is derived in this section. Using the average model the small signal model is developed. The converter is analyzed using the small signal model.

A. Small Signal Model of the Converter

The input (ac) side and the output (dc) side of the converter [Fig. 1(a)] can be represented by (19a)–(19c), where R_L is the inductor resistance, R is the equivalent load resistance across each half of the dc bus, $C = C_1 = C_2$ and D is defined in (8). It should be noted that all the quantities used in this section represent the switching-cycle averaged quantities [18]. The combinations of the switches S_1 and S_2 and the dc bus voltages V_{o1} and V_{o2} can be considered to be an inverter, with V_P its pole voltage, defined in (19d). The voltage V_L across the line-side inductor L [Fig. 1(a)] can be controlled through the pole voltage V_P as shown in (19e). Using (19a)–(19e), the steady state switching-cycle, averaged model of the converter (in frequency domain) is obtained as shown in Fig. 7(a)

$$V_L = L\frac{dI_g}{dt} + R_L I_g \tag{19a}$$

$$I_{d1} = C\frac{dV_{o1}}{dt} + \frac{V_{o1}}{R} = (1 - D)I_g \tag{19b}$$

$$I_{d2} = C\frac{dV_{o2}}{dt} + \frac{V_{o2}}{R} = -DI_g \tag{19c}$$

$$V_P = V_{o1} - D(V_{o1} + V_{o2}) \tag{19d}$$

$$V_L = v_g - V_P. \tag{19e}$$

The above model represents the open loop system of the converter in the steady state. In order to study the dynamic behavior of the system, it is required to close the feedback loop through the controller, shown in Fig. 2. In Fig. 7(a), the input D is obtained by solving the control equation (7) in the modulator. Using (7), (19e) is modified in (20). It can be seen that (20) represents a nonlinear system. This can be linearized around a steady state operating point (OP) (v_g, m_g, $V_{o1} = V_{o2} = V_o$, I_g and $V_{m1} = V_{m2} = V_m$) as shown in (21a), whose parameters are given in (21b)

$$\begin{aligned} V_L &= v_g - V_P \\ &= v_g - V_{o1} + \frac{(V_{m1} - i_g R_s)(V_{o1} + V_{o2})}{(V_{m1} + V_{m2})} \end{aligned} \tag{20}$$

$$\begin{aligned} \hat{v}_L = &- X_1\hat{v}_{o1} + X_2\hat{v}_{o2} + X_3\hat{v}_{m1} \\ &- X_4\hat{v}_{m2} - X_5\hat{i}_g + \hat{v}_g \end{aligned} \tag{21a}$$

$$X_1 = \left.\frac{-\partial V_L}{\partial V_{o1}}\right|_{(OP)} = \frac{(1 + m_g)}{2}$$

$$X_2 = \left.\frac{\partial V_L}{\partial V_{o2}}\right|_{(OP)} = \frac{(1 - m_g)}{2}$$

$$X_3 = \left.\frac{\partial V_L}{\partial V_{m1}}\right|_{(OP)} = (1 + m_g)\frac{R_e}{2R_s}$$

$$X_4 = \left.\frac{-\partial V_L}{\partial V_{m2}}\right|_{(OP)} = (1 - m_g)\frac{R_e}{2R_s}$$

$$X_5 = \left.\frac{-\partial V_L}{\partial i_g}\right|_{(OP)} = R_e$$

$$V_{m1} = V_{m2} = V_m = \frac{V_o R_s}{R_e}. \tag{21b}$$

Similarly the small signal transfer functions between I_{d1}, I_{d2} and I_g around a steady state operating point m_g and D can be obtained from (19b) and (19c) as shown in (22a) and (22b), respectively

$$\left.\frac{\hat{i}_{d1}}{\hat{i}_g}\right|_{\hat{d}=0} = (1 - D) = 0.5(1 + m_g) \tag{22a}$$

$$\left.\frac{\hat{i}_{d2}}{\hat{i}_g}\right|_{\hat{d}=0} = -D = -0.5(1 - m_g). \tag{22b}$$

Using the linearized equations (20)–(22) and Figs. 2 and 7(a), the linearized model is obtained as shown in Fig. 7(b), where $H(s)$ is the voltage controller to be designed and K_V is the gain of dc voltage sensors.

B. Equivalent Current Loop

It is mentioned earlier that instead of a current controller, the proposed controller has a modulator that generates the required

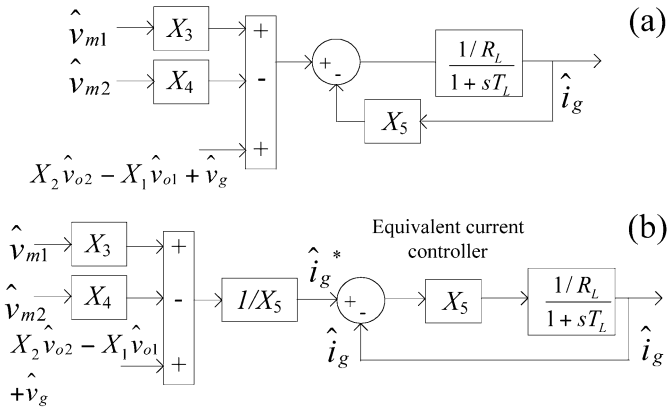

Fig. 8. Equivalent current loop.

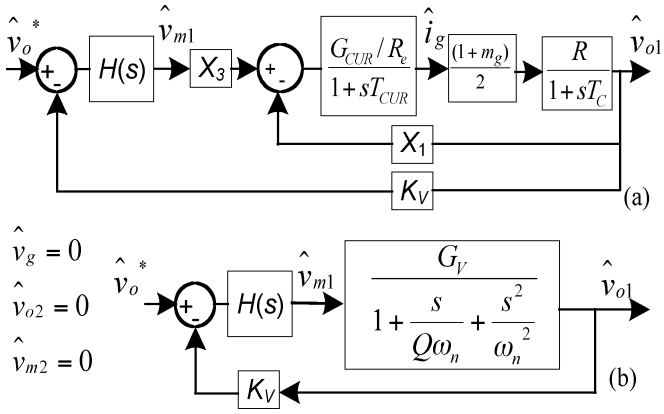

Fig. 9. Voltage loop.

gating pulses. In this section, it is shown that the modulator can be viewed as an equivalent current loop. This is required to analyze the voltage loop. The equivalent current loop, derived from Fig. 7 is shown in Fig. 8(a), which is modified in Fig. 8(b). I_g^* is the reference current for the equivalent current loop. The gain X_5 is the emulated resistance R_e of the converter as given in (22), which may be considered to be an equivalent proportional controller. The closed loop transfer function of the equivalent current loop is shown in (23). The bandwidth of the equivalent current loop $F_{\rm BW}$ (Hz) can be obtained as shown in (24). The full load bandwidth of the current loop is calculated to be 240 Hz (parameters are given in Table I). As load decreases, R_e increases and the bandwidth increases

$$\frac{\hat{i_g}(s)}{\hat{i_g}^*(s)} = \frac{G_{\rm CUR}}{(1+sT_{\rm CUR})}$$
$$G_{\rm CUR} = \frac{R_e}{R_L+R_e} \approx 1$$
$$T_{\rm CUR} = \frac{L}{R_L+R_e} \approx \frac{L}{R_e}; \quad R_e \gg R_L \tag{23}$$
$$F_{\rm BW} = \frac{1}{2\pi T_{\rm CUR}}. \tag{24}$$

C. Voltage Loop

Since the two voltage loops are identical (Fig. 7), it is sufficient to consider one of them to design the voltage controllers $H(s)$. The voltage loop corresponding to V_{o1} and V_{m1} can be obtained from Fig. 7 as shown in Fig. 9(a), which is simplified in Fig. 9(b). The loop gain of the voltage loop with $(H(s) = 1)$ is given in (25), whose parameters are given in (26). The loop gain depends on m_g and the load resistor R

$$G_L(s) = \frac{G_V K_V}{1+\frac{s}{Q\omega_n}+\frac{s^2}{\omega_n^2}} \tag{25}$$
$$G_V = \frac{\frac{R(1+m_g)^2}{4R_s}}{1+\left(\frac{1+m_g}{M_g}\right)^2}; \quad \omega_n = \sqrt{\frac{M_g^2+(1+m_g)^2}{4LC}}$$
$$Q = \frac{4\omega_n}{\frac{RM_g^2}{L}+\frac{4}{RC}}. \tag{26}$$

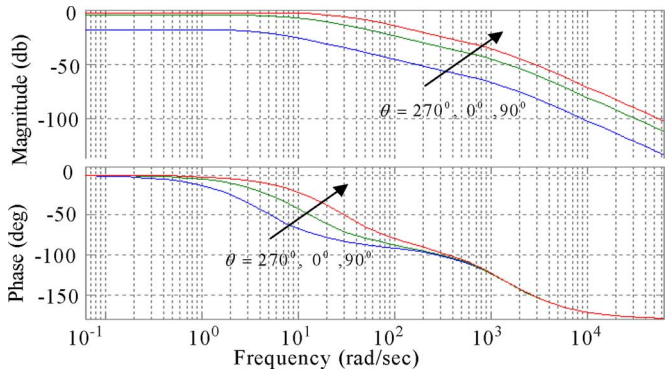

Fig. 10. Bode plot of loop gain $G_L(s)$.

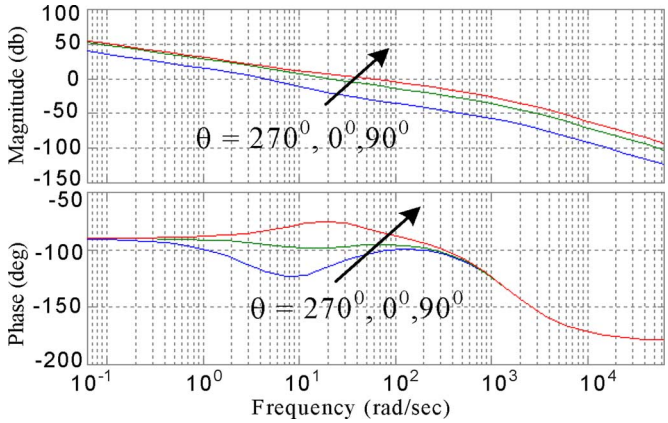

Fig. 11. Bode plot of voltage loop gain $G_L(s)H(s)$.

The Bode plot of (25) is shown for different values of $\theta(\theta = \omega t)$ in Fig. 10 (parameters are given in Table I). It can be shown that $G_L(s)$ has a high frequency pole around 1500 rad/s and a low frequency pole around 15 rad/s. A simple proportional-integral (PI) type of voltage controller, shown in (27) is used to control the system. The corner frequency $(1/T_{\rm PI})$ is set at 15 rad/s and the proportional gain $K_{\rm PI}$ is set at 3. Fig. 11 shows the bode plot of the loop gain $G_L(s)H(s)$ for different values of θ, where $H(s)$ is defined in (27). The average gain crossover frequency ω_c (corresponding to $\theta = 900^\circ$ and $\theta = 270^\circ$) and the settling time $(4/\omega_c)$ are found to be 25 rad/s and 160 ms, respectively.

It should be noted that the parameter $K_{\rm PI}$ has an effect on the steady state input current distortion and the input current displacement caused by the dc bus voltage ripple. This is explained in the next section, where it is shown that selection of $K_{\rm PI}=3$ is a good trade-off between the distortion and displacement in i_g on one hand and fastness of response on the other

$$H(s)=\frac{K_{\rm PI}(1+sT_{\rm PI})}{sT_{PI}}. \tag{27}$$

D. Effect of dc Bus Voltage Ripple on Steady State Input Current

In previous sections it was assumed that at steady state V_{o1}, V_{o2}, V_{m1}, V_{m2} are the dc quantities, where $V_{o1}=V_{o2}=V_o$ and $V_{m1}=V_{m2}$. However, in actual practice they contain low frequency ripple superimposed on the dc voltages. Using (8) and the input–output power balance the switching cycle average dc bus currents I_{d1} and I_{d2} [Fig. 1(a)] are obtained in (28) and (29), respectively, where $i_g=I_{\rm gm}\sin(\omega t)$

$$\begin{aligned} I_{d1}&=(1-D)i_g\\ &=0.5I_{\rm gm}\left[\sin(\omega t)-0.5M_g\cos(2\omega t)\right]+I_o \qquad (28)\\ I_{d2}&=(-D)i_g\\ &=-0.5I_{\rm gm}\left[\sin(\omega t)+0.5M_g\cos(2\omega t)\right]+I_o. \qquad (29)\end{aligned}$$

The steady state ripple voltages in V_{o1} and V_{o2} are shown in (30) and (31), respectively

$$\begin{aligned}\tilde{v}_{o1}&=\frac{1}{\omega C}\int(I_{d1}-I_o)d\omega t\\ &=\frac{I_{\rm gm}}{2\omega C}[-\cos\omega t-0.25M_g\sin 2\omega t] \qquad (30)\\ \tilde{v}_{o2}&=\frac{1}{\omega C}\int(I_{d2}-I_o)d\omega t\\ &=\frac{I_{\rm gm}}{2\omega C}[\cos\omega t-0.25M_g\sin 2\omega t]. \qquad (31)\end{aligned}$$

The shapes of $\tilde{v}_{o1}$ and $\tilde{v}_{o2}$ are shown in [4]. At steady state, the dc components of V_{o1} and V_{o2} are equal to the reference voltage $V^*_{\rm dc}/2$ (Fig. 2), while the ripple components get processed by the voltage controllers as shown in (32) and (33). With a corner frequency $1/T_{\rm PI}$ of 15 rad/s (see Section IV-C) the integral terms in (32) and (33) are negligible compared to the proportional terms and hence they may be neglected

$$\begin{aligned}\tilde{v}_{m1}&=-K_{\rm PI}K_V\tilde{v}_{o1}-\frac{K_{\rm PI}K_V}{T_{\rm PI}}\int\tilde{v}_{o1}dt\\ &\approx -K_{\rm PI}K_V\tilde{v}_{o1} \qquad (32)\\ \tilde{v}_{m2}&=-K_{\rm PI}K_V\tilde{v}_{o2}-\frac{K_{\rm PI}K_V}{T_{\rm PI}}\int\tilde{v}_{o2}dt\\ &\approx -K_{\rm PI}K_V\tilde{v}_{o2}. \qquad (33)\end{aligned}$$

Now to study the effect of $\tilde{v}_{m1}$ and $\tilde{v}_{m2}$ on the input current i_g, it is assumed that the current loop response is very fast and the input current i_g exactly follows the reference current i^*_g. The small signal linearized model shown in Fig. 8(b) is used to determine the steady state reference current i^*_g as shown in (34a). It is found that i^*_g has a dc component and an ac component as shown in (34b) and (34c), respectively. It can be seen

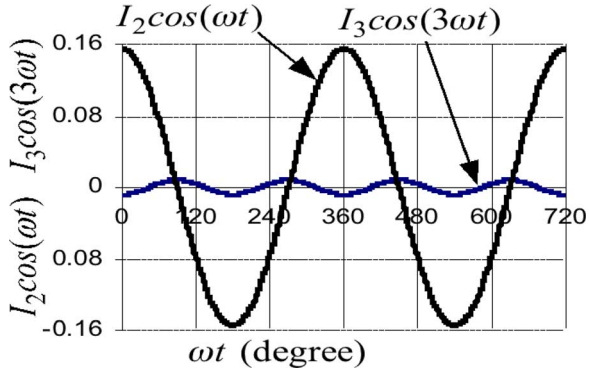

Fig. 12. Variations of displacement and distortion components over two fundamental cycles.

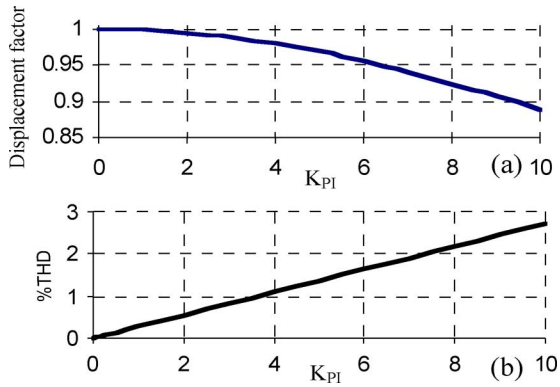

Fig. 13. Variation of (a) displacement and (b) THD in the input current with respect to $K_{\rm PI}$.

that if there is no ripple in V_{o1} and V_{o2} then at steady state $i^*_g=i_g=i_g(ac)=v_g/R_e$ and $i_g(dc)=0$. However, due to presence of voltage ripple, the current reference is as shown in (35), whose parameters are defined in (36) and in Table I

$$\begin{aligned} i^*_g&=i_g=i_{g(\rm ac)}+i_{g(\rm dc)} \qquad (34a)\\ i_{g(\rm ac)}&=(V_{m1}+V_{m2}).m_g/(2R_s) \qquad (34b)\\ i_{g(\rm dc)}&=(V_{m1}-V_{m2})/(2R_s) \qquad (34c)\\ i^*_g&=I_{\rm gm}\left[\sin(\omega t)+I_2\cos(\omega t)+I_3\cos(3\omega t)\right] \qquad (35)\\ I_2&=\frac{\left(1+0.375M_g^2\right)K_{\rm PI}K_V}{2\omega R_sC}=0.0516K_{\rm PI}\\ I_3&=\frac{-K_{\rm PI}K_VM_g^2}{16\omega R_sC}=-0.0027K_{\rm PI}. \qquad (36)\end{aligned}$$

The first term in the RHS of (35) corresponds to the desired sinusoidal current $v_g/R_e=I_{\rm gm}\sin(\omega t)$. For $K_{\rm PI}=3$, the variation of the second and the last terms of RHS of (35) as per unit of $I_{\rm gm}$ are shown in Fig. 12. It can be seen that the second term introduces a displacement in i_g with respect to v_g, while the last term causes the distortion (third harmonic) in i_g. For a given K_V, the displacement factor $(\cos(\tan^{-1}(I_2))$ and the distortion factor (I_3) in i_g depend on $K_{\rm PI}$ as shown in Fig. 13. For $K_{\rm PI}=3$, the THD and the displacement factor are acceptable at 0.82% and 0.99, respectively. The transient performance is also fast enough with a settling time of 160 ms as mentioned in Section IV-C.

E. Voltage Balancing

Referring to (28), (29), (34), and Fig. 1(a) the dc bus current I_{d1} can be expressed in terms of I_{d2} as shown in (37). Equation (37) contains both dc as well as ac components. The ac components in I_{d1} and I_{d2} cause voltage ripple in C_1 and C_2, while the dc components $(I_{d1}-I_o)$ and $(I_{d2}-I_o)$ are responsible for the change of voltage level. The dc components of (37) may be obtained by averaging (37) over the supply fundamental cycle as shown in (38), where I_{D1} and I_{D2} are the respective dc components in I_{d1} and I_{d2}

$$I_{d1} = I_{d2} + i_g = I_{d2} + i_{g(\mathrm{ac})} + i_{g(\mathrm{dc})} \quad (37)$$

$$I_{D1} = I_{D2} + i_{g(\mathrm{dc})} = I_{D2} + (V_{m1} - V_{m2})/(2R_s). \quad (38)$$

Under balance condition $V_{o1} = V_{o2}$ and $V_{m1} = V_{m2}$. It can be seen from (38) that $I_{D1} = I_{D2}$ and each of them equals to load current I_o [see (28) and (29)]. Now considering a case when $V_{o1} < V^*_{\mathrm{dc}}/2$ and $V_{o2} = V^*_{\mathrm{dc}}/2$ it can be seen that $V_{m1} > V_{m2}$, where $V^*_{\mathrm{dc}}/2$ is the reference voltage for each half of the dc bus. This causes $I_{D1} > I_{D2}$, while $I_{D2} = I_o$. The additional dc current $i_{g(\mathrm{dc})}$ actually flows through C_1 to charge it up to reduce the voltage unbalance. Similarly it can be shown that $i_{g(\mathrm{dc})}$ flows through C_2 when $V_{o2} < V^*_{\mathrm{dc}}/2$.

Hence, the voltage controllers add a suitable dc component of appropriate polarity to the current reference for the equivalent inner current loop to eliminate the voltage unbalance. The small signal model developed in this section enables us to see the similarity between the proposed controller and the controllers reported in [4], [5] in this regard.

V. Subharmonic Stability

The inner current loop of a fixed-frequency, uncompensated, current programmed controller is reported to have an unconditional subharmonic instability for operation above 50% switch duty ratio [17], [18]. It is found that for the duty ratio D >0.5 the inductor current has a damped sinusoidal response at one-half of the switching frequency, which introduces unwanted ringing on the expected inductor current during the input voltage and load transients. Further the outer voltage loop is also found to have oscillation around one-half of the switching frequency. This is known as subharmonic Oscillation [17]. This problem is solved by adding a suitable linear compensating ramp to the reference current I_{ref} to make the controller stable for D >0.5 as shown in Fig. 14(a) and also in [17] and [18].

It has been shown in Section IV that the proposed control can be viewed as current programmed control with an equivalent inner current loop and an outer voltage loop. Furthermore, in the proposed control scheme D >0.5 during the entire negative half of the fundamental cycle as seen from (8) and Fig. 3. Therefore, oscillations at frequencies less than the switching frequency may be expected.

Fig. 14(b) shows the inductor current I_g over an arbitrary switching interval T_s. The inductor current increases with a slope m_1 during the interval DT_s and then for rest of the interval it falls with a slope m_2. As mentioned in Section II, the intersection of I_g with the carrier V_c determines the turn off instant of the converter switch S_2. Therefore the carrier V_c [Fig. 14(b)] can be considered similar to be a current reference with compensating

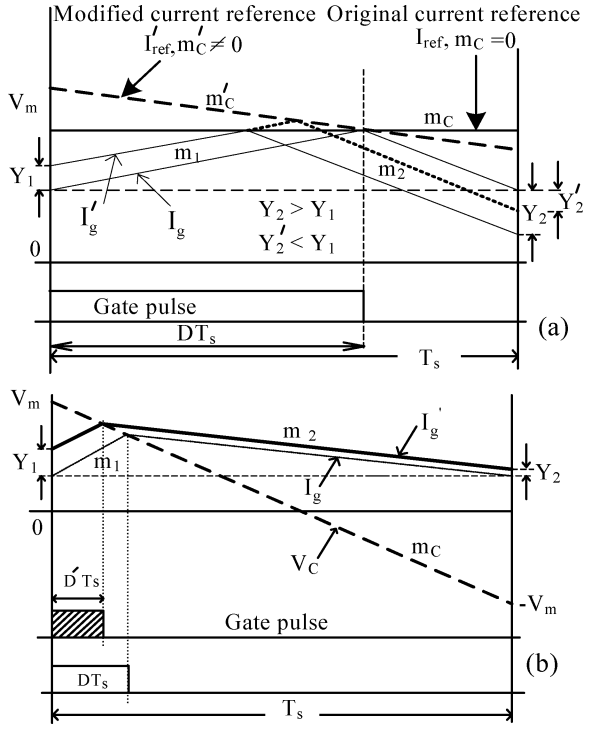

Fig. 14. Analysis of subharmonic instability: (a) conventional current programmed control and (b) proposed control.

ramp of slope m_c. The absolute values of m_1, m_2 and m_c are defined in (39). It can be seen that the slopes m_1 and m_2 vary over the fundamental cycle. Therefore the actual volt–second balance across the inductor L is maintained over a fundamental cycle. However, because of high switching frequency f_{sw} (compared to the fundamental frequency) the volt–second balance may be assumed to be maintained across L in each switching cycle T_s as discussed in Section II. This assumption states that the average voltage across L and hence the average slope of I_g over a switching cycle T_s is zero. Thus, at the end of T_s, the current I_g is shown to be falling to the same level from where it started in the beginning of the interval [Fig. 14(b)].

In Fig. 14(b), I_g is the steady state inductor current over a switching interval T_s. Let us consider I'_g is the inductor current, when I_g is perturbed by an amount $Y_1(Y_1 \approx 0)$ in the beginning of the interval T_s. Now Y_2 is the perturbation at the end of T_s. The expression relating Y_1 and Y_2 is shown in (40) [18], where m_g and K are defined in (41). Note that (K/R_s) is the system conduction parameter [18]

$$m_1 = \frac{V_o + v_g}{L};$$

$$m_2 = \frac{V_o - v_g}{L}; \quad m_c = \frac{2V_m}{T_s} = \frac{2V_o R_s}{R_e T_s} \quad (39)$$

$$\frac{Y_2}{Y_1} = \frac{m_2 - m_c}{m_1 + m_c} = \frac{1 - K - m_g}{1 + K + m_g} \quad (40)$$

$$m_g = \frac{v_g}{V_o} = M_g \sin(\omega t); \quad K = \frac{2LR_s}{R_e T_s}. \quad (41)$$

In case of a dc-dc converter [Fig. 14(a)], the sufficient condition for the subharmonic stability is shown to be $Y_2 < Y_1$ [17], [18]. It is explained that with $Y_2 < Y_1$ the perturbation Y_2, after

propagating through a finite number of successive switching cycles decays to zero. Unlike dc-dc converter the slopes m_1 and m_2 of the proposed system are however not constant over the fundamental cycle. This causes the instantaneous inductor current profile, over the successive switching cycles to be nonrepetitive and the switching cycle average inductor current profile over the fundamental cycle to be sinusoidal. Despite these, the proposed controller can be said to be stable if the condition $Y_2 < Y_1$ is maintained in each switching cycle T_s. The required subharmonic stability condition, obtained from (40) and $(Y_2 < Y_1)$ is shown in

$$K > M_g \tag{42}$$

In dc–dc converter the constant slope m_c' [Fig. 14(a)] of the compensating ramp can be adjusted to any desired value to ensure the controller stability for the entire range of duty ratio D. However, in the present case it can be seen from (39) that m_c is load dependent and cannot be adjusted for the purpose of stability. Therefore, the stability condition, shown in (42) depends on load. Using the input output power balance it can be shown that the proposed controller is stable in each switching cycle for output power

$$P_o > \frac{V_{\rm gm}^3}{4V_o L R_{\rm s} f_{\rm sw}}. \tag{43}$$

Using the parameters given in Table I it can be calculated that for the given half-bridge converter, the subharmonic stability is always maintained for an output power greater than 43 W.

VI. Switching Losses and Conduction Losses

In this section an estimation of switching and conduction losses associated with the devices used in the half-bridge rectifier is presented. A sinusoidal input current at unity power factor is considered.

A. Conduction Losses

As discussed in Section II, S_2 conducts for duration DT_s while D_1 conducts for $(1-D)T_s$ in a switching cycle T_s during the positive half cycle of i_g. The average voltage drop over a switching interval T_s is shown in (44), where $V_{\rm ce}$ and $V_{\rm dd}$ are the on state voltage drops across the switch and diode, respectively

$$V_{\rm AV} = DV_{\rm ce} + (1-D)V_{\rm dd} = V_{\rm dd} + (V_{\rm ce} - V_{\rm dd})D. \tag{44}$$

Since the operation is symmetric in the two half cycles, the average loss is as shown in (45). The conduction loss, normalized w.r.t the input power $P_{\rm IN}$ is as shown in (46), where $P_{\rm IN} = (V_{\rm gm}I_{\rm gm}/2)$. The full load conduction loss is found to be 1.9% of the input power (parameters are shown in Table I)

$$P_{\rm cond} = \frac{1}{\pi}\int_0^{\pi} V_{\rm AV} I_{\rm gm}\sin(\omega t)d\omega t \tag{45}$$

$$\frac{P_{\rm cond}}{P_{\rm IN}} = \frac{2(V_{\rm dd}+V_{\rm ce})}{\pi V_{\rm gm}} + \frac{(V_{\rm dd}-V_{\rm ce})}{2V_o} \approx \frac{2(V_{\rm dd}+V_{\rm ce})}{\pi V_{\rm gm}}. \tag{46}$$

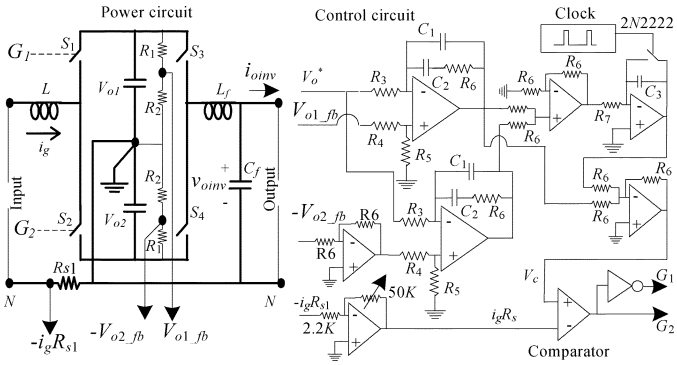

Fig. 15. Experimental setup.

B. Switching Losses

The switches S_1 and S_2 [Fig. 1(a)] are subjected to switching losses during the negative and positive half cycles of the input current i_g, respectively. The energy associated with one switching cycle, which includes one turn on and one turn off is given in (47), where $t_{\rm on}$ and $t_{\rm off}$ are the turn on and turn off times of the devices. The expression for the average switching loss is shown in (48). Equations (47) and (48) yield the expression for the switching loss expressed as per unit of the input power $P_{\rm IN}$ as shown in (49). The full load switching loss is found to be 1.3% of the input power (parameters are shown in Table I)

$$E = 0.5.(2V_o).i_g.(t_{\rm on} + t_{\rm off}) \tag{47}$$

$$P_{\rm switch} = \frac{1}{\pi}\int_0^{\pi} E.f_{\rm sw}d\omega t \tag{48}$$

$$\frac{P_{\rm switch}}{P_{\rm IN}} = \frac{4V_o f_{\rm sw}(t_{\rm on}+t_{\rm off})}{\pi V_{\rm gm}}. \tag{49}$$

VII. Simulation and Experimental Results

The proposed control concept (Fig. 2) has been verified through simulation using MATLAB/SIMULINK and also experimentally on an 800-W laboratory prototype. The experimental set up is shown in Fig. 15. The arrangement for sensing the output voltages and the input current are shown. All measurements are made with respect to the mid-point of the dc bus. Hence, no electrical isolation is required. The system parameters are shown in Table I. The gating pulses generated by the controller are shown in Fig. 16. The supply frequency is 50 Hz. Experimental results for ac–dc application and ac–dc–ac applications are presented here.

A. AC–DC Rectification

The inverter switches S_3 and S_4 (Fig. 15) are kept off and a load resistor is connected across the dc bus. The experimental results corresponding to 775-W output power are shown in Fig. 17. The variations of experimental converter efficiency and the input power factor with output power are shown in Fig. 18(a). The full load efficiency is around 96%. This agrees with the estimated converter losses of 3.2% (conduction and switching) as calculated in Section VI. The measured input

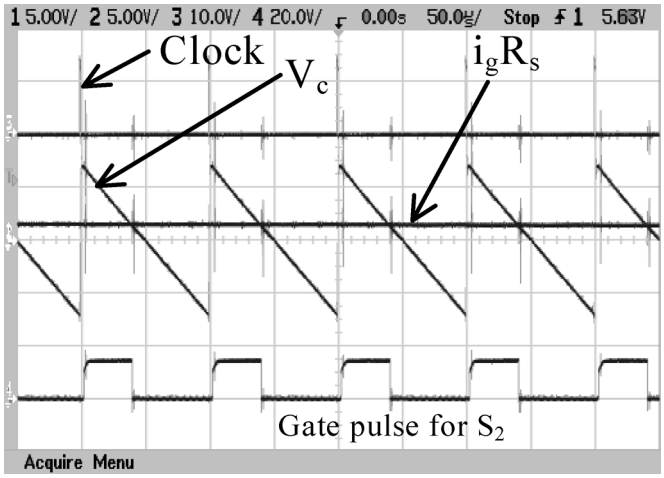

Fig. 16. Experimental gate pulse generation.

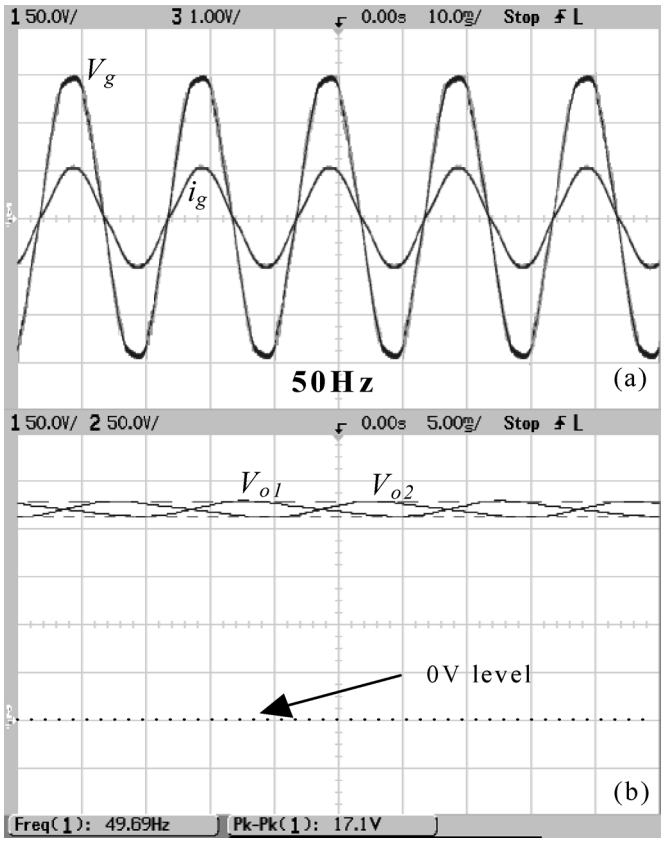

Fig. 17. AC–DC; (a) input voltage V_g (50 V/div) and input current i_g (10 A/div). (b) output voltages V_{o1} and V_{o2} (50 V/div).

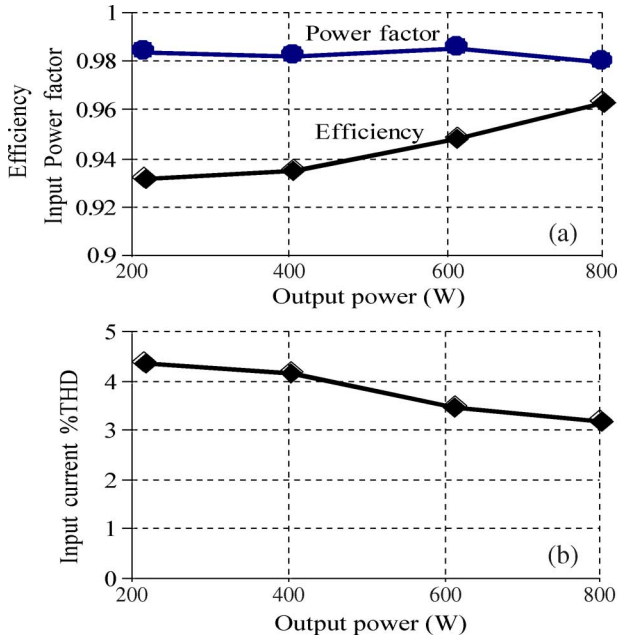

Fig. 18. AC–DC application: (a) variations of efficiency and input power factor and (b) variations of input current THD.

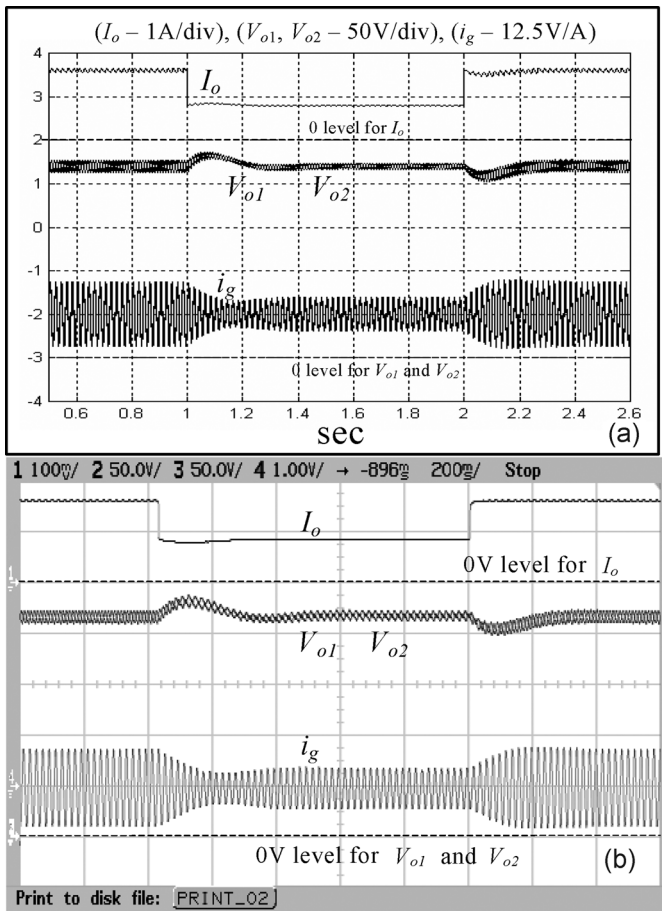

Fig. 19. Transient performance during change in load: (a) simulation results and (b) experimental results [scale shown in (a)].

current total harmonic distortion (THD) factor at different loads is shown in Fig. 18(b). The THD increases as the load reduces. Fig. 19 shows the dynamic response of the system (both simulation and experimental), when there is step change in load from 700 W to 400 W and vice-versa. The settling time is around 200 ms. This agrees reasonably with the estimated settling time of 160 ms (see Section IV-C).

Figs. 17–19 show the experimental results for the ac–dc application with linear load. Additional experimental results with ac–dc–ac application [Figs. 1(b) and 15] are provided in the next section.

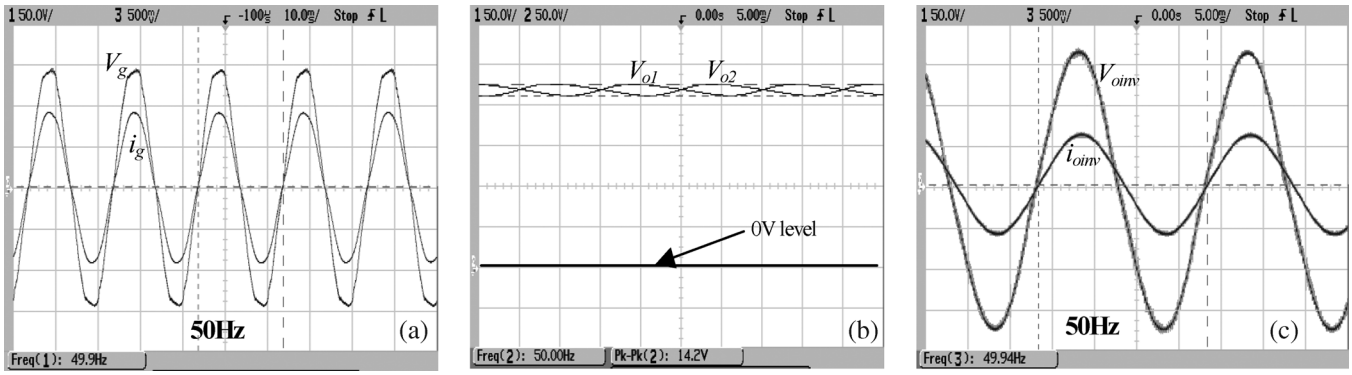

Fig. 20. AC–dc–ac application (50-Hz linear load): (a) input voltage V_g (50 V/div) and input current i_g (5 A/div), (b) output voltages V_{o1} and V_{o2} (50 V/div), and (c) inverter output voltage V_{oinv} (50 V/div) and output current i_{oinv} (5 A/div).

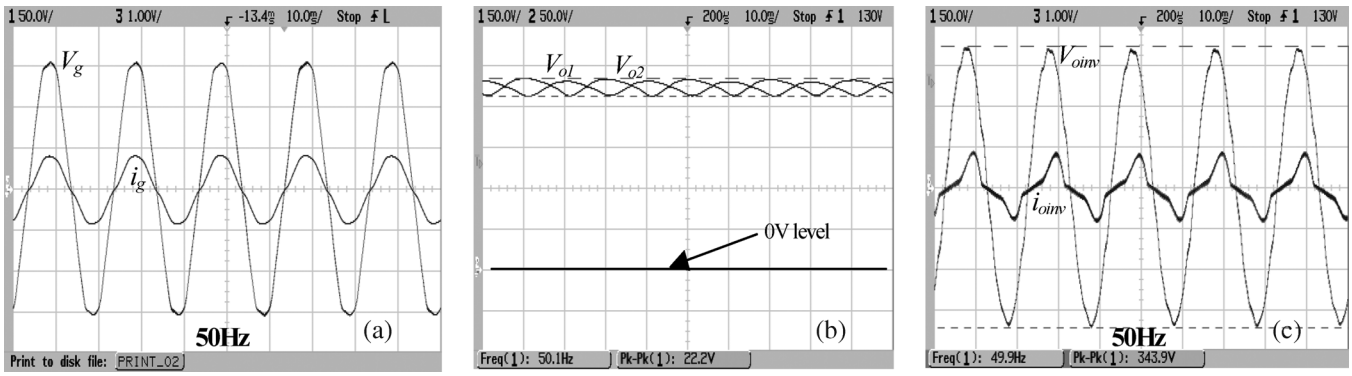

Fig. 21. AC–DC–AC application (50-Hz nonlinear load): (a) input voltage V_g (50 V/div) and input current i_g (10 A/div), (b) output voltages V_{o1} and V_{o2} (50 V/div), and (c) inverter output voltage V_{oinv} (50 V/div) and output current i_{oinv} (10 A/div).

B. AC–DC–AC Application

The objective of this test is to explore the performance of the single-phase half-bridge rectifier, with the proposed control technique in 1) single-phase high power factor input line conditioner, 2) transformerless UPS, and 3) static frequency changer applications. Some applications mentioned in 1) and 2) require the output frequency to be same as the input frequency, while some applications such as 2) and 3) may demand a different output frequency compared to the input frequency. In these applications, the output side inverter (see Fig. 15) might have linear and/or nonlinear loads. Therefore, considering all the above possibilities the given converter is tested at two different output frequencies, namely 50 and 60 Hz. At each output frequency, both linear and nonlinear loads are considered. In all these cases, the output inverter is operated with sine-triangle PWM scheme [18].

a) 50-Hz linear load: An inductive RL load is connected at the output of the inverter. The output power is 600 W at 50 Hz. The corresponding experimental results are shown in Fig. 20. The input current THD is 3.6%.

b) 50-Hz nonlinear load: A diode bridge rectifier load, in series with an inductor is connected at the output. The output power is 650 W at 50 Hz. The corresponding results are shown in Fig. 21. The input current THD is 3.9%.

c) 60 Hz linear load: An inductive RL load is connected at the output. The output power is 450 W at 60 Hz. The corresponding experimental results are shown in Fig. 22. The input current THD is found to be 4.2%.

d) 60 Hz nonlinear load: A diode bridge rectifier load in series with an inductor is connected at the output. The output power is 575 W at 60 Hz. The corresponding results are shown in Fig. 23. The input current THD is 4.5%.

Similar to (28)–(31) it can be shown that if the output frequency is 60 Hz and the input is 50 Hz, the currents through the capacitors C_1 and C_2 contain both 50-Hz and 60-Hz components as well as their respective second harmonic components. Hence, the ripple in V_{o1} and V_{o2} has a periodicity of 100 ms as seen in Figs. 22(b) and 23(b). It should be noted that the distorted currents in Figs. 21(c) and 23(c) are due to the nonlinear diode-bridge rectifier loads, which the load-side inverter (see Fig. 15) is supplying. Therefore, it is shown that irrespective of the output frequency and the type of load (linear/nonlinear), supplied by the load-side inverter, the half-bridge rectifier with the proposed control draws an input current with low distortion at near unity power factor as demonstrated by the experimental results in Figs. 17–23.

VIII. Conclusion

A simple, low-cost, constant frequency analog controller is proposed for the half-bridge PWM rectifier using the concept of one-cycle control or resistance emulation control. Two voltage controllers, each controlling each half of the dc bus and a modulator for the input current shaping are used in the controller. The required gating pulses are generated by comparing the input current with a suitable carrier in the modulator without using any complex mathematic operation (multiplier and/or divider), PLL,

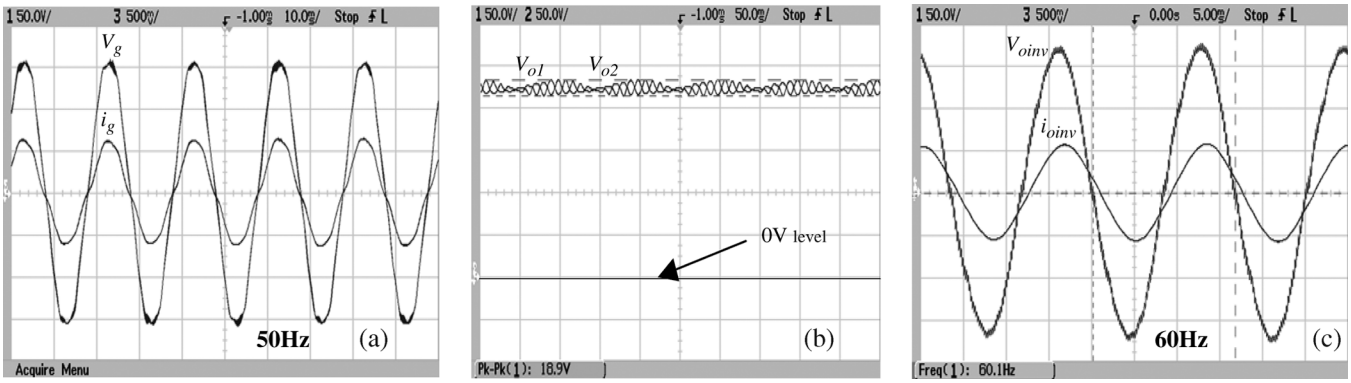

Fig. 22. AC–DC–AC application (60 Hz linear load): (a) input voltage V_g (50 V/div) and input current i_g (5 A/div), (b) output voltages V_{o1} and V_{o2} (50 V/div), and (c) inverter output voltage $V_{\rm oinv}$ (50 V/div) and output current $i_{\rm oinv}$ (5 A/div).

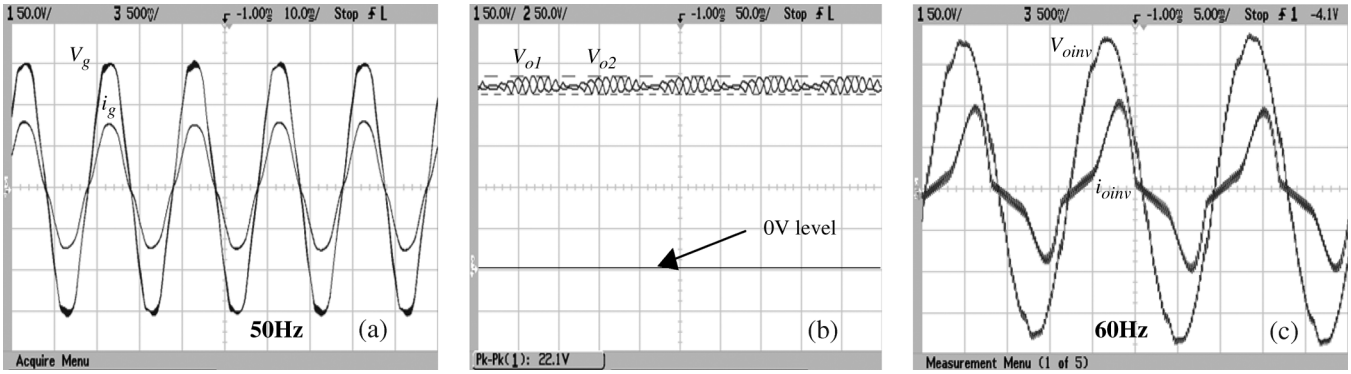

Fig. 23. AC–DC–AC application (60-Hz nonlinear load): (a) input voltage V_g (50 V/div) and input current i_g (5 A/div), (b) output voltages V_{o1} and V_{o2} (50 V/div), (c) inverter output voltage $V_{\rm oinv}$ (50 V/div) and output current $i_{\rm oinv}$ (5 A/div).

and input voltage sensing. The small signal analysis presented here is useful for the study of control of any converter topology involving a modulator instead of a current error amplifier as with the present work. It is shown that such a modulator-based control structure can be viewed as a current-controlled system with an outer voltage loop and an equivalent inner current loop for the purpose of analysis. Such a small signal model is useful in designing the voltage controller. Further the effect of the dc output voltage ripple on the input current distortion and the input current displacement can also be studied easily. Control of voltage unbalance in the proposed scheme for half-bridge rectifier essentially involves addition of certain dc component to the current reference of the equivalent current loop. The analysis helps us understand the similarity between the proposed controller and the existing controllers in the control of voltage unbalance. Complete design equations and calculation of converter losses are presented. The work achieves simplicity in control of a single-phase half-bridge rectifier without significant degradation in performance over the existing schemes as shown by simulation and experimental results. The experimental study involves ac–dc as well as ac–dc–ac application with linear and nonlinear loads. It is shown that irrespective of the output frequency and the type of load (linear/nonlinear), the half-bridge rectifier with the proposed control draws an input current with low distortion at near unity power factor. The proposed control method can easily be extended to a three-phase, four-wire PWM rectifier.

REFERENCES

[1] *IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems*, IEEE Std. 519-1992, 1992.

[2] *Electromagnetic Compatibility Part 3: Limits—Section 2: Limits for Harmonic Currents Emissions (equipment input current ≤16 A per phase)*, IEC 1000-3-2, 1995.

[3] V. Anunciada and B. Borges, "Power factor correction in single phase AC–DC conversion: control circuits for performance optimization," in *IEEE PESC'04 Conf.*, 2004, vol. 5, pp. 3775–3779.

[4] R. Srinivasan and R. Oruganti, "A unity power factor converter using half-bridge topology," *IEEE Trans. Power Electron.*, vol. 13, no. 3, pp. 487–500, May 1998.

[5] J. T. Boys and A. W. Green, "Current-forced single phase reversible rectifier," *Proc. Inst. Elect. Eng.*, vol. 136, no. 5, pt. B, pp. 205–211, 1989.

[6] T. Uematsu, T. Ikeda, N. Hirao, S. Totsuka, T. Ninomiya, and H. Kawamoto, "A study of the high performance single-phase UPS," in *Proc. IEEE PESC'98 Conf.*, 1998, vol. 2, pp. 1872–1878.

[7] G.-J. Su and T. Ohno, "A new topology for single phase UPS systems," in *Proc. IEEE Power Conv. Conf.*, Aug. 1997, vol. 2, pp. 913–918.

[8] Y.-K. Lo and C.-L. Chen, "A voltage-mode controlled high-input-power-factor AC line conditioner with minimized output voltage harmonics," in *Proc. IEEE PESC'94 Conf.*, 1994, vol. 1, pp. 369–374.

[9] S. B. Bekiarov and A. Emadi, "A new on-line single-phase to three-phase UPS topology with reduced number of switches," in *Proc. IEEE PESC'03 Conf.*, 2003, vol. 2, pp. 900–906.

[10] M. E. Fraser, C. D. Manning, and B. M. Wells, "Transformerless four-wire PWM rectifier and its application in AC–DC–AC converters," *Proc. Inst. Elect.. Eng.*, vol. 142, no. 6, pp. 410–416, Nov. 1995.

[11] J. Salaet, J. Bordonau, and J. Peracaula, "SVM based control of a single-phase half-bridge rectifier under power factor correction and balanced operation," in *Proc. IEEE ISIE'00 Conf.*, 2000, vol. 1, pp. 130–134.

[12] M.-F. Tsai, K.-L. Chai, and Y.-Y. Tzou, "CPLD realization of a digital programmable PFC control IC for single-phase half-bridge boost AC–DC converters," in *Proc. IEEE PESC'04 Conf.*, 2004, vol. 2, pp. 1134–1139.
[13] C. Qiao and K. M. Smedley, "Unified constant-frequency integration control of three-phase standard bridge boost rectifiers with power-factor correction," *IEEE Trans. Ind. Electron.*, vol. 50, no. 1, pp. 100–107, Feb. 2003.
[14] D. Maksimovic, Y. Jang, and R. Erickson, "Nonlinear-carrier control for high-power-factor boost rectifiers," *IEEE Trans. Power Electron.*, vol. 11, no. 4, pp. 578–584, Jul. 1996.
[15] S. Chattopadhyay, V. Ramanarayanan, and V. Jayashankar, "Predictive switching modulator for current mode control of high power factor boost rectifier," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 114–123, Jan. 2003.
[16] Y.-K. Lo, T.-H. Song, and H.-J. Chiu, "Analysis and elimination of voltage imbalance between the split capacitors in half-bridge boost rectifiers," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 1175–1177, Oct. 2002.
[17] Unitrode, Inc., "Modeling, Analysis and Compensation of the Current-Mode Converter," Appl. Note U-97, 2006, pp. 3-43–3-48.
[18] R. W. Erickson, *Fundamentals of Power Electronics*, 1st ed. New York: Chapman & Hall, May 1997.

Rajesh Ghosh received the Diploma degree from Coochbehar Polytechnic, Coochbehar, West Bengal, in 1994, the B.E degree from Jadavpur University, Kolkata, India, in 2000, and the M.Tech. degree from the Indian Institute of Technology, Kanpur, in 2002, all in electrical engineering, and is currently pursuing the Ph. D degree in the Electrical Engineering Department, Indian Institute of Science, Bangalore.

From 1994 to 2000, he was with the Substations Department, Calcutta Electric Supply Corporation Ltd (CESC), involved in the maintenance and erection and commissioning of LT/HT switchgears, power, and distribution transformers. From 2002 to 2003, he was with GE Global Research Center (JFWTC), Bangalore, as an Electrical Engineer. His research interests are design, analysis and control of switched-mode power converters, and active power filters.

G. Narayanan (S'99–M'01) received the B.E. degree from Anna University, Madras, India, in 1992, the M.Tech. degree from the Indian Institute of Technology, Kharagpur, in 1994, and the Ph.D. degree from the Indian Institute of Science, Bangalore, in 2000.

He is currently an Assistant Professor in the Department of Electrical Engineering, Indian Institute of Science. His research interests include ac drives, pulsewidth modulation, multilevel inverters, and protection of power devices.

Dr. Narayanan received the Innovative Student Project Award for his Ph.D. work from the Indian National Academy of Engineering in 2000, and the Young Scientist Award from the Indian National Science Academy in 2003.