A Novel Resonant Transition Half-Bridge Converter

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***Abstract* – Resonant transition converters are characterized by low switching losses and low conduction losses. This paper proposes a novel half-bridge resonant transition converter with soft switching properties. The improvised half-bridge converter uses two additional switches and two diodes. The additional switches introduce freewheeling intervals in the primary circuit and thus enable loss-less switching. In classical half-bridge converter, the transformer primary is left open during two sub-intervals in a period. On account of this feature, the turn-on of the switch in these converters is always hard. The new circuit topology converts these open circuit intervals into freewheeling intervals with such a modification, all trapped energy in the core is conserved to achieve ZVS during all the switching transition. The principle of operation of the proposed topology is explained. Design procedure is explained. Design procedure is validated through a prototype converter rated 300kHz, 640W half-bridge converter.**

Keywords – Half-bridge converter, Push-pull converter, ZVS, Resonant transition.

I. INTRODUCTION

Switched mode power supplies (SMPS) are being extensively used in most power conversion processes. They are efficient and compact. The analysis, design and modeling processes have all matured in the past three decades. Most of these developments centered around hard-switching converters, where the switching frequency was limited to a few 10's of kHz. The present direction of evolution in SMPS is towards higher efficiency and higher power density. These twin objectives demand high switching frequency and low overall losses. Soft switching results in practically zero switching losses and extends the switching frequency to 100's of kHz and beyond. The soft switching converters belong to several families namely resonant load [1], resonant switch [2] resonant transition [3], [5] and more recently active clamped circuit topologies [4]. The resonant load converters depend on the characteristics of the load to achieve soft switching. The resonant switch converters have additional elements in the switch enabling loss-less switching. Resonant transition converters employ the parasitic of the circuit to achieve loss-less switching.

This paper presents novel variant of half-bridge DC-DC converter with soft switching properties. Half-bridge converter is a popular power converter at medium power levels. Half-bridge converter is characterized by circuit intervals when both power transfer switches are off. Such circuits exhibit hard switching and not readily adaptable to soft switching. The proposed topology uses two additional switches and two diodes. The additional switches introduce freewheeling intervals in the circuit and enable loss-less switching. The following are the features are the new circuit,

1) Loss-less switching transition for all the switches employed.
2) Switch stress similar to hard-switched PWM converter.
3) Conduction loss is almost same as hard-switched PWM converter.
4) Control and small signal behavior similar to hard-switched PWM converter.

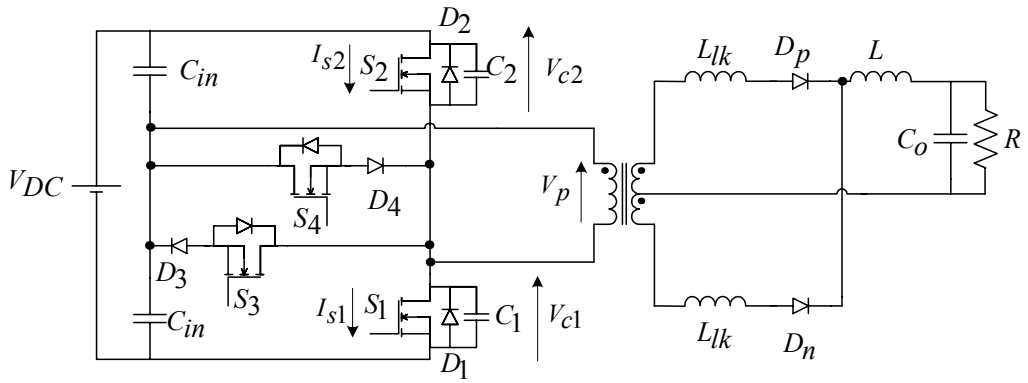

Fig. 1 ZVS Half-bridge DC-DC Converter

II. PROPOSED CIRCUIT AND OPERATION

Fig. 1 shows the proposed ZVS half-bridge converter. This circuit is obtained from the hard-switched half-bridge converter by connecting two switches (S_3 & S_4) and two diodes (D_3 & D_4) as in fig. 1. The leakage inductance of the transformer is lumped on the secondary side and represented as L_{lk} in fig. 1. C_1 and C_2 are the snubber capacitors.

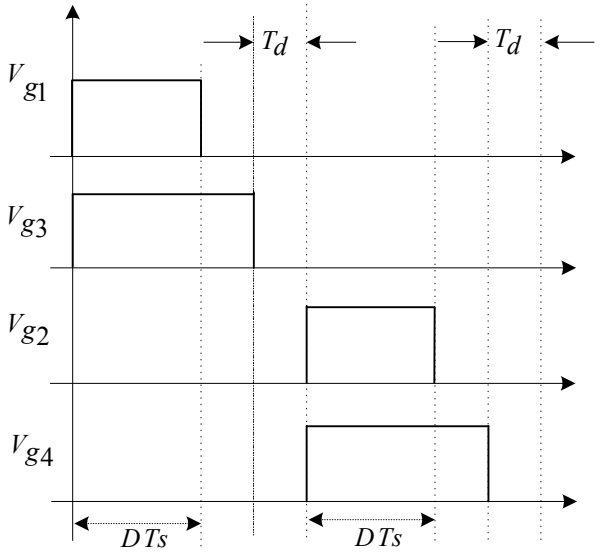

Fig. 2 Control Pulses

Fig. 2 indicates the gate pulses V_{g1}, V_{g2}, V_{g3} and V_{g4} for the switches S_1, S_2, S_3 and S_4 respectively. S_3 and S_4 have a duty ratio of nearly 50% (with a small dead time). The dead time (T_d) is also shown in fig. 2.

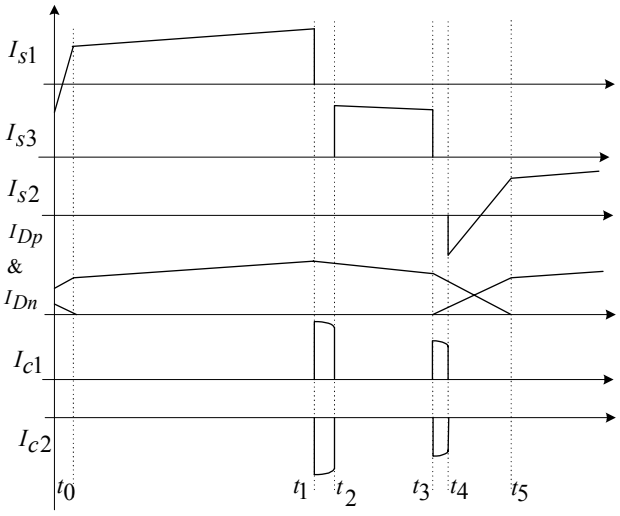

Fig. 3 Idealized waveforms

Idealized operation of the circuit is explained by a set of 6 intervals. Fig. 3 shows the idealized waveforms of primary switch current, snubber capacitor current and secondary diode currents.

The following are the assumptions made during the idealized analysis:

1. Switching devices are ideal.
2. Diodes are ideal.
3. Device output capacitance is neglected. Only the effect of snubber capacitor is considered.

Interval T_1 ($t_0 < t < t_1$)

In interval T_1, S_1 and S_3 are on. When S_1 is conducting, diode D_3 is reverse biased in the primary circuit. In the secondary circuit diode Dp is forward biased. This interval is known as power transfer interval. During this interval power is transferred from primary to secondary. Fig. 4 shows the conduction path and fig. 5 shows the equivalent circuit for interval T_1.

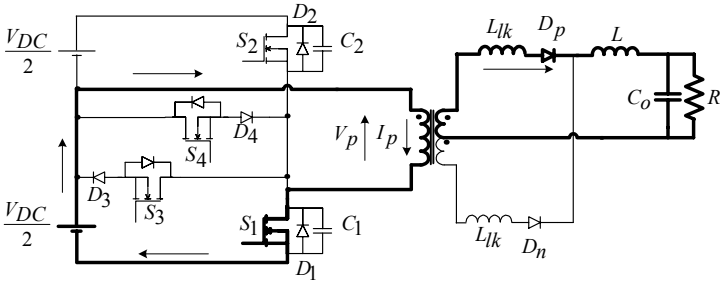

Fig. 4 Conducting path in interval T_1

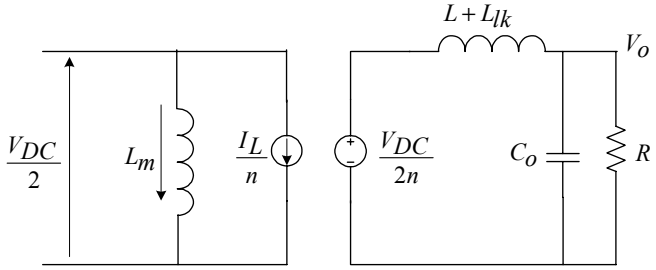

Fig. 5 Equivalent circuit for interval T_1

Interval T_2 ($t_1 < t < t_2$)

Interval T_2 begins when S_1 is turned off. The snubber capacitor C_1 assists the turn-off process of S_1. As the turn-off process is capacitor assisted, the turn-off process is low loss switching transition. The magnetizing current and reflected current charge C_1 from 0 to $\frac{V_{DC}}{2}$ and discharge C_2 from V_{DC} to $\frac{V_{DC}}{2}$. Although S_3 is on, D_3 is still reverse biased because the voltage V_{C1} has not reached to $\frac{V_{DC}}{2}$.

In the secondary circuit D_p takes the load current. This interval is known as resonant transition-I interval. Fig. 6 shows the conduction path and fig. 7 shows the equivalent circuit for interval T_2.

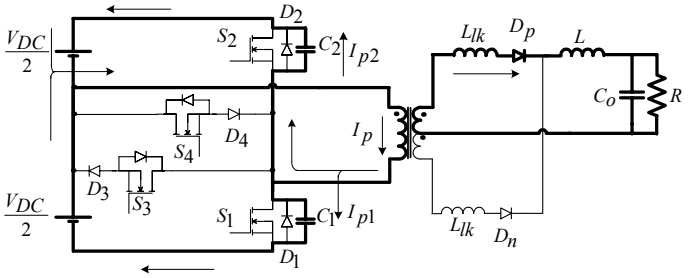

Fig. 6 Conducting path in interval T_2

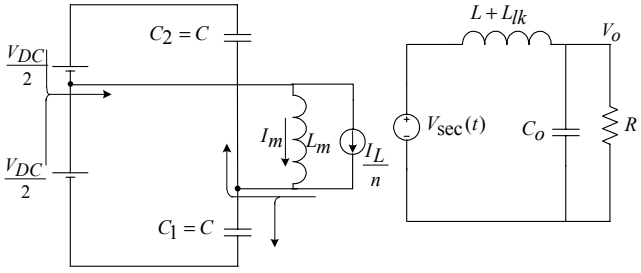

Fig. 7 Equivalent circuit for interval T_2

Interval T_3 ($t_2 < t < t_3$)

Interval T_3 begins when C_1 charged to $\frac{V_{DC}}{2}$. As C_1 charged to $\frac{V_{DC}}{2}$, D_3 is forward biased. The magnetizing current and reflected current I_p freewheel through S_3 and D_3. This interval is known as freewheeling interval. The leakage inductance L_{lk} ensures that only D_p takes the load current. Fig. 8 shows the conduction path and fig. 9 shows the equivalent circuit for interval T_3.

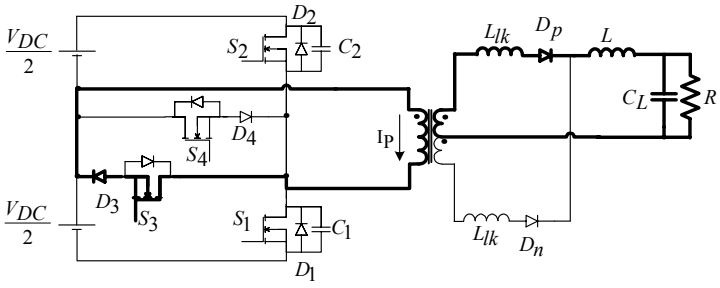

Fig. 8 Conducting path in interval T_3

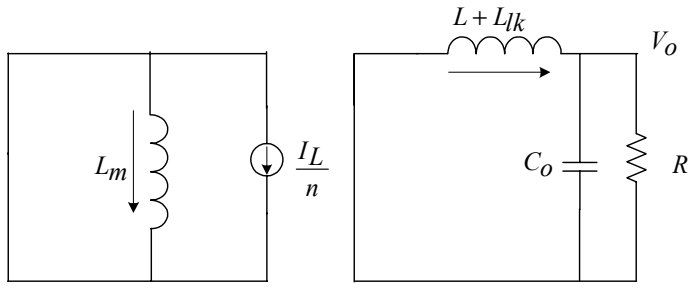

Fig. 9 Equivalent circuit for interval T_3

Interval T_4 ($t_3 < t < t_4$)

At the start ($t = t_3$) of this interval T_4, S_3 is switched off. The magnetizing current and reflected current charge C_1 from $\frac{V_{DC}}{2}$ to V_{DC} and discharge C_2 from $\frac{V_{DC}}{2}$ to 0. This interval is known as resonant transition – II interval. From the equivalent circuit (fig. 11) it is seen that reflected current and magnetizing current discharges C_2. So magnetizing inductance and leakage inductance has to be designed to discharge C_2. In the secondary circuit the load current starts shifting from D_p to D_n. Fig. 10 shows the conduction path and fig. 11 shows the equivalent circuit for interval T_4.

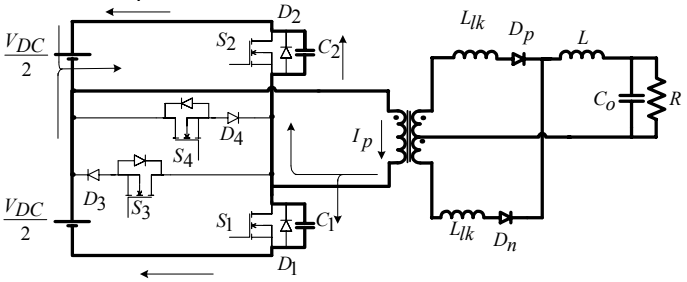

Fig. 10 Conducting path in interval T_4

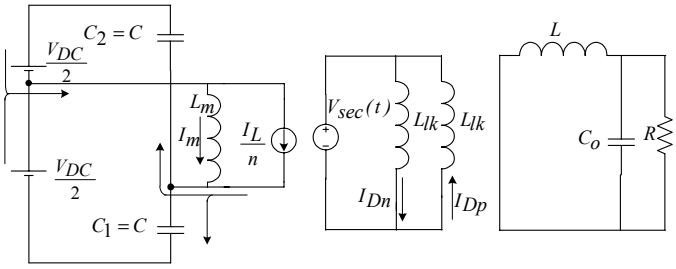

Fig. 11 Equivalent circuit for interval T_4

Interval T_5 ($t_4 < t < t_5$)

Interval T_5 begins when C_2 is discharged fully. As C_2 is discharged, the magnetizing current and reflected load current forward biases D_2. The magnetizing current and

reflected load current (I_p) flow through D_2. When current is flowing through D_2, S_2 and S_4 are turned on. Thus zero voltage switching of device S_2 is achieved. This interval is known as ZVS interval. When S_2 is on D_4 is reverse biased in the primary circuit.

When the primary current direction changes its direction, S_2 takes the current from D_2. At the end of this interval D_p blocks fully and D_n takes the full load current. The time of interval T_5 is decided by the leakage inductance. Fig. 12 shows the conduction path and fig. 13 shows the equivalent circuit for interval T_5.

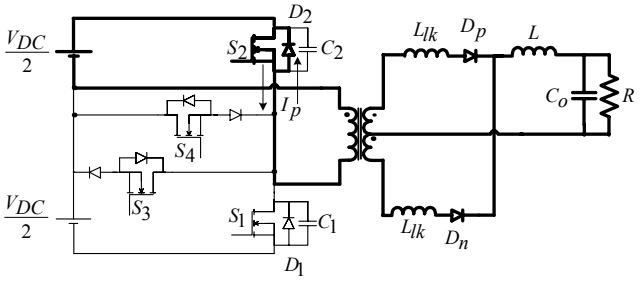

Fig. 12 Conducting path in interval T_5

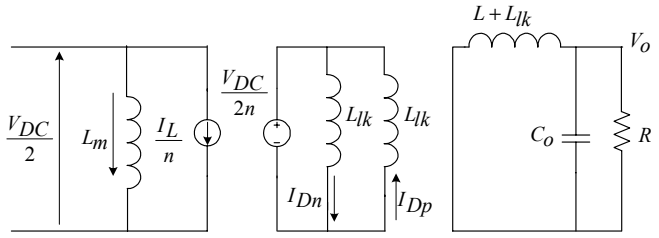

Fig. 13 Equivalent circuit for interval T_5

Interval T_6 ($t > t_5$)

This interval is known as power transfer interval. During this interval S_2 and S_4 are on in the primary circuit. D_4 is reverse biased in the primary circuit. D_n is forward biased in the secondary circuit. Fig. 14 shows the conduction path in interval T_6. This interval is followed by similar sets of intervals as before to achieve ZVS for S_1. Interval T_6 is the complimentary interval of T_1. Each cycle consists of 10 intervals. These are given in table 1.

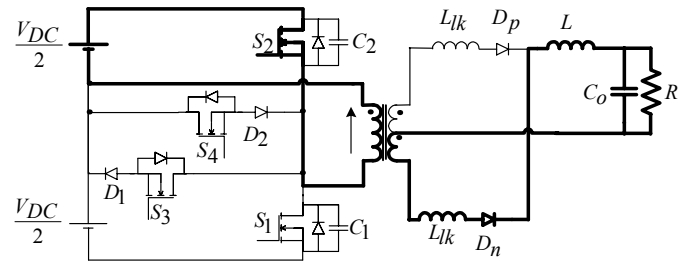

Fig. 14 Conducting path in interval T_6

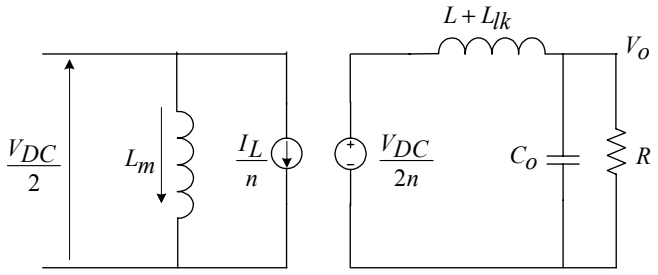

Fig. 15 Equivalent circuit for interval T_6

III. DESIGNING FOR ZVS

Parameters affecting ZVS

There are various parameters affecting ZVS. They are magnetizing current, leakage inductance, time delay, load current and device output capacitance. The choice of the various parameters is a trade-off between switching loss and conduction loss. The following section explains about the various parameters affecting ZVS.

(a) Magnetizing current

Magnetizing current aids ZVS. The magnetizing current is always in the direction to discharge the device output and snubber capacitance. Hence higher the value of magnetizing current is good from the ZVS point of view. But increase in magnetizing current increases the conduction loss and peak current.

(b) Leakage inductance

Leakage inductance of the transformer aids ZVS. Leakage inductance limits rate of reversal of reflected current in the primary circuit. Higher value of leakage inductance means more energy is available to discharge the device output capacitance and snubber capacitance. But increase in leakage inductance decreases the effective duty ratio. Hence utilization of the installed components is less. Further leakage inductance resonates with junction capacitance of diode and causes severe ringing in the secondary circuit.

(c) Snubber capacitance and device output capacitance

Snubber capacitance and device output capacitance together called as effective capacitance. Increasing the value of effective capacitance reduces the turn-off switching loss. Further it will reduce any voltage spike that is caused during turn-off transition. But higher value of effective capacitance demands more energy to be stored in magnetizing inductance and leakage inductance.

(d) Time delay

Fig. 16 shows the voltage across the S_2, current through S_2 and current through the effective capacitance C_2 during ZVS instant. The operation of the circuit during ZVS is explained through 3 sub-intervals. The sub-intervals are mentioned in the fig. 16 as τ_1, τ_2 and τ_3.

Interval T_4 (Resonant transition – II interval) is same as the sub-interval τ_1. During this sub-interval - τ_1 the capacitance C_2 discharge from $\frac{V_{DC}}{2}$ to 0. If the switch is turned on during this sub-interval - τ_1 results in hard

switching. The time of discharge of the capacitor depends only on the reactive elements (leakage inductance and effective capacitance).

During sub-interval τ_2 the body diode of the switch conducts. As body diode of the switch is conducting during this sub-interval - τ_2, If the switch is turned during sub-interval τ_2 ZVS can be achieved. The time of sub-interval τ_2 depends on the reflected current. Higher load current increases the sub-interval τ_2. This is shown in fig. 16 through simulation results. If the switch is not turned on during sub-interval τ_2, the effective capacitance charges again. So the switching will be hard. So, time delay of the circuit should be above τ_1 and below ($\tau_1 + \tau_2$).

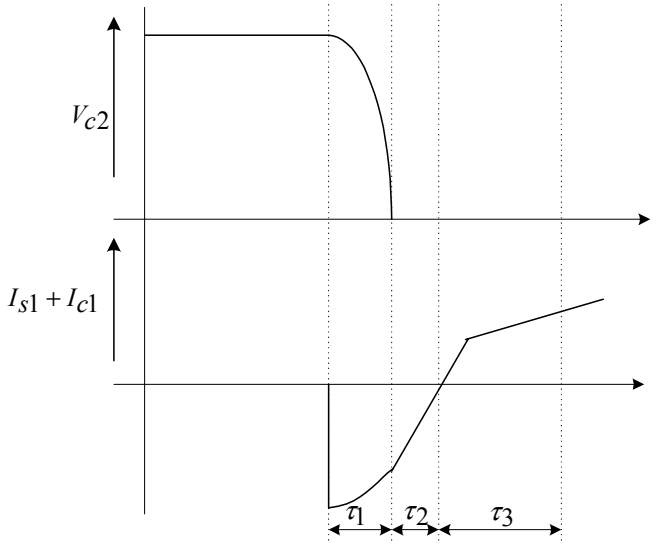

Fig. 16 Idealized waveforms during ZVS

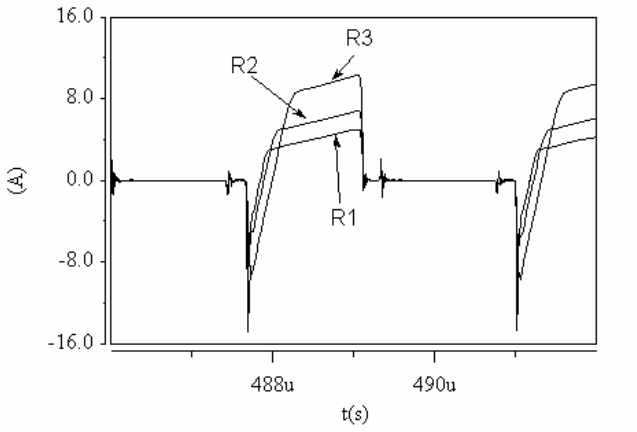

Fig. 17 switch current during ZVS transition
(For different value of load resistance, R1>R2>R3)

(f) Design Procedure

There are two important parameters which decides the ZVS, they are

1. Energy available in leakage (secondary leakage inductance) and magnetizing should be sufficient to discharge the device output capacitance and snubber capacitance.
2. Sufficient time delay should be available to discharge the device output capacitance.

Fig. 18 shows the equivalent circuit in the primary side during the interval T_4.

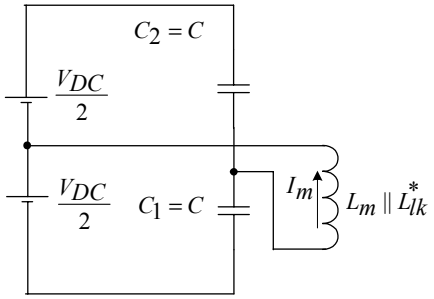

Fig. 18
Equivalent circuit in the primary side during interval T4

From the equivalent circuit the condition to achieve ZVS can be determined.

The condition is,

$$\frac{V_{DC}}{2} \le i(0)\sqrt{\frac{L}{2C}};\ i(0) = I_m + I_{refl} \qquad [1]$$

Also the minimum time required discharge the effective capacitance could be determined from the equivalent circuit in fig. 18.

$$T = \pi\sqrt{2LC} \text{ is the total time period}$$

$$\therefore \text{Minimum time delay} = T_d = \frac{T}{4} = \pi\sqrt{\frac{LC}{2}} \qquad [2]$$

The following are the design steps to be followed,

Step: 1 - Based on switching frequency and device characteristics select the time delay and effective capacitance (output capacitance and snubber capacitance).

Step: 2 - Calculate the L from the equation 2. Calculated value of L is approximately equal to L_{lk}^* because magnetizing inductance L_m is much higher than the leakage inductance.

Step: 3 - If the equation 1, is not satisfied with the value of the leakage inductance then magnetizing current has to be increased to satisfy the equation 1.

Interval	Conducting devices	V_{c1}	V_{c2}	V_p	I_{Dp}	I_{Dn}	Slope of the Inductor (L) current
T_1	S_1, D_p	0	V_{DC}	$\frac{V_{DC}}{2}$	I_L	0	$\left(\frac{1}{L+L_{lk}}\right)\left(\frac{V_{DC}}{n}-V_o\right)$
T_2	C_1, C_2, D_p	$V_{c1}(t)$	$V_{c2}(t)$	$\frac{V_{DC}}{2}-V_{c1}(t)$	I_L	0	$\left(\frac{1}{L+L_{lk}}\right)\left(\frac{\frac{V_{DC}}{2}-V_{c1}(t)}{n}-V_o\right)$
T_3	S_3, D_3, D_p	$\frac{V_{DC}}{2}$	$\frac{V_{DC}}{2}$	0	I_L	0	$\left(\frac{1}{L+L_{lk}}\right)(-V_o)$
T_4	C_1, C_2, D_p, D_n	$V_{c1}(t)$	$V_{c2}(t)$	$V_{c1}(t)-\frac{V_{DC}}{2}$	$I_L - I_{Dn}(t)$	$I_{Dn}(t)$	$-\frac{V_o}{L}$
T_5	D_2, S_2, D_p, D_n	V_{DC}	0	$-\frac{V_{DC}}{2}$	$I_L - I_{Dn}(t)$	$I_{Dn}(t)$	$-\frac{V_o}{L}$
T_6	S_2, D_n	V_{DC}	0	$-\frac{V_{DC}}{2}$	0	I_L	$\left(\frac{1}{L+L_{lk}}\right)\left(\frac{V_{DC}}{n}-V_o\right)$
T_7	C_1, C_2, D_n	$V_{c1}(t)$	$V_{c2}(t)$	$\frac{V_{DC}}{2}-V_{c1}(t)$	0	I_L	$\left(\frac{1}{L+L_{lk}}\right)\left(\frac{\frac{V_{DC}}{2}-V_{c1}(t)}{n}-V_o\right)$
T_8	S_4, D_4, D_n	$\frac{V_{DC}}{2}$	$\frac{V_{DC}}{2}$	0	0	I_L	$\left(\frac{1}{L+L_{lk}}\right)(-V_o)$
T_9	C_1, C_2, D_p, D_n	$V_{c1}(t)$	$V_{c1}(t)$	$V_{c1}(t)-\frac{V_{DC}}{2}$	$I_L - I_{Dn}(t)$	$I_{Dn}(t)$	$-\frac{V_o}{L}$
T_{10}	D_1, S_1, D_p, D_n	0	V_{DC}	$\frac{V_{DC}}{2}$	$I_L - I_{Dn}(t)$	$I_{Dn}(t)$	$-\frac{V_o}{L}$
T_1	S_1, D_p	0	V_{DC}	$\frac{V_{DC}}{2}$	I_L	0	$\left(\frac{1}{L+L_{lk}}\right)\left(\frac{V_{DC}}{n}-V_o\right)$

Table :1 Voltages and currents in the primary and secondary of in all the intervals

(g) ZVS limit

From the above design procedure (Equation 1) it is understood that ZVS is dependent on load current and magnetizing current. At lightly loaded condition it is difficult to achieve ZVS because the energy stored in the leakage inductance and magnetizing inductance may not be sufficient to discharge the effective capacitance prior to the turn-on of the switch. When the load current is high, the reflected current in the primary is more. So it is easy to achieve ZVS at higher load currents.

So for a wider ZVS range more energy has to be stored in leakage and magnetizing inductance. Wider ZVS range suffers from the disadvantage of higher conduction loss. Hence selecting the ZVS range is a trade off between conduction loss and switching loss.

Table shows the current and voltages in the circuit during different operating intervals. The values for $V_{c1}(t), V_{c2}(t), I_{Dn}(t)$ and $I_{Dp}(t)$ are found from the equivalent circuit in each intervals.

Prototype specification

Based on the design methodology proposed in the paper a prototype of ZVS half-bridge converter is built. The following are the I/O specifications of the power supply,

Input voltage - 170V
Output voltage - 32V
Output power - 640W
Switching frequency - 300kHz.

IV. Experimental Results

Fig. 19 shows the voltage across S_1 and current through transformer. Fig. 20 shows the voltage across S_1 and current through the transformer at the instant of ZVS. Fig. 20 shows the expanded time scale of fig. 19. From the fig. 20 it is clear that the current through the transformer is negative just before the switch is turned on. This indicates that the S_1 achieve ZVS.

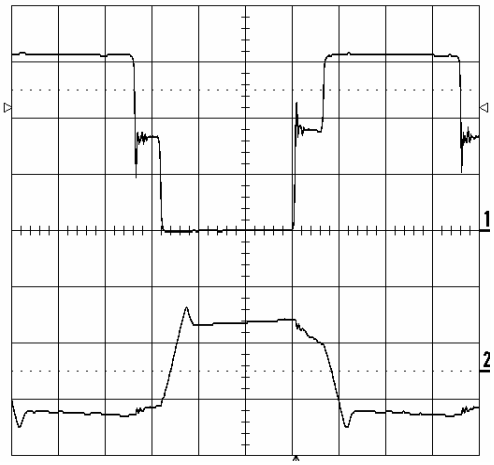

Fig. 19 Experimental Results of Voltage across S_1 and Current in the primary of Transformer
Scale:(V_{C1} – 50V/div, 0.5μs/div , I_P – 10A/div, 0.5μs/div)

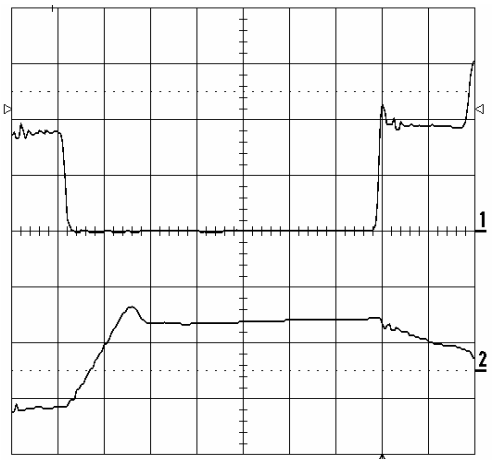

Fig. 20 Experimental Results of Voltage across S_2 and Current in the primary of Transformer
Scale:(V_{C1} – 50V/div, 0.2μs/div, I_P – 10A/div, 0.2μs/div)

Fig. 21 shows the voltage across S_2 and current through transformer. Fig. 22 shows the voltage across S_2 and current through the transformer at the instant of ZVS. Fig. 22 shows the expanded time scale of fig. 21. From the fig. 22 it is clear that the current through the transformer is negative just before the switch is turned on. This indicates that the S_2 achieve ZVS.

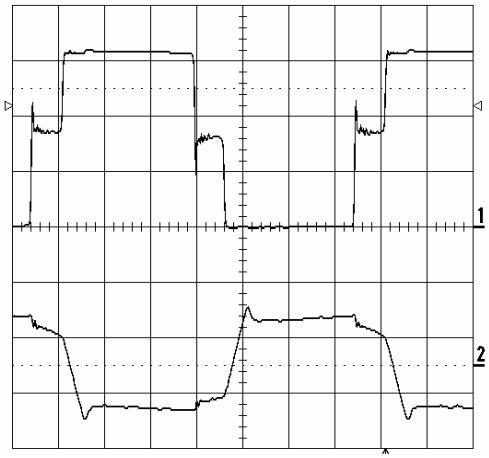

Fig. 21 Experimental Results of Voltage across S_2 and Current in the primary of Transformer
Scale:(V_{C2} – 50V/div, 0.5μs/div , I_P – 10A/div, 0.5μs/div)

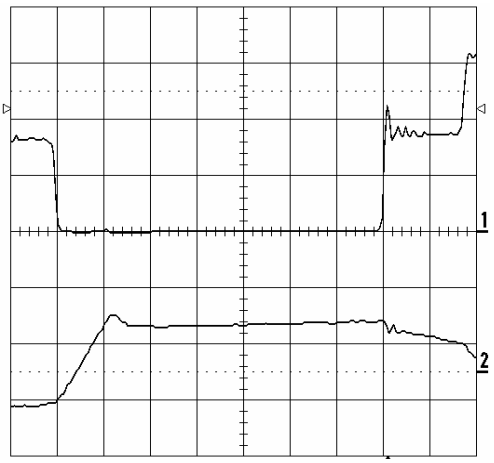

Fig. 22 Experimental Results of Voltage across S_1 and Current in the primary of Transformer *Scale:(V_{C1} – 50V/div, 0.2μs/div, I_P – 10A/div, 0.2μs/div)*

Fig. 23 shows the voltage across the secondary diode D_p. Additional inductance, which is added to aid ZVS, oscillates with the junction capacitance of D_p. From fig. 23 it is seen that the peak of the ringing voltage goes almost twice the nominal voltage. This is a disadvantage of the proposed topology. Fig. 24 shows the voltage across D_n.

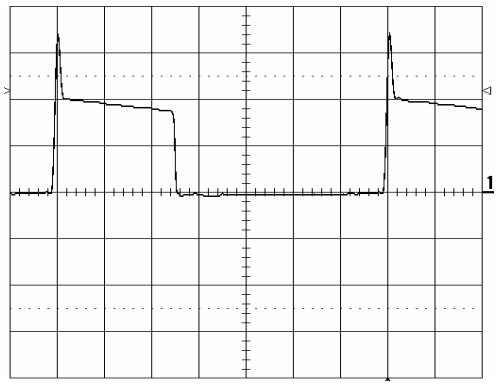

Fig. 23 Voltage across D_p

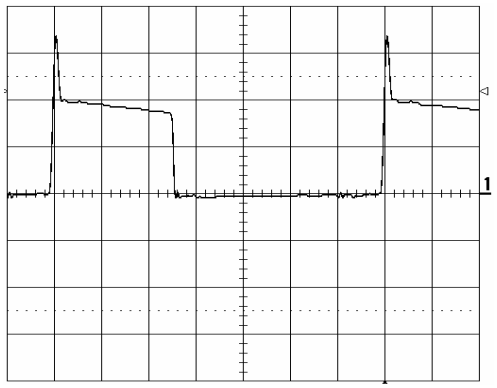

Fig. 24 Voltage across D_n

V. DYNAMIC ANALYSIS OF ZVS HALF-BRIDGE CONVERTER

The small signal dynamic model of half-bridge converter is similar to PWM hard-switched converter.

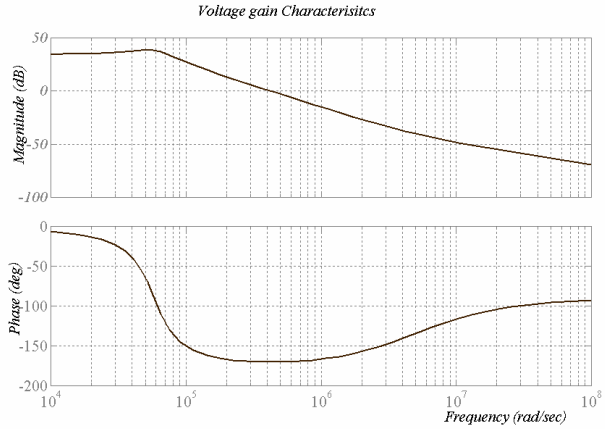

Fig. 25 Control voltage gain characteristics of ZVS half-bridge converter

The additional leakage inductances, which are introduced for achieving ZVS, are of small value when compared to the filter inductor. It is assumed that the filter inductor absorbs these leakage inductances. So the converter function remains same as the hard-switched PWM converter.

VI. CONCLUSION

ZVS limit of the converter is fixed at 12A. Fig. 26 shows the efficiency vs. load current. As discussed earlier the leakage inductance that introduced in the secondary circuit oscillates with the junction capacitance of the diode. The energy associated with the ringing is higher. Hence the efficiency of the converter comes down considerably because of leakage inductance. The proposed topology can be extended to push-pull converter also. Fig. 27 shows the resonant transition push-pull converter.

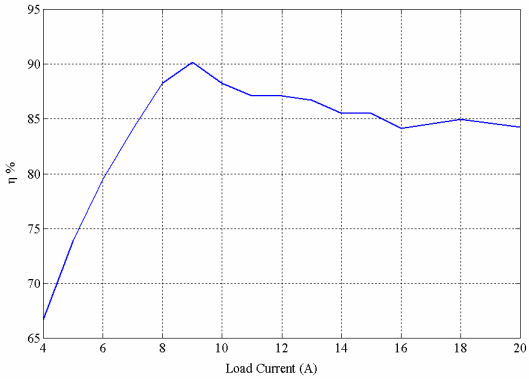

Fig. 26 Efficiency Vs load current

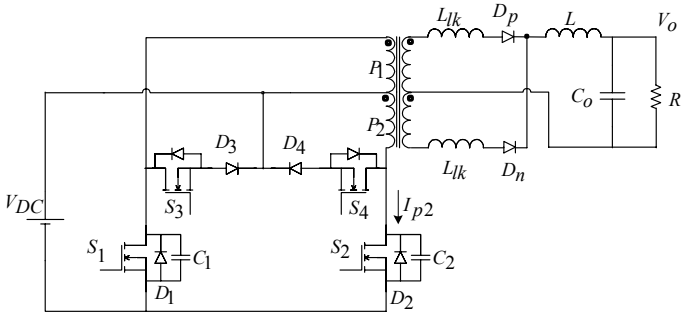

Fig. 27 ZVS Push-pull DC-DC Converter

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